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National Semiconductor Corporation

ALS/AS Logic Databook

For information on Low Power Schottky, Schottky and Transistor-Transistor Logic devices see the LS/S/TTL Logic databook.

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Charles E. Sporck
President, Chief Executive Officer
National Semiconductor Corporation

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Charles E. Sporck
President, Chief Executive Officer
National Semiconductor Corporation

ALS/AS Logic
DATABOOK

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Section 1

Introduction to Bipolar Logic

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Guide to Bipolar Logic Device Families

Since the introduction of the first saturating logic bipolar integrated circuit family (DM54/DM74), there have been many developments in the process and manufacturing technologies as well as circuit design techniques which have produced new generations (families) of bipolar logic devices. Each generation had advantages and disadvantages over the previous generations. Today National provides six bipolar logic families.

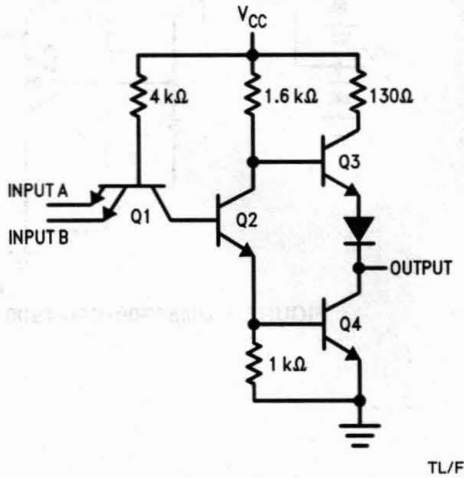
TTL	(DM54/DM74)
Low Power	(DM54L/DM74L)
Low Power Schottky	(DM54LS/DM74LS)
Advanced Low Power Schottky	(DM54ALS/DM74ALS)
Schottky	(DM54S/DM74S)
Advanced Schottky	(DM54AS/DM74AS)

TTL LOGIC (DM54/DM74)

TTL logic was the first saturating logic integrated circuit family introduced, thus setting the standard for all the future families. It offers a combination of speed, power consumption, output source and sink capabilities suitable for most applications. This family offers the greatest variety of logic functions. The basic gate (see *Figure 1*) features a multiple-emitter input configuration for fast switching speeds, active pull-up output to provide a low driving source impedance which also improves noise margin and device speed. Typical device power dissipation is 10 mW per gate and the typical propagation delay is 10 ns when driving a 15 pF/400Ω load.

LOW POWER (DM54L/DM74L)

The low power family has essentially the same circuit configuration as the TTL devices. The resistor values, however, are increased by nearly tenfold, which results in tremendous reduction of power dissipation to less than $1/10$ of the TTL family. Because of this reduction of power, the device speed is sacrificed. The propagation delays are increased threefold. These devices have a typical power dissipation of 1 mW per gate and typical propagation delay of 33 ns, making this family ideal for applications where power consumption and heat dissipation are the critical parameters.



TL/F/5534–1

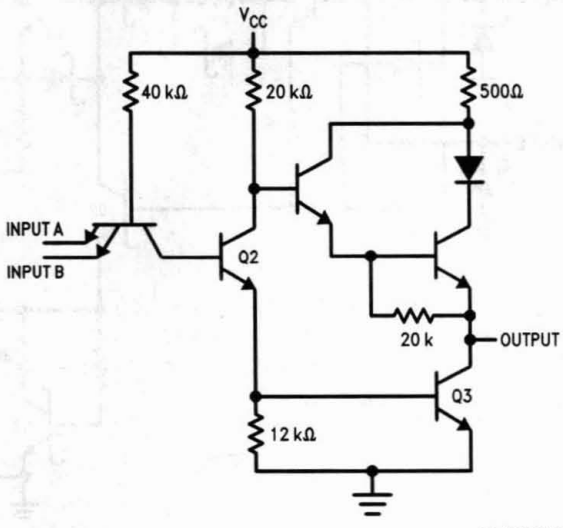
FIGURE 1. DM5400/DM7400

LOW POWER SCHOTTKY (DM54LS/DM74LS)

The low power Schottky family features a combined fivefold reduction in current and power when compared to the TTL family. Gold doping commonly used in the TTL devices reduces switching times at the expense of current gain. The LS process overcomes this limitation by using a surface barrier diode (Schottky diode) in the baker clamp configuration between the base and collector junction of the transistor. In this way, the transistor is never fully saturated and recovers quickly when base drive is interrupted. Using shallower diffusion and soft-saturating Schottky diode clamped transistors, higher current gains and faster turn-on times are obtained. The LS circuits do not use the multi-emitter inputs. They use diode-transistor inputs which are faster and give increased input breakdown voltage; the input threshold is ~0.1V lower than TTL. Another commonly used input is the vertical substrate PNP transistor. In addition to fast switching, it exhibits very high impedance at both the high and low input states, and the transistor's current gain (β) significantly reduces input loading and provides better output performance. The output structure is also modified with a Darlington transistor pair to increase speed and improve drive capability. An active pull-down transistor (Q3) is incorporated to yield a symmetrical transfer characteristic (squaring network). This family achieves circuit performance exceeding the standard TTL family at fractions of its power consumption. The typical device power dissipation is 2 mW per gate and typical propagation delay is 10 ns while driving a 15 pF/2 kΩ load.

SCHOTTKY (DM54S/DM74S)

This family features the high switching speed of unsaturated bipolar emitter-coupled logic, but consumes more power than standard TTL devices. To achieve this high speed, the Schottky barrier diode is incorporated as a clamp to divert the excess base current and to prevent the transistor from reaching deep saturation. The Schottky gate input and inter-



TL/F/5534–2

FIGURE 2. DM54L00/DM74L00

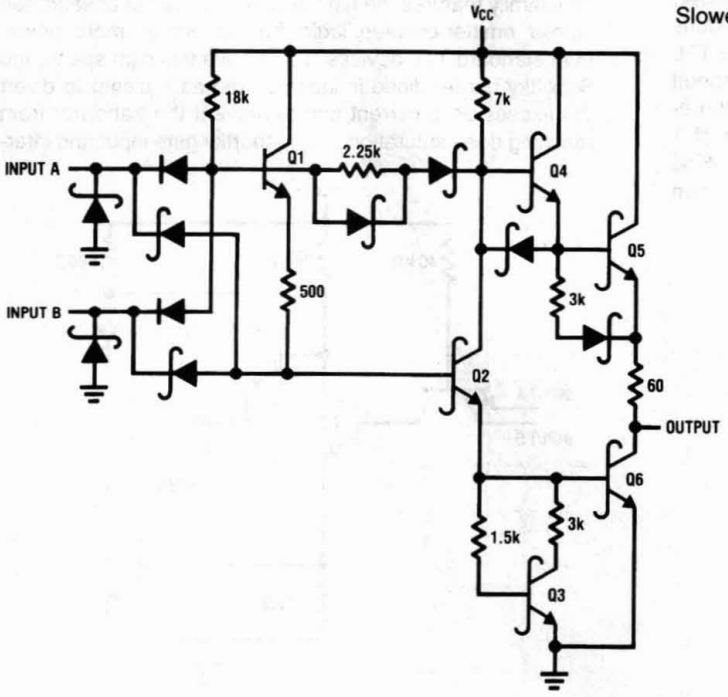
nal circuitry resemble the standard TTL gate except the resistor values are about one-half the TTL value. The output section has a Darlington transistor pair for pull-up and an active pull-down squaring network. This family has power dissipation of 20 mW per gate and propagation delays three times as fast as TTL devices with the average time of 3 ns while driving 15 pF/280Ω load.

ADVANCED LOW POWER SCHOTTKY (DM54ALS/DM74ALS)

The advanced low power Schottky family is one of the most advanced TTL families. It delivers twice the data handling efficiency and still provides up to 50% reduction in power consumption compared to the LS family. This is possible because of a new fabrication process where components are isolated by a selectively grown thick-oxide rather than the P-N junction used in conventional processes. This refined process, coupled with improved circuit design techniques, yields smaller component geometries, shallower diffusions, and lower junction capacitances. This enables the devices to have increased f_T in excess of 5 GHz and improved switching speeds by a factor of two, while offering much lower operating currents.

In addition to the pin-to-pin compatibility of the ALS family, a large number of MSI and LSI functions are introduced in the high density 24-pin 300 mil DIP. These devices offer the designers greater cost effectiveness with the advantages of reduced component count, reduced circuit board real-estate, increased functional capabilities per device and improved speed-power perfomance.

The basic ALS gate schematic is quite similar to the LS gate. It consists of either the PNP transistor or the diode inputs, Darlington transistor pair pull-up and active pull-down (squaring network) at the output. Since the shallower diffusions and thinner oxides will cause ALS devices to be more susceptible to damage from electro-static discharge, additional protection via a base-emitter shorted transistor is included at the input for rapid discharge of high voltage static electricity. Furthermore, the inputs and outputs are clamped by Schottky diodes to prevent them from swinging excessively below ground level. A buried N^+ guard ring around all input and output structures prevents crosstalk. The ALS family has a typical power dissipation of 1 mW per gate and typical propagation delay time of 4 ns into a 50 pF/2 kΩ load.



TL/F/5534–3

FIGURE 3. DM54LS00/DM74LS00

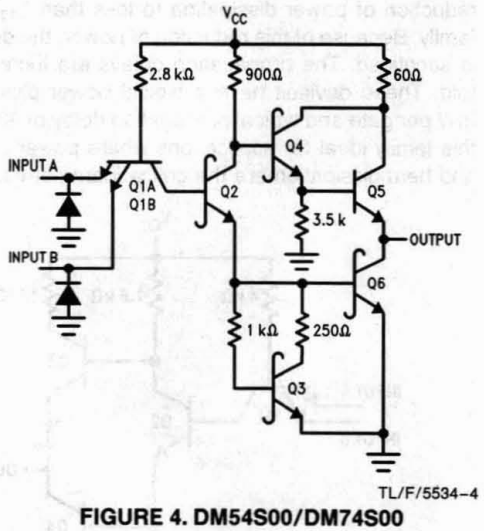
ADVANCED SCHOTTKY (DM54AS/DM74AS)

This family of devices is designed to meet the needs of the system designers who require the ultimate in speed. Utilizing Schottky barrier diode clamped transistors with shallower diffusions and advanced oxide-isolation fabrication techniques, the AS family achieves the fastest propagation delay that bipolar technology can offer. The AS family has virtually the same circuit configuration as the ALS family. It has PNP transistor or diode inputs with electrostatic protection base-emitter shorted transistors. The output totem-pole consists of a Darlington pair transistor pull-up and an active pull-down squaring network. The inputs and outputs are Schottky clamped to attenuate critical transmission line reflections. In addition, the circuit contains the "Miller Killer" network at the output section to improve output rise time and reduce power consumption during switching at high repetition rates. The AS family yields typical power dissipation of 7 mW per gate and propagation delay time of 1.5 ns when driving a 50 pF/2 kΩ load.

SELECTING A FAMILY

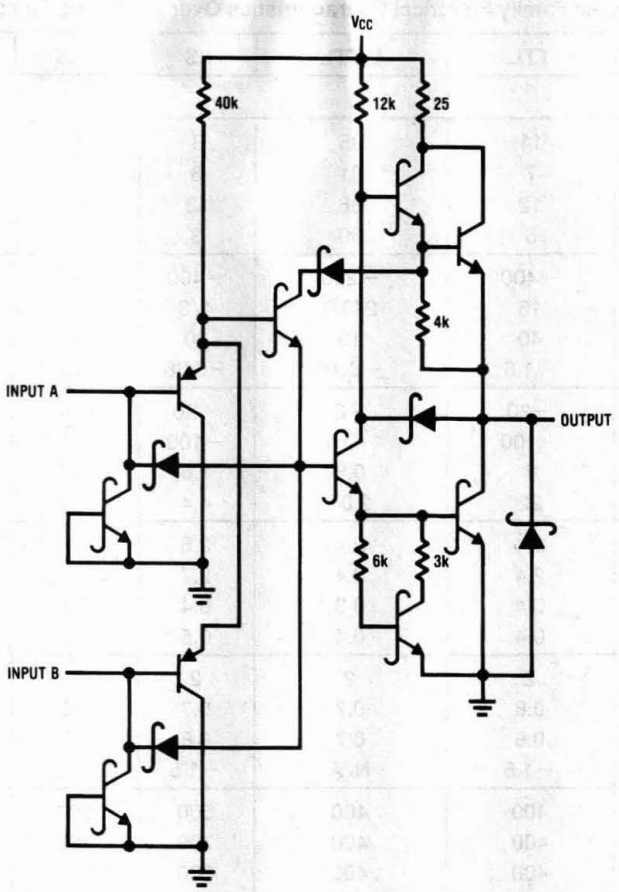
Two factors shoud be considered when choosing a logic family for application, speed and power consumption. New logic families were created to improve the speed or lower the power consumption of the previous families. The following tables rate each family.

Speed		Power Consumption	
Fastest	AS	Low	L
	S		ALS
↓	ALS	↓	LS
	LS		AS
	TTL		TTL
Slowest	L	High	S



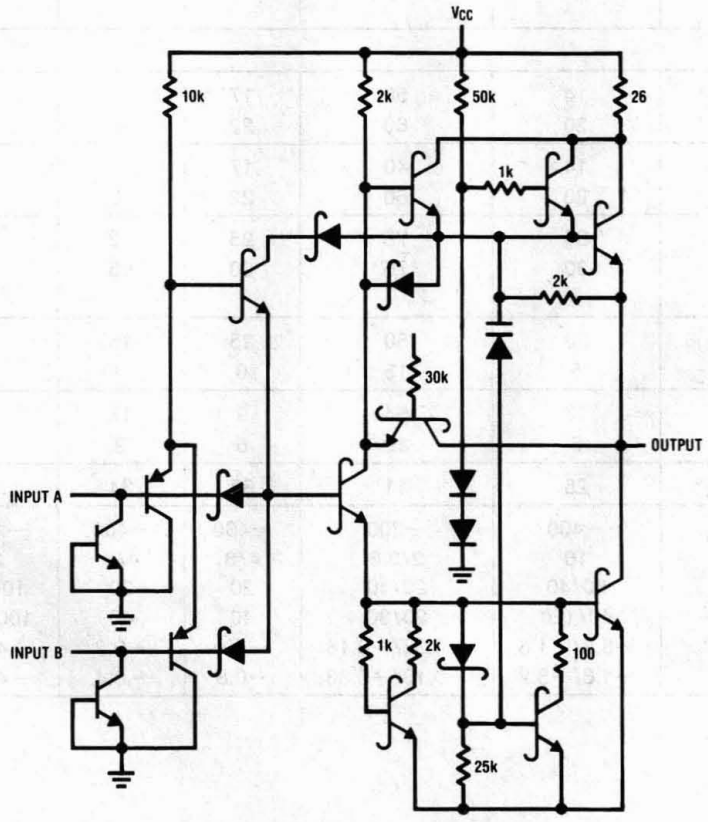
TL/F/5534–4

FIGURE 4. DM54S00/DM74S00



TL/F/5534–5

FIGURE 5. DM54ALS00/DM74ALS00



TL/F/5534–6

FIGURE 6. DM54AS00/DM74AS00

Bipolar Logic Family Electrical Characteristics Over Operating Temperatures

		TTL	L-TTL	LS	ALS	S	AS	Units
DM5400/DM7400								
2-Input NAND	t_{PLH}*	11	35	8	4	3	2.5	ns
	t_{PHL}*	7	31	8	4	3	1.5	ns
	t_r*	12	66	13	10	6	5	ns
	t_r*	5	30	3	6	3	3	ns
	I_{OH}	−400	−200	−400	−400	−1000	−2000	μA
Mil/Com	I_{OL}	16	2/3.6	4/8	4/8	20	20	mA
	I_{IH}	40	10	20	20	50	20	μA
	I_{IL}	−1.6	−0.18	−0.36	−0.20	−2	−0.50	mA
Min	I_{OS}	−20	−3	−20	−30	−40	−30	mA
Max	I_{OS}	−100	−15	−100	−112	−100	−112	mA
	I_{CCH}	8	0.8	1.6	0.85	16	3.2	mA
	I_{CCL}	22	2.04	4.4	3.0	36	16.1	mA
Mil	V_{OH}	2.4	2.4	2.5	$V_{CC}-2$	2.5	$V_{CC}-2$	V
Com	V_{OH}	2.4	2.4	2.7	$V_{CC}-2$	2.7	$V_{CC}-2$	V
Mil	V_{OL}	0.4	0.3	0.4	0.4	0.5	0.5	V
Com	V_{OL}	0.4	0.4	0.5	0.5	0.5	0.5	V
	V_{IH}	2	2	2	2	2	2	V
Mil	V_{IL}	0.8	0.7	0.7	0.8	0.8	0.8	V
Com	V_{IL}	0.8	0.7	0.8	0.8	0.8	0.8	V
	V_I	−1.5	N/A	−1.5	−1.5	−1.2	−1.2	V
Mil	NM-H	400	400	500	500	500	500	mV
Com	NM-H	400	400	700	700	700	700	mV
Mil	NM-L	400	400	300	400	400	300	mV
Com	NM-L	400	300	300	300	300	300	mV
Gate Power x Delay Product		100	20	20	4	60	30	pj
DM5474/DM7474								
D Flip-Flop	t_{PLH}*	14	50	17	5	8	6	ns
(CLK to Q)	t_{PHL}*	20	60	22	8	9	6	ns
(PS or	t_{PLH}*	14	40	17	7	6	4.5	ns
CLR to Q)	t_{PHL}*	20	60	22	10	12	6	ns
(CLK HI)	t_W	30	75	25	12	8	4	ns
(PS or CLR LOW)	t_W	30	75	20	15	9	4	ns
	t_{SET-UP}	20	50	25	15	3	3/2	ns
	t_{HOLD}	5	15	0	0	2	2/1	ns
	t_r*	13	64	9	17	4	5	ns
	t_r*	6	19	6	9	3	3	ns
	f_{MAX}*	25	11	33	34	95	125	MHz
	I_{OH}	−400	−200	−400	−400	−1000	−2000	μA
Mil/Com	I_{OL}	16	2/3.6	4/8	4/8	20	20	mA
(CLK/D)	I_{IH}	80/40	20/10	20	20	100/50	20	μA
(PS/CLR)	I_{IH}	40/120	20/30	40	40	100/150	40	μA
(CLK/D)	I_{IL}	−3.2/−1.6	−0.36/−0.18	−0.4	−0.2	−4/−2	−0.5	mA
(PS/CLR)	I_{IL}	−1.6/−3.2	−0.18/−0.36	−0.8	−0.4	−4/−6	−1.0	mA

Bipolar Logic Family Electrical Characteristics Over Operating Temperatures (Continued)

		TTL	L-TTL	LS	ALS	S	AS	Units
DM5474/DM7474 (Continued)								
Min	I_{OS}	−20/−18	−3	−20	−30	−40	−30	mA
Max	I_{OS}	−55	−15	−100	−112	−100	−112	mA
	I_{CC}	15	3	8	4	50	16	mA
Mil	V_{OH}	2.4	2.4	2.5	$V_{CC}-2$	2.5	$V_{CC}-2$	V
Com	V_{OH}	2.4	2.4	2.7	$V_{CC}-2$	2.7	$V_{CC}-2$	V
Mil	V_{OL}	0.4	0.3	0.4	0.4	0.5	0.5	V
Com	V_{OL}	0.4	0.4	0.5	0.5	0.5	0.5	V
	V_{IH}	2	2	2	2	2	2	V
Mil/Com	V_{IL}	0.8	0.7	0.7/0.8	0.8	0.8	0.8	V
	V_I	−1.5	N/A	−1.5	−1.5	−1.2	−1.2	V
Mil	NM-H	400	400	500	500	500	500	mV
Com	NM-H	400	400	700	700	700	700	mV
Mil	NM-L	400	400	400	400	300	300	mV
Com	NM-L	400	300	300	300	300	300	mV

Note: See Test Waveforms in this section for loading conditions, t_r and t_f are measured from 10% to 90% of waveform.

Note: NM-H is noise margin high. NM-L is noise margin low.

*Typical values. Other values are limit values.

Bipolar Logic Family Output Source/Sink Capability: 54/74 Families

Output			TTL	L-TTL	LS	ALS	S	AS	Units
Standard	Mil	I_{OH}	−0.4	−0.2	−0.4	−0.4	−1	−2	mA
	Com		−0.4	−0.2	−0.4	−0.4	−1	−2	mA
	Mil	I_{OL}	16	2	4	4	20	20	mA
	Com		16	3.6	8	8	20	20	mA
Buffered	Mil	I_{OH}	−0.8	−0.2	−0.4	−1	−1	−12	mA
	Com		−0.8	−0.2	−0.4	−2.6	−1	−15	mA
	Mil	I_{OL}	16	2	4	12	20	32	mA
	Com		16	3.6	8	24	20	48	mA
Bus Driver	Mil	I_{OH}	−2	N/A	−1	−12	−2	−48	mA
	Com		−5.2	N/A	−2.6	−15	−6.5	−48	mA
	Mil	I_{OL}	32	N/A	12	12	20	40	mA
	Com		32	N/A	24	24-48	20	48	mA

Fan-in and Fan-Out

	TTL	L-TTL	LS	ALS	S	AS	Units
Input Load: high	1	0.25	0.5	0.5	1.25	0.5	U.L.
Low	1	0.1125	0.225	0.125	1.25	0.3125	U.L.
Output Drive: High	10	2.25	5	5	12.5	12.5	U.L.
Low	10	5	10	10	25	50	U.L.

Note: UNIT LOAD (U.L.) Standard is referenced with respect to standard TTL device loading. It is defined as:

1 U.L. = 40 μA (HIGH STATE)

1 U.L. = 1.6 mA (LOW STATE)

IC Device Testing

Understanding the intent and practice of IC device testing is vital to insuring both the quality and proper usage of integrated circuits. All National Semiconductor data sheets list the AC and DC parameters with min and/or max limits, along with forcing functions. Understanding when a part fails the limit, and which forcing functions are really tighter, is critical when determining if an IC device is good or bad.

All of National's databook parameters are defined and guaranteed for "worst-case testing." Input loading currents (fan-in) are tested at the input and V_{CC} levels that most increase that loading, while the output drive capability (fan-out) is tested at the input and V_{CC} levels that most decrease that capability. I_{CC} is tested with the input conditions and V_{CC} level that yield the greatest I_{CC} value, and V_{CLAMP} is tested such that the negative voltage is maximized for the given clamp current. The fan-in and fan-out specs are contained in the I_{IH}, I_{OH}, I_{IL} and I_{OL} values. To guarantee these fan-in and fan-out limits at 10, the I_{OL} must be at least 10 times the I_{IL} and the I_{OH} must be at least 10 times the I_{IH}. Be aware that the fan-in and fan-out specifications are valid only within a given device family. The standard input loading and output drives are shown in Table I.

Notice that the I_{OL} is at least 10 times the I_{IL} and that the I_{OH} is greater than 10 times the I_{IH}. Also notice that these are "standard" drive and load currents for single sink outputs and inputs. Certain devices may have multiple load inputs where the input line goes to several input structures and has, say, 2 or 3 times the normal I_{IL} and I_{IH} loading. Certain other devices will have "triple sink" outputs that can drive 3 times the standard I_{OL} and I_{OH} currents. These devices are generally bus drivers, or drivers intended to drive highly capacitive loads. Finally, there are certain devices that have PNP inputs that reduce the I_{IL} loading to typically $-200\ \mu A$, thus allowing an increased DC fan-in of 20. One must therefore be careful when interfacing many different types of devices, even in the same family, and not simply go the "fan-out of 10" rule.

When dealing with any kind of device specification, it is important to note that there exists a *pair* of test conditions that define that test: the forcing function and the limit. Forcing functions appear under the column labeled "Conditions" and define the external operating constraints placed upon the device tested. The actual test limit defines how well the device responds to these constraints. For example, take the parameter $V_{OH(min)}$ for the DM74LS00. It is tested at $V_{CC(min)} = 4.75V$ commercial, using an $I_{OH} = -400\ \mu A$. If we required an $I_{OH} = -800\ \mu A$, this would be a "tighter" test, as the output voltage drops with increased I_{OH}. Hence, a device that would pass the $-800\ \mu A$ I_{OH} would also pass the $-400\ \mu A$ I_{OH}, but not necessarily the other way around. Futhermore, V_{OH} tracks with V_{CC}, which is why $V_{CC(min)}$ is the worst-case testing, and not $V_{CC(max)}$. Finally, forcing inputs to threshold represents the most difficult testing because this puts those inputs as close as possible to the actual switching point and guarantees that the device will meet the V_{IH}/V_{IL} spec.

TABLE I. Fan-In/Fan-Out

Device Family	Input Loading	Output Drive
TTL	$I_{IL} = -1.6$ mA $I_{IH} = 40\ \mu A$	$I_{OL} = 16$ mA $I_{OH} = -400\ \mu A$
Low Power Schottky	$I_{IL} = -400\ \mu A$ $I_{IH} = 20\ \mu A$	$I_{OL} = 4$ mA (Mil) $I_{OL} = 8$ mA (Com) $I_{OH} = -400\ \mu A$
Advanced Low Power Schottky	$I_{IL} = -100\ \mu A$ $I_{IH} = 20\ \mu A$	$I_{OL} = 4$ mA (Mil) $I_{OL} = 8$ mA (Com) $I_{OH} = -400\ \mu A$
Schottky	$I_{IL} = -2$ mA $I_{IH} = 50\ \mu A$	$I_{OL} = 20$ mA $I_{OH} = -1$ mA
Advanced Schottky	$I_{IL} = -500\ \mu A$ $I_{IH} = 20\ \mu A$	$I_{OL} = 20$ mA $I_{OH} = -2$ mA
Low Power	$I_{IL} = -180\ \mu A$ $I_{IH} = 10\ \mu A$	$I_{OL} = 2$ mA (Mil) $I_{OL} = 3.6$ mA (Com) $I_{OH} = -200\ \mu A$

Tables II and III show the "direction" of the looser/tighter testing for most common DC parameters. Notice that one can tighten either the forcing function or the limit, or both. Tightening either one is sufficient to insure a tighter test. Also notice the difference between max and min limits. For I_{OS} (double-ended limits), even though −20 mA is more positive than −100 mA, and is mathematically the max limit, the magnitude of the number is the determining factor when deciding which is the max limit. The negative sign simply implies the direction that the current is going, with a negative current leaving the device, and a positive current entering the device. Table II shows the direction of tighter forcing functions, while Table III shows the direction of tighter limits.

TABLE II. Looser/Tighter Forcing Functions Example: DM74LS00

Condition	Test	Looser	Nominal	Tighter	Units
I_{IK}	V_{IK}	−17	−18	−19	mA
I_{OH}	V_{OH}	−350	−400	−450	μA
I_{OL}	V_{OL}	3	4	5	mA
V_I	I_I	6.5	7	7.5	V
V_{IH}	I_{IH}	2.6	2.7	2.8	V
V_{IL}	I_{IL}	0.5	0.4	0.3	V
V_O	I_{OS}	0.1	0.0	−0.1	V
V_{CC}	I_{CC}	5.0	5.5	6.0	V

TABLE III. Looser/Tighter Test Limits Example: DM74LS00

Parameter	Looser	Nominal	Tighter	Units
$V_{IH(min)}$	2.1	2.0	1.9	V
$V_{IL(max)}$	0.7	0.8	0.9	V
$V_{IK(max)}$	−1.6	−1.5	−1.4	V
$V_{OH(min)}$	2.6	2.7	2.8	V
$V_{OL(max)}$	0.6	0.5	0.4	V
$I_{I(min)}$	6.5	7.0	7.5	V
$I_{IH(max)}$	50	40	30	μA
$I_{IL(max)}$	−450	−400	−390	μA
$I_{OS(max)}$	−110	−100	−90	mA
$I_{OS(min)}$	−10	−20	−30	mA
$I_{CCH(max)}$	1.7	1.6	1.5	mA
$I_{CCL(max)}$	4.5	4.4	4.3	mA

Following are the test set-ups that are used to test the DC parametrics. In each case, the gate connection, equivalent circuit schematic and resultant voltage/current plot are shown.

The indicated graphs are typical of LS products and are similiar to other bipolar logic families. The schematics shown are for single inversion devices and represent generalized circuits.

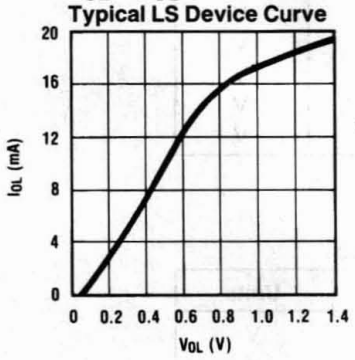
OUTPUT VOLTAGE LOW LEVEL (V_{OL})

Both inputs are connected to logic "1" values (assuming an inverting gate) and forced at the V_{IH} specs. V_{CC} minimum is used, and I_{OL} is forced on the output. The resulting V_{OL} is measured. For typical LS products, the military and commercial test points are indicated on the V_{OL} vs I_{OL} graph. In each case, the device must not exceed the V_{OL} spec when the I_{OL} current is being forced.

OUTPUT VOLTAGE HIGH LEVEL (V_{OH})

One input is tied high (any value above 2.0V) and the other input is forced at the V_{IL} threshold (assuming a single inversion gate). The minimum V_{CC} value is used. Each input is tested independently and the I_{OH} current is forced. The resulting V_{OH} is measured. The V_{OH} vs I_{OH} graph shows the military and commercial V_{OH}/I_{OH} test points for standard LS products.

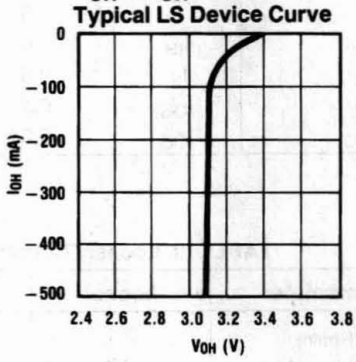
V_{OL} vs I_{OL}
Typical LS Device Curve



	I_{OL}	V_{OL}
Mil:	4.0 mA	0.40V
Com:	8.0 mA	0.50V

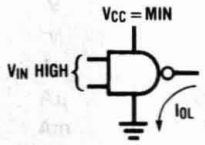
TL/F/6731–1

V_{OH} vs I_{OH}
Typical LS Device Curve



	I_{OH}	V_{OH}
Mil:	−400 μA	2.5V
Com:	−400 μA	2.7V

TL/F/6731–2



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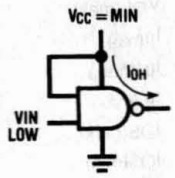

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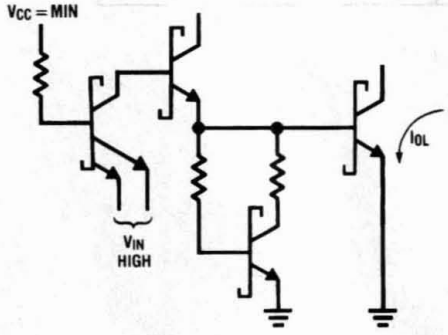

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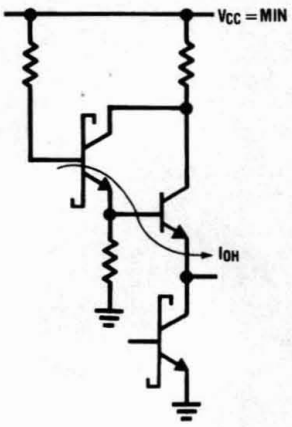


TL/F/6731–6

INPUT CURRENT HIGH LEVEL (I_{IH})

I_{IH} tests the input leakage in the high state. For MET, diode, and PNP input, the test set-up consists of all inputs except the one under test tied high (greater than V_{IH}). The remaining input has the V_{IH} value forced upon it, and the resultant I_{IH} is measured. This test checks for emitter-to-collector inverse transistor action for MET inputs, and reverse bias leakage for diode and PNP inputs.

For MET inputs, there is also an additional set-up for I_{IH} testing that checks for emitter-to-emitter transistor action. This is done with all the other inputs tied to ground.

MAXIMUM INPUT CURRENT (I_I)

I_I or BV_{IN} testing is the same as the emitter-to-collector leakage test (I_{IH}) and guarantees that the input will not pass more than the specified current at the stated specification (100 μA at 7V for LS).

INPUT CURRENT LOW LEVEL (I_{IL})

One input at a time is tested with the other inputs tied to a solid "1" value. V_{CC} is set to the maximum value and the V_{IL} value is forced. I_{IL} is then measured.

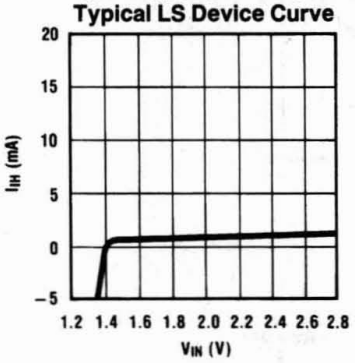
$$I_{IL} = \frac{[V_{CC} - (V_{IL} + V_{BE})]}{R1} \quad \text{Standard Inputs}$$

$$I_{IL} = \frac{[V_{CC} - (V_{IL} + V_{SH})]}{R1} \quad \text{Diode Inputs}$$

$$I_{IL} = \frac{[V_{CC} - (V_{IL} + V_{BE})]}{R1 \times \beta} \quad \text{PNP Inputs}$$

I_{IL} is intended to measure the value of the base pull-up resistor on the input, and to guarantee the maximum input load an IC presents.

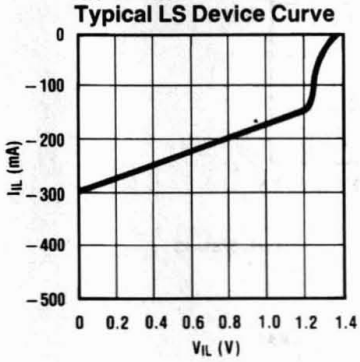
I_{IN} vs V_{IN} (High State)
Typical LS Device Curve



I_{IH} 20 μA V_{IH} 2.7V

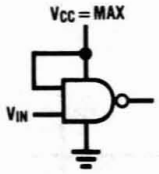
TL/F/6731–7

I_{IN} vs V_{IN} (Low State)
Typical LS Device Curve

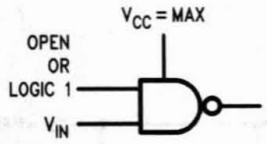


I_{IL} −400 μA V_{IL} 0.40V

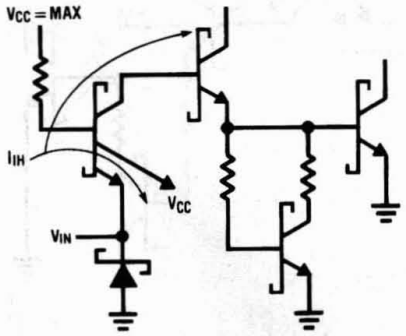
TL/F/6731–8



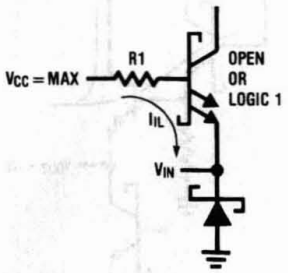
TL/F/6731–9



TL/F/6731–10



TL/F/6731–11

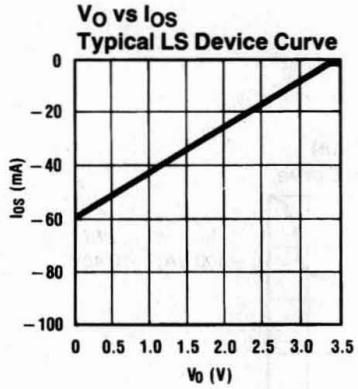


TL/F/6731–12

OUTPUT SHORT CIRCUIT CURRENT (I_{OS})

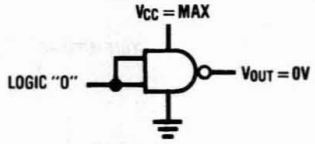
I_{OS} is measured with $V_{CC(max)}$ and the 0V forced on the output while it is in the high state. The resultant current is measured. The purpose of this is to check the I_{OS} resistor that forms the Darlington's collector pull-up. This parameter is important as it reflects both the maximum current the device will draw and the maximum drive it will provide when it is switching from low to high.

Caution must be taken when measuring TTL, LS and S outputs as the power dissipated on the die will be substantial. I_{OS} shorts should not be maintained in excess of one second or damage to the device may result.



	Min	Max
I_{OS}	−20	−100

TL/F/6731–13



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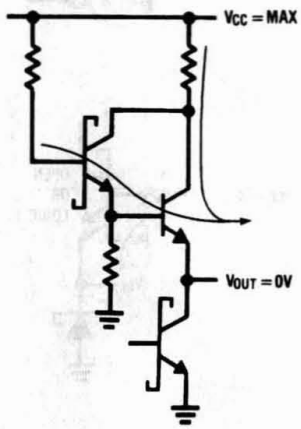

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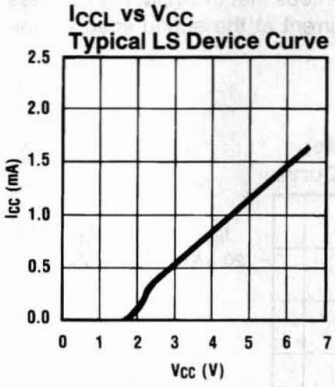
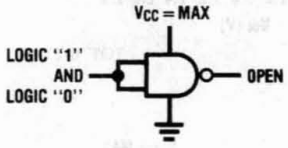
SUPPLY CURRENT HIGH LEVEL (I_{CCH}) AND SUPPLY CURRENT LOW LEVEL (I_{CCL})

Both I_{CCH} and I_{CCL} are tested using the V_{CC} maximum value. The inputs are set to the values necessary to achieve the output in the desired state. All outputs are left open, neither sourcing nor sinking current. The goal of this test is to guarantee the maximum quiescent operating power that the device will draw.

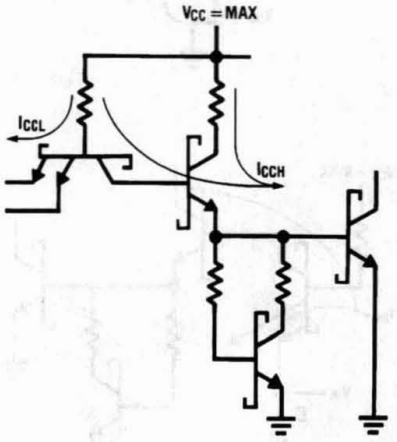


I_{CC}	Volts
1.6 mA	5.25V

TL/F/6731–14



TL/F/6731–16



TL/F/6731–18

INPUT CLAMP VOLTAGE (V_{IC} OR V_{IK})

$V_{CLAMP}(V_{IK})$ is measured with all but one input tied high and the I_{IK} current forced on the remaining input. V_{CC} is set to the minimum and the V_{IK} voltage is measured.

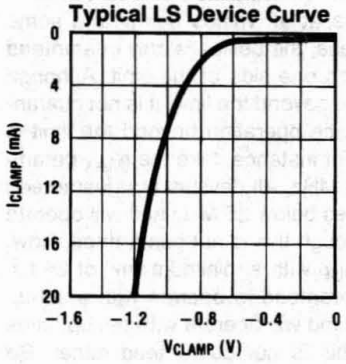
OUTPUT TRI-STATE CURRENT HIGH LEVEL (I_{OZH}) AND OUTPUT TRI-STATE CURRENT LOW LEVEL (I_{OZL})

TRI-STATE® I_{SINK} and I_{SOURCE} are measured with the output control input tied to the appropriate threshold value (usually V_{IL} = 0.8V) and with $V_{CC(max)}$. This is to insure that the output will have the greatest drive capability and the TRI-STATE control can effectively "turn off" the output under these conditions.

TRI-STATE I_{SINK}: Output is set in the high state and then TRI-STATE mode. V_{OZL} = 0.4V is then applied. The current drawn out of the device is then measured.

TRI-STATE I_{SOURCE}: Output is set in the low state and then TRI-STATE mode. V_{OZH} = 2.7V is then applied. The current drawn into the device is then measured.

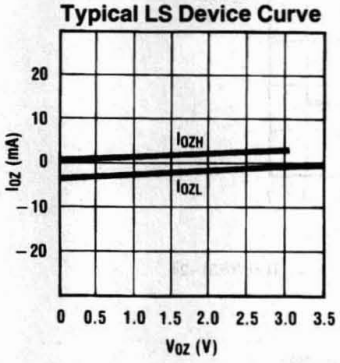
V_{CLAMP} vs I_{CLAMP}
Typical LS Device Curve



I_{CLAMP}	V_{CLAMP}
−18 mA	−1.5V

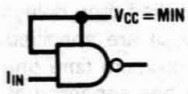
TL/F/6731–19

I_{OZH} vs V_{OZH}
(TRI-STATE I_{SOURCE}),
I_{OZL} vs V_{OZL}
(TRI-STATE I_{SINK})
Typical LS Device Curve



	I_{OZ}	V_{OZ}
I_{OZL}	−20 μA	0.4V
I_{OZH}	20 μA	2.7V

TL/F/6731–20



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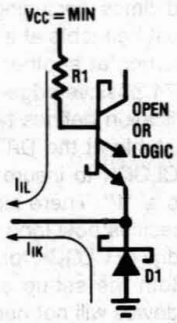
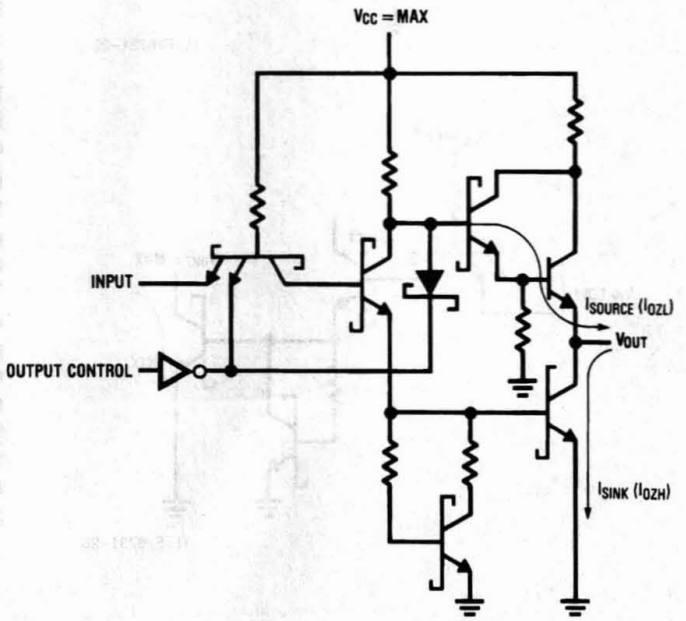


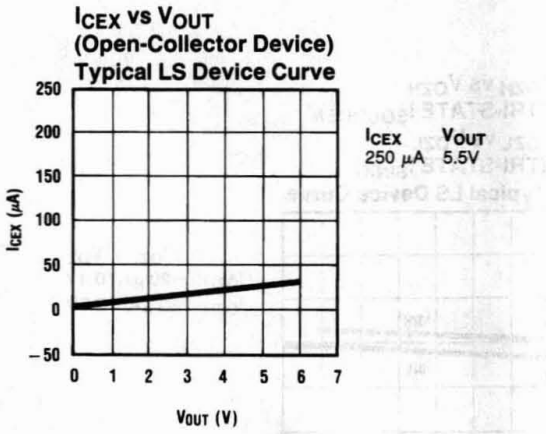
TL/F/6731–22



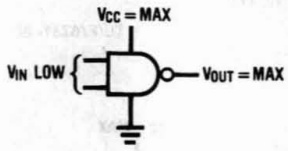
TL/F/6731–23

HIGH LEVEL OUTPUT CURRENT (OPEN-COLLECTOR DEVICES ONLY)

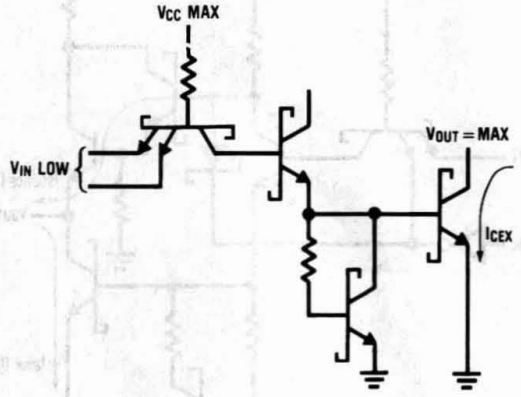
I_{CEX} is tested with the output in the high state. V_{CC} is set to 5.0V and the specified voltage (5.5V for LS) is applied to the output. The inputs are at the threshold values (0.8V and 2.0V, depending upon the logic to put output in the high state) and the resulting I_{CEX} leakage current is measured.



TL/F/6731–24



TL/F/6731–25



TL/F/6731–26

AC SWITCHING CHARACTERISTICS

The AC switching characteristics are generally measured in units of time (commonly in nanoseconds), and define how long it takes for the signal to propagate from the input to the output. The definitions used in determining the pass/fail status of each limit are not the same for AC as they are for DC. The distinction lies in the fact that for DC operation there exists one characteristic V-I curve on which the device must operate. Devices are good if they operate on the correct side of the limit, and bad if they operate on the wrong side of the limit. When dealing with certain AC parameters (f_{MAX}, $t_{SET\text{-}UP}$, t_{HOLD}, $t_{RELEASE}$, t_{PW}), the device can, and usually does, operate on both sides of the databook limit. The limit really implies a boundary that all devices are guaranteed to exceed. Depending upon the parameter, the device will either operate at all values above and some below the limit, or it will operate at all values below and some above the limit. In each case, the device is only guaranteed to operate for all values on one side of the limit. Although the device will also operate beyond the limit, it is not guaranteed to. Furthermore, device operation beyond the limit is not considered a failure. For instance, take the f_{MAX} parameter with a min limit of 25 MHz. All devices are guaranteed to operate at all frequencies below 25 MHz and will operate in excess of 25 MHz, although this is not guaranteed. Now, take the example of $t_{SET\text{-}UP}$ with a minimum limit of 25 ns. All of the devices are guaranteed to operate with a set-up time of 25 ns and longer, and will operate with set-up times below 25 ns, although this is not guaranteed either. Be aware that both of these specifications are listed in the minimum column in the databook, but the interpretation of what is failing differs significantly.

Propagation delays (called prop delays and denoted by the symbols t_{PHL} and t_{PLH}) are specified as maximum limits, and guarantee the maximum time one must wait to insure that the correct data has appeared at the device's output. Each propagation delay is specified from one input to one output only.

Input set-up and hold times (including $t_{RELEASE}$) specify how long one input must be stable at a particular logic level prior to an action occurring at another input. For example, take the DM54/74LS74 positive-edge-triggered D flip-flop. The "set-up 1" specification defines how long a logic "1" must be present *and* stable at the DATA input prior to the positive edge of the CLOCK to insure that the device will recognize that data as a "1". There also exists a "hold 1" specification which specifies how long a logic "1" must be held after the active edge of CLOCK for the device to recognize that logic "1". Both the set-up and hold times must always be met or the device will not necessarily bring in the proper data. Set-up times are generally positive, while hold

times may be either positive or negative, usually negative. The meaning of a negative hold time is that the data may be removed from the input prior to the active edge of CLOCK, and the CLOCK will still bring in the desired data. Set-up and hold times are specified as minimum values, since this defines the minimum time data must be stable prior to any change at the CLOCK input. Removing the data sooner than the minimum time may cause improper action on the part of the device.

$t_{RELEASE}$ is specified on devices where there is an input that must be set inactive prior to the active edge of CLOCK. Such inputs are usually overriding inputs like CLEAR and PRESET. With CLEAR active, it will prevent the device from switching on the CLOCK signal. $t_{RELEASE}$ is defined as the time it takes for the CLEAR input to "release" the device for clocking action, and is specified as a minimum. This represents the maximum delay required between CLEAR going inactive and the active edge of CLOCK to insure proper device operation.

All devices that have a CLOCK input also have a specification that defines the maximum speed that the CLOCK can be driven, called f_{MAX}. This specification is defined as a minimum specification and states that all of the devices will be able to operate at frequencies up to 25 MHz. For the DM54/74LS74 with an f_{MAX} of 25 MHz, all of the devices are guaranteed to operate at all clock frequencies, up to and including 25 MHz. Although no devices are guaranteed to operate above f_{MAX} (only below it), most devices will operate beyond the maximum specification. The minimum limit does *not* state that the device will not operate below f_{MAX} or that any devices that do are bad, but rather that all the devices will operate up to the limit.

Table IV shows the direction of the tighter testing for the more common AC parameters. All prop dealys (those AC parameters that have the symbols t_{PLH} or t_{PHL}) have simple min/max limits. The device is guaranteed to operate within the bounds of the min/max limits, and any operation outside these limits denotes a device failure. $t_{SET\text{-}UP}$, t_{HOLD}, f_{MAX}, and $t_{RELEASE}$ parameters have limits that denote guaranteed operation boundaries (i.e., the device is guaranteed to operate up to the boundary) but no guarantee is made concerning the device operation (or lack of it) beyond the boundary.

For detailed information on the AC waveforms, please see the test waveforms in this section.

TABLE IV. Looser/Tighter AC Test Limits Example: DM74LS74

Test	From	Looser	Nominal	Tighter	Units
$f_{max(min)}$		24	25	26	MHz
$t_{PLH(max)}$	CLR, PRE, CLK	26	25	24	ns
$t_{PHL(max)}$	CLR, PRE, CLK	31	30	29	ns
$t_{W(min)}$	CLOCK HIGH	21	20	19	ns
$t_{W(min)}$	PRE, CLR LOW	26	25	24	ns
$t_{SET\text{-}UP(min)}$	DATA HIGH	21	20	19	ns
$t_{SET\text{-}UP(min)}$	DATA LOW	21	20	19	ns
$t_{HOLD(min)}$	All DATA	1	0	−1	ns

Designing with TTL

National Semiconductor Corp.
Application Note 363
Walt Sirovy

54/74 series TTL has been used for more than a decade with excellent results, and continues to be a standard choice for design engineers because of the wide performance range and system optimization possible from the different families available. 54/74 logic comes in 7 different speed/power families (standard TTL, LS, S, ALS, AS, and L) that allow a design engineer to select device performance to suit his needs. Understanding the differences and the general limitations of all these families will go a long way toward insuring that a system will operate as intended with the minimum of corrections and redesigning.

FAMILY COMPATIBILITY: Intermixing Logic Types in One Design

Family interchangeability is a beneficial characteristic of the different TTL families and provides the designer with the ability to customize specific areas of his design in order to accomplish the task of achieving both high performance and the lowest power consumption possible. However, interchangeability is not simply a matter of replacing, say, an S00 for an LS00 to improve the speed and replacing an LS00 for an S00 for power savings. One must also look at the DC and AC characteristics to insure that the replacement device will be compatible with the existing circuit. The DC problems include input loading and compatible output drive capabilities. The AC problems include insuring that the new device speeds will be acceptable to the rest of the system. The different logic families also generate different amounts of noise and have different noise immunity. Finally, measure points for the AC parameters of the different families, although very similar, do vary some, and this will require attention.

SUPPLY RAILS: Why Not to Exceed the Specs

All bipolar logic (both junction and oxide isolated) is made up of selectively located regions of differently doped materials that form transistors, resistors, and diodes. Because of this, certain overall requirements are necessary to insure that the IC will be able to perform its task without interference from its environment. The first characteristic of bipolar devices is that the two power rails (V_{CC} and ground) represent the two voltage extremes that should be used in any system. Certain exceptions exist, primarily inputs and open-collector outputs that are pulled up to higher voltages than V_{CC}. However, while it is occasionally permissible to exceed the V_{CC} specification, it is never permissible to drive any input or output more than 0.5V below the ground reference. This limitation is due to the method used to electrically isolate the many circuit elements that are present on a bipolar IC. Oxide isolated devices use an oxide layer surrounding the various transistor and resistor tanks to provide an insulating barrier, while the original junction isolated devices use reverse biased PN junctions to provide that barrier. In both cases, the circuit is built on a P-type substrate that uses reverse biased PN junctions to separate the different circuit elements. The ground pin is electrically connected to the substrate and must be the most negative voltage on the device. When an input or output pin is taken below ground, the normally reverse biased isolation regions between the elements become forward biased and electrically connect these elements together, thus eliminating the integrity of the circuit. This may or may not result in actual damage to the device depending upon the magnitude of the violating signal and the specifics of the device being violated. This holds true for both junction and oxide isolated logic. Oxide isolated logic may provide more margin before failing (thereby "working" in some marginal designs), but it is nevertheless subject to the same kind of limitations as junction isolated logic.

IMPROPER GROUNDING: Noise Immunity, Floating Grounds

Bipolar logic uses the ground rail as the signal reference. Consequently, any modulation on the ground line will be directly added to the signal voltage. The logic "0" input noise margin is guaranteed as the difference between the V_{OL} and V_{IL} specification, and the logical "1" input noise margin is guaranteed as the difference between the V_{OH} and V_{IH} specification. This noise margin is intended to be protection against a reasonable amount of noise present. Insufficient grounding techniques can cause significant I_R and I_L drops on the ground line between two ICs and result in a "floating" ground line. This is due to the large currents that are present on ground and V_{CC} during high speed switching and means that the two devices are not using the same reference point. Any voltage drop in the ground line is added to the signal and ends up consuming some of the noise margin. Eventually, the mismatch caused by the floating ground will exceed the total noise margin and cause erroneous data to propagate through the system. The solutions to this problem are many and varied, but all of them revolve around improving the system grounding and include such ideas as providing separate signal and power grounds.

V_{CC} NOISE AND DECOUPLING: Providing Clean Power

The V_{CC} power rail is also susceptible to both I_R and I_L voltage drops. The problems that arise from the V_{CC} line are not the same as the problems that arise from the ground line. Since the V_{OH} level tracks the V_{CC} almost exactly, any voltage loss on the V_{CC} line is directly transferred to the V_{OH} level. However, the noise margin for the logic high state is typically 700 mV for commercial and 500 mV for military product, versus 400 mV and 300 mV for commercial and military product, respectively, for the logic low level. The main consequences of a drooping V_{CC} line now become I_{OL}/I_{OH} drive capability, and the AC performance in critical applications. Although bipolar devices are only guaranteed to operate over a given V_{CC} range (5V $\pm$ 10%), these devices typically function to V_{CC} values as low as 4V. Be aware that if the device does indeed function down to 4V, the AC and DC characteristics will be compromised, some quite severely.

Designing in a good power distribution system will insure that all the devices in the circuit will perform the same, regardless of their physical location. Properly decoupling the V_{CC} against both high and low frequency noise will help eliminate any problems with individual device operation. High frequency noise (100 MHz and above) comes primarily from two sources, while low frequency noise (less than 25 MHz) results from primarily one source.

SOURCES OF HIGH FREQUENCY NOISE ON THE V_{CC} LINE

1) High frequency noise results from the device rapidly switching logic levels. The bulk of the switching current from a low to high transitions shows up in I_{CC} current surges, while the bulk of the switching current from a high to low transition shows up in ground current surges.

2) Noise is transmitted through the changing magnetic fields that result from the changing electric fields in a switching line and are picked up on adjacent signal paths.

Note that the frequency causing the noise is not the signal's frequency, but the frequency of the signal's slew rate. For instance, in an S00 that is switching 0V to 3V at 1 MHz, the slew rate of the output is typically about 1 ns/V, which is a frequency of around 160 MHz. The faster the slew rate, the higher the frequency, until one has an ideal square wave with infinite frequency. It is this frequency component that gives rise to the strong magnetic fields associated with switching bipolar devices.

SOURCES OF LOW FREQUENCY NOISE ON THE V_{CC} LINE

1) Low frequency noise results from the change in the I_{CC} current demand as devices change state. For instance, gates, flip-flops, and registers will draw different I_{CC} currents, depending upon the state of the outputs.

The most commonly used method for countering these noise problems is to decouple the V_{CC} line. With this approach, capacitors are used to stabilize the V_{CC} line and filter out the unwanted frequency components. A small value capacitor (i.e., 0.1 μF) is used near the device to insure that the transient currents arising from device switching and magnetic coupling are minimized. A large value capacitor (i.e., 50 μF to 100 μF) is used on the board in general to accommodate the continually changing I_{CC} requirements of the total V_{CC} bus line. The following table shows a rough "rule of thumb" approach to determining how many capacitors to use for a given number if ICs. Be aware that the table is not a hard and fast rule, and that you must always evaluate your particular application to insure that there is sufficient V_{CC} decoupling. When using these guidelines, be sure that the devices are located near each other and near the capacitor. If the capacitor is too far away, I_R and I_L drops will diminish the capacitor's effect. All capacitors (especially the 0.01 μFs) must be high frequency RF capacitors. Disk ceramics are acceptable for this application. Keep in mind that, in synchronous systems, since a majority of the devices will be switching at once, alter your power distribution system accordingly.

Device Family	Number of Capacitors
AS, S, ALS, LS, H	1 Cap per 1 device
TTL, L	1 Cap per 2 devices

TYING ALL UNUSED INPUTS TO A SOLID LOGIC LEVEL

Unused inputs on TTL devices float at threshold, anywhere from 1.1V to 1.5V, depending upon the device and its family. While this usually simulates a "high", many application problems can be traced to open inputs. Inputs floating at threshold are very susceptible to induced noise (transmitted from other lines) and can easily switch the state of the device. A good design rule is to tie unused inputs to a solid logic level. Inputs are usually tied to V_{CC} through a 1 kΩ to 5 kΩ resistor, since tying them to ground means supplying the I_{IL} current instead of the I_{IH} current. I_{IL} is several orders of magnitude greater than I_{IH}. The resistor is recommended to protect the input against V_{CC} voltage surges and to protect the system against the possibility of the input shorting directly to ground. A single 1k resistor can handle up to 10 inputs.

TERMINATIONS: Why Terminate a Transmission Line?

Whenever signals change voltage levels, a wavefront is created that propagates according to the characteristics of the transmission line being used. If the overall length of the signal path is short compared with the signal's wavelength (1/frequency), then none of the complications of transmission lines are present. However, if the length of the signal path is long in comparison, then the wavefront will be significantly affected by the geometry and composition of that transmission line.

Fortunately, when dealing with a single board layout, the distances are usually short enough that one need not worry about the difficulties of terminating or impedance matching the line. However, if one is driving between boards or over long distances, he must be aware of the characteristics involved. When dealing with transmission lines it is necessary to know the impedance of the line. Every time the signal wavefront encounters a discontinuity (a point where the impedance changes, whether from a branch, junction or because of a change of environment), the opportunity for reflections and standing waves is present. These waves can easily cause the loss of the signal's integrity, having the ability to build voltages that are large enough to destroy an IC. Proper line termination will insure that the signal propagates down the line and is totally absorbed at the receiving end, thus preventing these waves from occurring.

Listed below is a guideline to the types of transmission lines to use when sending signals over various distances.

0″ to 12″ Single wire conductor OK. Use point-to-point routing and avoid parallel routing if possible. Ground plane recommended, but not mandatory. Space conductors as far apart as possible to reduce line to line capacitance.

12″ to 6′ Dense ground plane required with wire routed as closely as possible. Twisted-pair lines or coaxial cable mandatory for clock lines and recommended for all sensitive control lines.

Over 6′ Use fully terminated transmission lines. Avoid the use of radially distributed lines and avoid sharp bends in the line. Be aware that transmission lines have complex impedances and are not simply resistive in nature.

BUS DRIVERS: On Board vs Off Board

Many of the TRI-STATE® buffers and flip-flops are intended to connect directly to the system bus and must be able to drive heavily capacitive loads. Keeping this in mind, all of National's LS TRI-STATE devices have "triple-sink" capability; that is, the I_{OL} and I_{OH} drive currents have been tripled. However, these devices are intended to drive single board buses. Driving off the board with these devices can easily lead to serious problems.

When using standard logic bus drivers on a single board, be aware that many of the octal and bus oriented devices have PNP inputs to reduce DC loading. PNP inputs on 54S/74S devices tend to be more capacitive than the corresponding diode or emitter inputs, and as such, compromise the AC loading of the bus. Careful attention must be given to both DC and AC loading when driving heavily loaded buses. PNP

inputs on LS/AS/ALS operate at significantly lower currents and do not significantly increase capacitive load.

It is strongly recommended that any time a bus line leaves a board, interface bus drivers be used. These devices (see National's 1986 Interface/Databook) are specifically designed to impedance match different kinds of transmission lines and have the necessary current drive to handle the job. Using an ordinary logic device will usually yield poor results. If one must drive a transmission line with a logic device, there are some guidelines that should be followed to minimize the problems that can result.

1) Take care to properly terminate the bus. Be aware that every time a signal passes through a different impedance, an interface is created and that any impedance mismatch will result in reflections.

2) Never drive off the board with a bistable element like a flip-flop or a latch. This is because those devices are very susceptible to reflected waves changing their state. By buffering the output of the latch with another device, the reflected wave can affect the output of the buffer, but not the latch. This means that when the wave finally dies out, the latch will still have the proper data and the buffer will "snap back" to the proper output.

3) Be sure to carry an adequate ground plan with the signals and to shield the bus. Carrying a good ground plan (use multiple ground lines spaced around the connector if possible) will reduce the problem of floating ground, and the shielding will help protect the signal lines for induced noise. Using twisted-pair transmission lines for critical signals helps to eliminate the capacitive coupling that can degrade signals, or even cause false signals.

4) It is best to buffer any clock or control lines that depend upon fast, clean switching. Buffering at both the sending and receiving end will go a long way toward insuring that the clock can accomplish its goals.

5) Use the devices with Schmitt inputs to add to the noise margin of the receiving device. This will help increase the noise rejection of the system. Decouple each receiver separately, connecting the capacitor directly between ground and V_{CC}. Make sure that the device ground is tied directly to the bus ground.

6) If using open-collector devices to drive the bus, add a pull-up resistor on the input to the receiving device if the I_{OL} current of the driving device can handle it. A resistance in the 300Ω range will significantly improve the signal's rise time.

AC LOADING: What Do AC Loads Look Like, and Why?

The standard AC load for all of the logic families, except ALS and AS, is built around a diode chain to ground and a pull-up resistor to V_{CC} with added capacitance. This load is designed to look like the standard logic circuit input structure, and to simulate the appearance of switching in an actual application. For ALS and AS, the load is built around a resistor to ground and added capacitance. This is primarily for the requirements of high speed device testing. There also exists a set of standardized military AC loads that were designed to approximate the input structure, while using no switches for the TRI-STATE parameters. Please see waveforms in this section. In the final analysis of these loads, it must be kept in mind that they represent a standard that can be used to determine the quality of an IC. No load will be able to predict exactly how a device will perform in a circuit or the speeds that a device can achieve in a good test jig with the spec load, as compared to the speeds that a device will produce in an application.

OPEN-COLLECTOR DEVICES: What They Are, How to Use Them

Open-collector devices are totem pole outputs where the upper output (usually a Darlington transistor) is left out of the circuit. As such, these devices have no active logic high drive and cannot be used to drive a line high. The advantage to open-collector devices is that a number of outputs can be directly tied together. If one were to tie two complete totem pole outputs together, then at some time one output would be driving high while the other output was driving low. The result is that one device will be dumping excessive current directly into the other device. The resulting power dissipation in both devices can easily degrade the lifetime of the device. Since open-collector devices only have active drive in one state, if two connected devices drive to opposite states, the low state will always predominate and there will be no degradation to either device. Open-collector specifications are obvious by the lack of a V_{OH} specification. The only V_{OH}/I_{OH} specification is the leakage limits, and these are specified at $V_{OH} = 5.5V$.

When dealing with open-collector devices, it must be noted that each output requires a resistive pull-up, usually tied to V_{CC}. (By using high voltage outputs, one can tie the resistor pull-up to a voltage higher than V_{CC}.) Designers often try to get away with tying the output to an input and relying on the I_{IL} current to pull up the output. This unwise, as it is just like leaving inputs floating: the input is very susceptible to noise and can easily give false signals. Shown below are two equations that can be used to determine the min/max range of the pull-up resistor.

$$R_{MAX} = \frac{(V_{CC(MIN)} - V_{OH})}{(N1 \bullet I_{OH} + N2 \bullet I_{IH})}$$

$$R_{MIN} = \frac{(V_{CC(MIN)} - V_{OL})}{(I_{OL} - N2 \bullet I_{IL})}$$

where: N1 = the number of open-collector devices tied together,

N2 = the number of inputs being driven on the line.

If the maximum resistance is exceeded, then it is possible for the total leakage currents from all of the inputs and outputs to pull the V_{OH} level below the spec value. Likewise, if the R_{MIN} value is exceeded, then the driving device may not be able to pull down the signal line to a solid V_{OL}. Either of these two cases can easily result in false logic levels being propagated through the system.

Designer's Encyclopedia of Bipolar One-Shots

National Semiconductor Corp.
Application Note 372
Kern Wong

INTRODUCTION

National Semiconductor manufacturers a broad variety of industrial bipolar monostable multivibrators (one-shots) in TTL and LS-TTL technologies to meet the stringent needs of systems designers for applications in the areas of pulse generation, pulse shaping, time delay, demodulation, and edge detection of waveforms. Features of the various device types include single and dual monostable parts, retriggerable and non-retriggerable devices, direct clearing input, and DC or pulse-triggered inputs. Furthermore, to provide the designer with complete flexibility in controlling the pulse width, some devices also have Schmitt trigger input, and/or contain internal timing components for added design convenience.

DESCRIPTION

One-shots are versatile devices in digital circuit design. They are actually quite easy to use and are best suited for applications to generate or to modify short timings ranging from several tens of nanoseconds to a few microseconds. However, difficulties are constantly being experienced by design and test engineers, and basically fall into the categories of either pulse width problems or triggering difficulties.

The purpose of this note is to present an overall view of what one-shots are, how they work, and how to use them properly. It is intended to give the reader comprehensive information which will serve as a designer's guide to bipolar one-shots.

Nearly all malfunctions and failures on one-shots are caused by misuse or misunderstanding of their fundamental operating rules, characteristic design equations, parameters, or more frequently by poor circuit layout, improper bypassing, and improper triggering signal.

In the following sections all bipolar one-shots manufactured by National Semiconductor are presented with features tables and design charts for comparisons. Operating rules are outlined for devices in general and for specific device types. Notes on unique differences per device and on special operating considerations are detailed. Finally, truth tables and connection diagrams are included for reference.

DEFINITION

A one-shot integrated circuit is a device that, when triggered, produces an output pulse width that is independent of the input pulse width, and can be programmed by an external Resistor-Capacitor network. The output pulse width will be a function of the RC time constant. There are various one-shots manufactured by National Semiconductor that have diverse features, although, all one-shots have the basic property of producing a programmable output pulse width. All National one-shots have True and Complementary outputs, and both positive and negative edge-triggered inputs.

OPERATING RULES

In all cases, R and C represented by the timing equations are the external resistor and capacitor, called R_{EXT} and C_{EXT}, respectively, in the data book. All the foregoing timing equations use C in pF, R in KΩ, and yield t_W in nanoseconds. For those one-shots that are not retriggerable, there is a duty cycle specification associated with them that

TTL AND LS-TTL ONE-SHOT FEATURES

Device Number	# Per IC Package	Re-trigger	Reset	Capacitor Min	Capacitor Max	Resistor Min	Resistor Max	Timing Equation* for $C_{EXT} > 1000$ pF
				in μF		in KΩ		
DM54121	One	No	No	0	1000	1.4	30	$t_W = KRC\bullet(1 + 0.7/R)$
DM74121	One	No	No	0	1000	1.4	40	$K = 0.55$
DM54LS122	One	Yes	Yes	None		5	180	$t_W = KRC$
DM74LS122	One	Yes	Yes	None		5	260	$K = 0.45$
DM54123	Two	Yes	Yes	None		5	25	$t_W = KRC\bullet(1 + 0.7/R)$
DM74123	Two	Yes	Yes	None		5	50	$K = 0.34$
DM54LS123	Two	Yes	Yes	None		5	180	$t_W = KRC$
DM74LS123	Two	Yes	Yes	None		5	260	$K = 0.45$
DM54LS221	Two	No	Yes	0	1000	1.4	70	$t_W = KRC$
DM74LS221	Two	No	Yes	0	1000	1.4	100	$K = 0.7$
DM8601	One	Yes	No	None		5	25	$t_W = KRC\bullet(1 + 0.7/R)$
DM9601	One	Yes	No	None		5	50	$K = 0.32$
DM8602	Two	Yes	Yes	None		5	25	$t_W = KRC\bullet(1 + 1/R)$
DM9602	Two	Yes	Yes	None		5	50	$K = 0.31$

*The above timing equations hold for all combinations of R_{EXT} and C_{EXT} for all cases of $C_{EXT} > 1000$ pF within specified limits on the R_{EXT} and C_{EXT}.

defines the maximum trigger frequency as a function of the external resistor, R_{EXT}.

In all cases, an external (or internal) timing resistor (R_{EXT}) connects from V_{CC} or another voltage source to the "R_{EXT}/C_{EXT}" pin, and an external timing capacitor (C_{EXT}) connects between the "R_{EXT}/C_{EXT}", and "C_{EXT}" pins are required for proper operation. There are no other elements needed to program the output pulse width, though the value of the timing capacitor may vary from 0.0 to any necessary value.

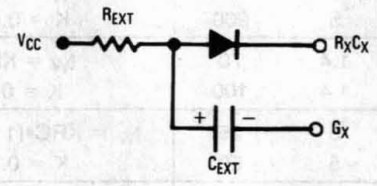
When connecting the R_{EXT} and C_{EXT} timing elements, care must be taken to put these components absolutely as close to the device pins as possible, electrically and physically. Any distance between the timing components and the device will cause time-out errors in the resulting pulse width, because the series impedance (both resistive and inductive) will result in a voltage difference between the capacitor and the one-shot. Since the one-shot is designed to discharge the capacitor to a specific fixed voltage, the series voltage will "fool" the one-shot into releasing the capacitor before the capacitor is fully discharged. This will result in a pulse width that appears much shorter than the programmed value. We have encountered users who have been frustrated by pulse width problems and had difficulty to perform correlations with commercial test equipment. The nature of such problems are usually related to the improper layout of the DUT adapter boards. (See *Figure 6* for a PC layout of an AC test adapter board.) It has been demonstrated that lead length greater than 3 cm from the timing component to the device pins can cause pulse width problems on some devices.

For precise timing, precision resistors with good temperature coefficient should be used. Similarly, the timing capacitor must have low leakage, good dielectric absorption characteristics, and a low temperature coefficient for stability. Please consult manufacturers to obtain the proper type of component for the application.

For small time constants, high-grade mica glass, polystyrene, polypropylene, or polycarbonate capacitor may be used. For large time constants, use a solid tantalum or special aluminum capacitor.

In general, if a small timing capacitor is used that has leakage approaching 100 nA or if the stray capacitance from either terminal to ground is greater than 50 pF, then the timing equations or design curves which predict the pulse width would not represent the programmed pulse width which the device generates.

When an electrolytic capacitor is used for C_{EXT}, a switching diode is often suggested for standard TTL one-shots to prevent high inverse leakage current *(Figure 1)*. In general, this switching diode is not required for LS-TTL devices; it is also not recommended with retriggerable applications.



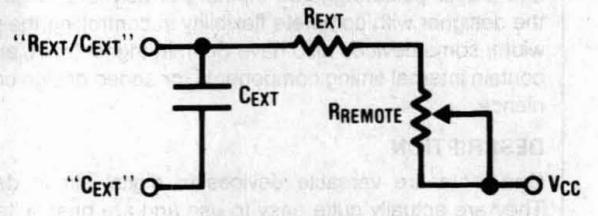
TL/F/7508–1

FIGURE 1

It is never a good practice to leave any unused inputs of a logic integrated circuit "floating". This is particularly true for one-shots. Floating uncommitted inputs or attempts to establish a logic HIGH level in this manner will result in malfunction of some devices.

Operating one-shots with values of the R_{EXT} outside the recommended limits is at the risk of the user. For some devices it will lead to complete inoperation, while for other devices it may result in either output pulse widths different from those values predicted by design charts or equations, or with modes of operation and performance quite different from known standard characterizations.

To obtain variable pulse width by remote trimmiing, the following circuit is recommended *(Figure 2)*. "R_{REMOTE}" should be placed as close to the one-shot as possible.

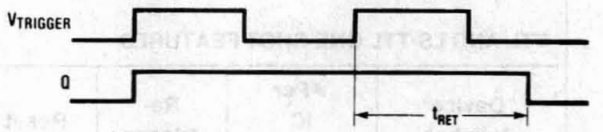


TL/F/7508–2

FIGURE 2

V_{CC} and ground wiring should conform to good high frequency standards and practices so that switching transients on the V_{CC} and ground return leads do not cause interaction between one-shots. A 0.001 μF to 0.1 μF bypass capacitor (disk or monolithic type) from the V_{CC} pin to ground is necessary on each device. Furthermore, the bypass capacitor shoud be located so as to provide as short an electrical path as possible between the V_{CC} and ground pins. In severe cases of supply-line noise, decoupling in the form of a local power supply voltage regulator is necessary.

For retriggerable devices the retrigger pulse width is calculated as follows for positive-edge triggering:



TL/F/7508–3

FIGURE 3

$$t_{RET} = t_W + t_{PLH} = K \bullet (R_{EXT})(C_{EXT}) + t_{PHL}$$

(See tables for exact expressions for K and t_W; K is unity on most HCMOS devices.)

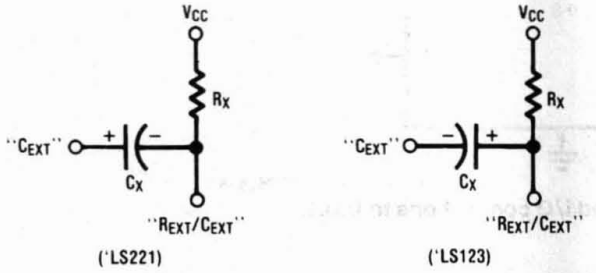
SPECIAL CONSIDERATIONS AND NOTES:

The 9601 is the single version of the dual 9602 one-shot. With the exception of an internal timing resistor, R_{INT}, the 'LS122 has performance characteristics virtually identical to the 'LS123. The design and characteristic curves for equivalent devices are not depicted individually, as they can be referenced from their parent device.

National's TTL-'123 dual retriggerable one-shot features a unique logic realization not implemented by other manufacturers. The "CLEAR" input does not trigger the device, a design tailored for applications where it is desired only to terminate or to reduce the timing pulse width.

The 'LS221, even though it has pin-outs identical to the 'LS123, is not functionally identical. It should be remembered that the 'LS221 is a non-retriggerable one-shot, while the 'LS123 is a retriggerable one. For the 'LS123 device, it is sometimes recommended to externally ground its "C_{EXT}" pin for improved system performance. The "C_{EXT}" pin on the 'LS221, however, is not an internal connection to the device ground. Hence, grounding this pin on the 'LS221 device will render the device inoperative.

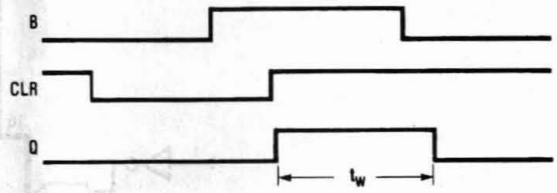
Furthermore, if a polarized timing capacitor is used on the 'LS221, the positive side of the capacitor should be connected to the "C_{EXT}" pin. For the 'LS123 part, it is the contrary, the negative terminal of the capacitor should be connected to the "C_{EXT}" pin of the device *(Figure 4)*.



TL/F/7508–4

FIGURE 4

The 'LS221 trigger on "CLEAR": This mode of trigger requires first the "B-Input" be set from a Low-to-High level while the "CLEAR" input is maintained at logic Low level. Then, with the "B" Input at logic High level, the "CLEAR" input, whose positive transition from LOW-to-HIGH will trigger an output pulse ("A input" is LOW).

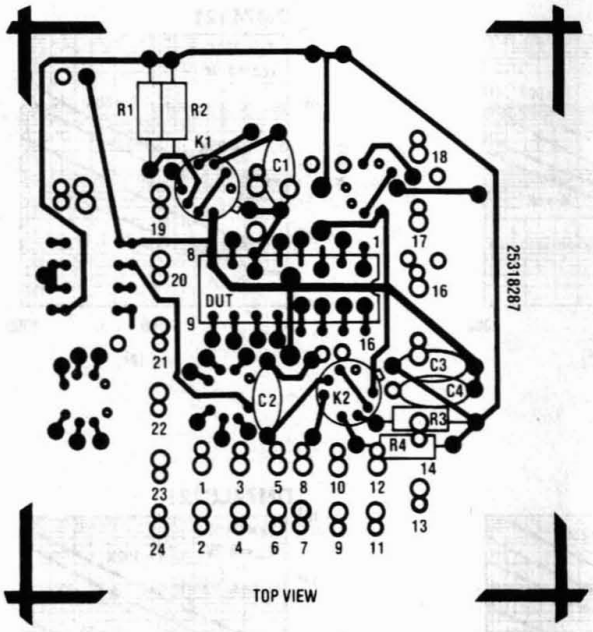


TL/F/7508–5

FIGURE 5

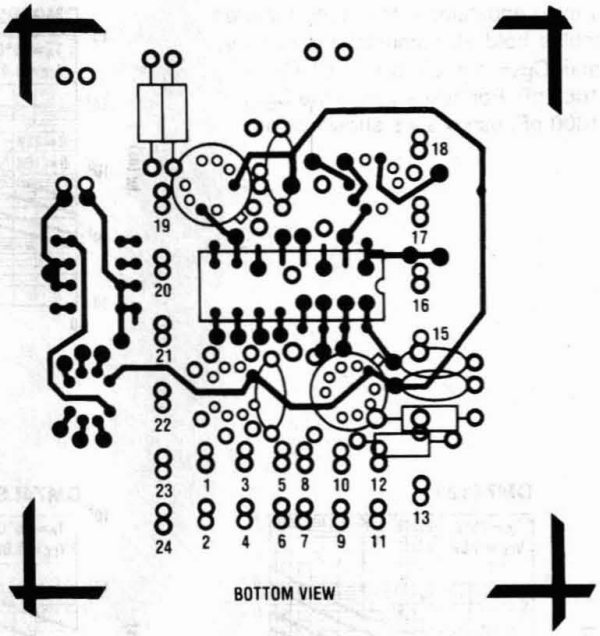
AC Test Adapter Board

The compact PC layout below is a universal one-shot test adapter board. By wiring different jumpers, it can be configured to accept all one-shots made by National Semiconductor. The configuration shown below is dedicated for the '123 device. It has been used successfully for functional and pulse width testing on all the '123 families of one-shots on the Teradyne AC test system.



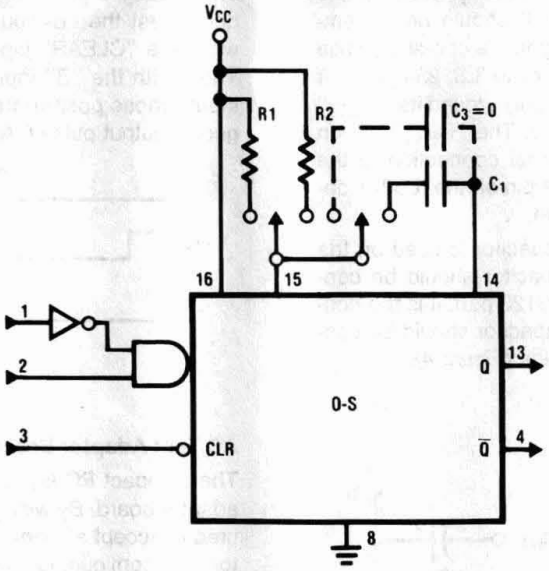
TL/F/7508–6

FIGURE 6a. AC Test Adapter



TL/F/7508–7

FIGURE 6b. AC Test Adapter

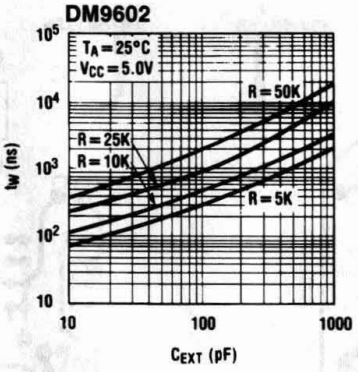


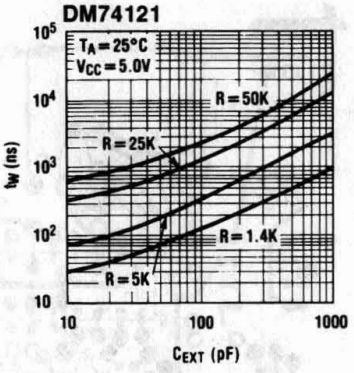
TL/F/7508–8

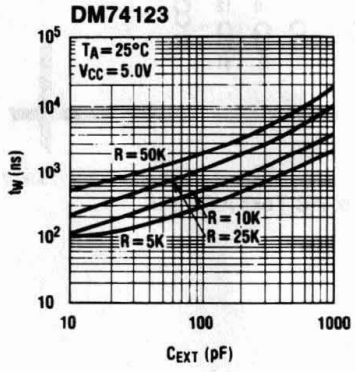
FIGURE 7a. Timing Components and I/O connections to D.U.T.

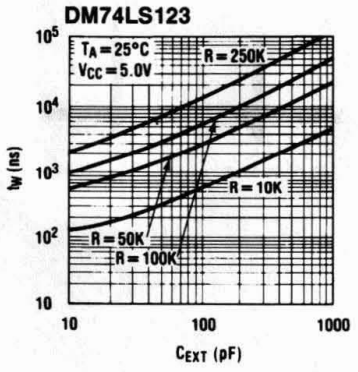
Typical Output Pulse Width vs Timing Components

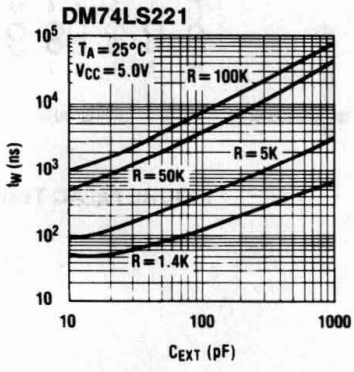
Timing equations listed in the features tables hold all combinations of R_{EXT} and C_{EXT} for all cases of C_{EXT} > 1000 pF. For cases where the C_{EXT} < 1000 pF, use graphs shown below.







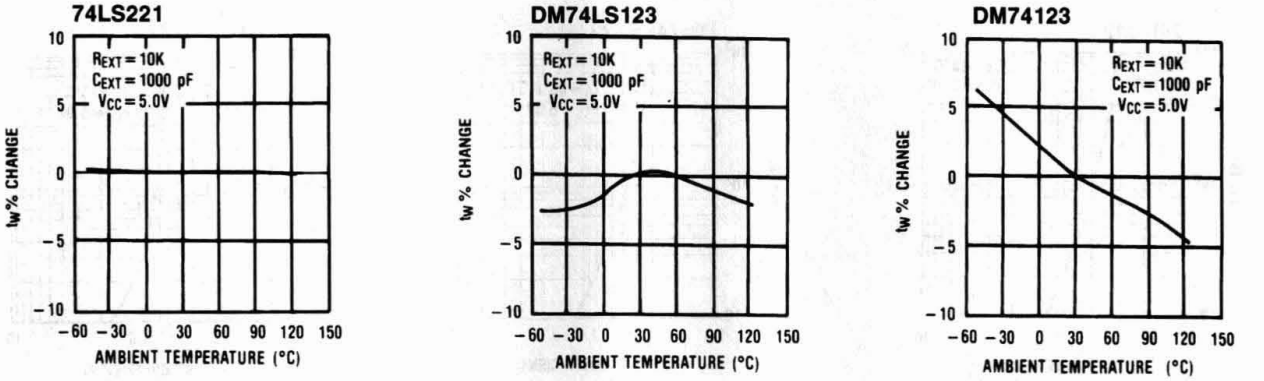




TL/F/7508–9

Typical Output Pulse Width Variation vs Ambient Temperature

The graphs shown below demonstrate the typical shift in the device output pulse widths as a function of temperature. It should be noted that these graphs represent the temperature shift of the device after being corrected for any temperature shift in the timing components. Any shift in these components will result in a corresponding shift in the pulse width, as well as any shift due to the device itself.

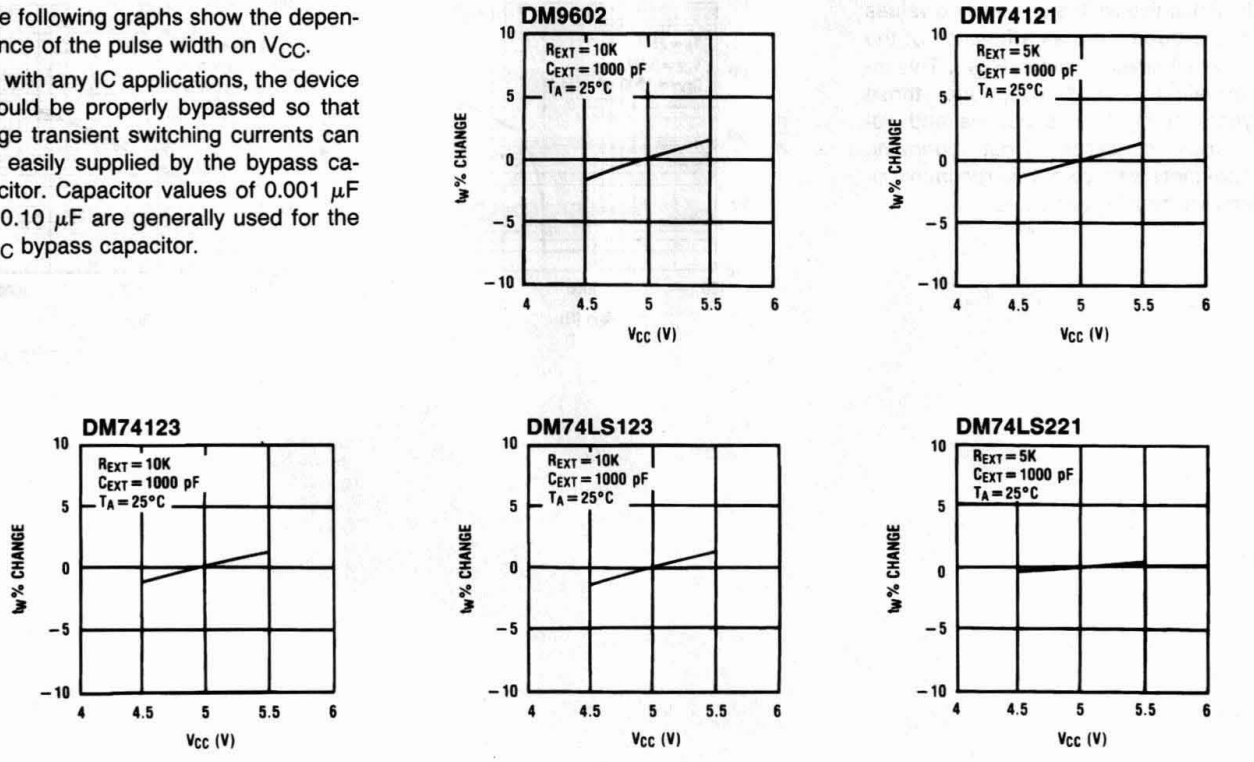


TL/F/7508–10

Typical Output Pulse Width Variation vs Supply Voltage

The following graphs show the dependence of the pulse width on V_{CC}.

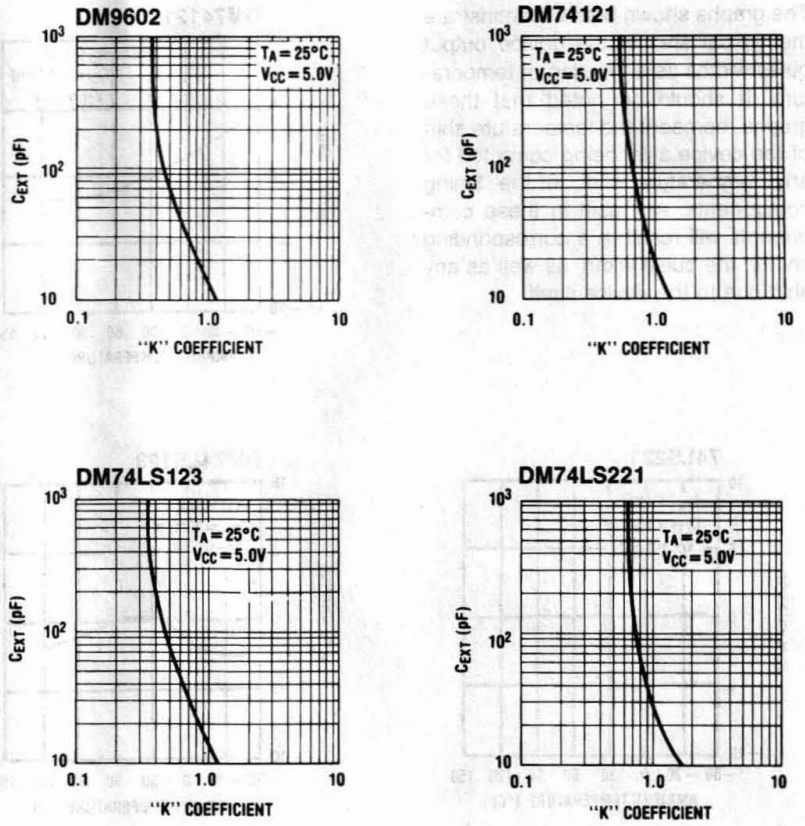
As with any IC applications, the device should be properly bypassed so that large transient switching currents can be easily supplied by the bypass capacitor. Capacitor values of 0.001 μF to 0.10 μF are generally used for the V_{CC} bypass capacitor.



TL/F/7508–11

Typical "K" Coefficient Variation vs Timing Capacitance

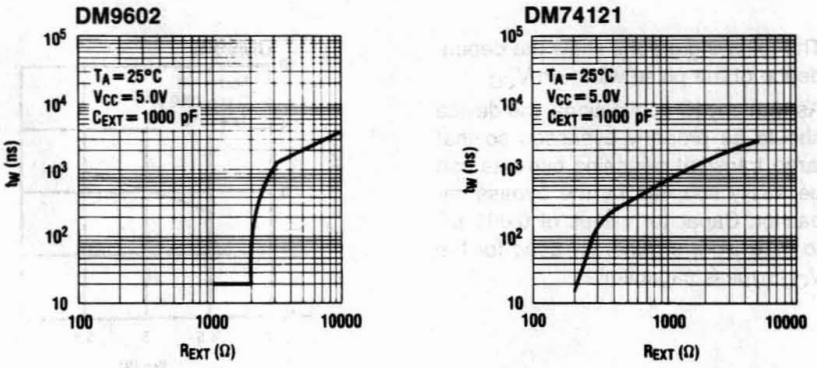
For certain one-shots, the "K" coefficient is not a constant, but varies as a function of the timing capacitor C_{EXT}. The graphs below detail this characteristic.



TL/F/7508–12

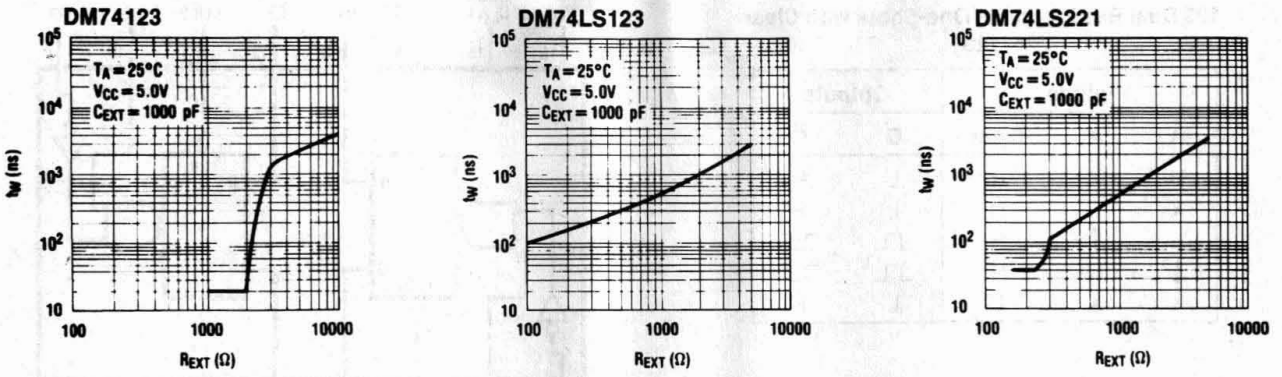
Typical Output Pulse Width vs Minimum Timing Resistance

The plots shown below demonstrate typical pulse widths and limiting values of the true output as a function of the external timing resistor, R_{EXT}. This information should evaporate those years of mysterious notions and numerous concerns about operating one-shots with lower that recommended minimum R_{EXT} values.



TL/F/7508–13

Typical Output Pulse Width vs Minimum Timing Resistance (Continued)



TL/F/7508–14

Function Tables

'121 One-Shots

Inputs			Outputs	
A1	A2	B	Q	$\overline{Q}$
L	X	H	L	H
X	L	H	L	H
X	X	L	L	H
H	H	X	L	H
H	↓	H	⎍	⎎
↓	H	H	⎍	⎎
↓	↓	H	⎍	⎎
L	X	↑	⎍	⎎
X	L	↑	⎍	⎎

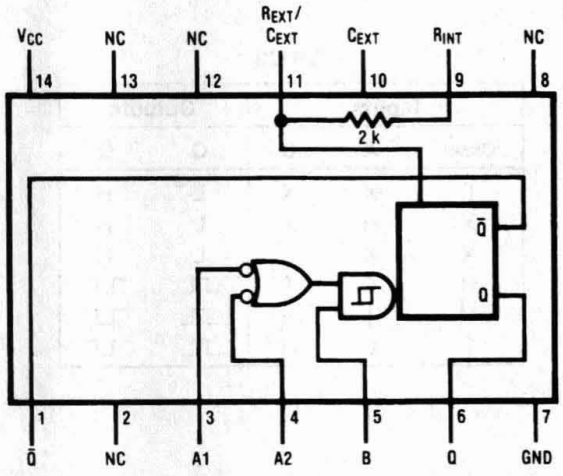
'122 Retriggerable One-Shots with Clear

Inputs					Outputs	
Clear	A1	A2	B1	B2	Q	$\overline{Q}$
L	X	X	X	X	L	H
X	H	H	X	X	L	H
X	X	X	L	X	L	H
X	X	X	X	L	L	H
X	L	X	H	H	L	H
H	L	X	↑	H	⎍	⎎
H	L	X	H	↑	⎍	⎎
H	X	L	H	H	L	H
H	X	L	↑	H	⎍	⎎
H	X	L	H	↑	⎍	⎎
H	H	↓	H	H	⎍	⎎
H	↓	↓	H	H	⎍	⎎
H	↓	H	H	H	⎍	⎎
↑	L	X	H	H	⎍	⎎
↑	X	L	H	H	⎍	⎎

H = HIGH Level
L = LOW Level
↑ = Transition from LOW-to-HIGH
↓ = Transition from HIGH-to-LOW
⎍ = One HIGH Level Pulse
⎎ = One LOW Level Pulse
X = Don't Care

Connection Diagrams

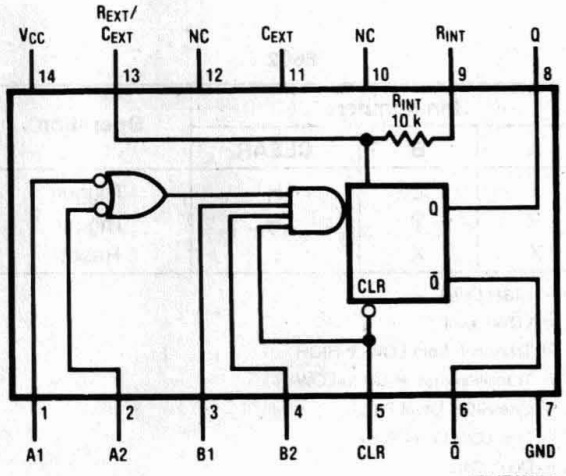
54121 (J, W); 74121 (N)



TL/F/7508–15

Top View

54LS122 (J, W); 74LS122 (N)



TL/F/7508–16

Top View

Function Tables (Continued)

'123 Dual Retriggerable One-Shots with Clear

'123

Inputs			Outputs	
A	A	Clear	Q	$\overline{Q}$
H	X	H	L	H
X	L	H	L	H
L	↑	H	⎍	⎎
↓	H	H	⎍	⎎
X	X	L	L	H

'LS123

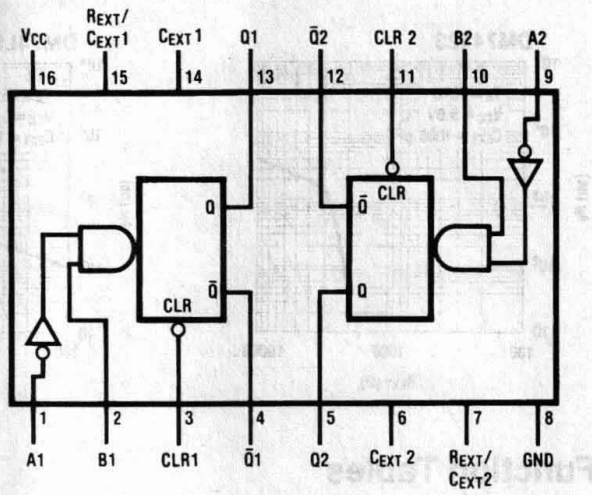
Inputs			Outputs	
Clear	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

8602

Pin Numbers			Operation
A	B	CLEAR	
↓	L	H	Trigger
H	↑	H	Trigger
X	X	L	Reset

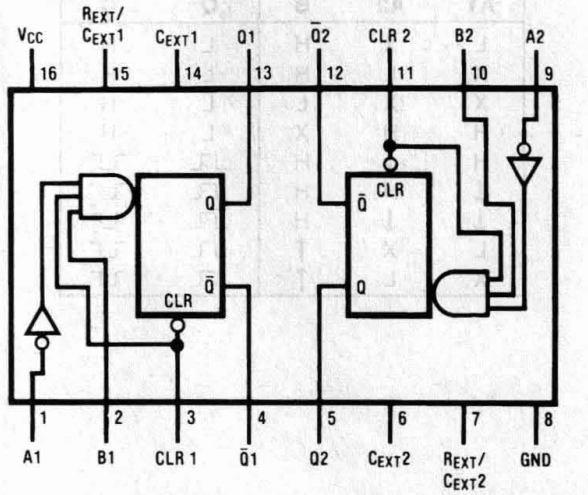
H = HIGH Level
L = LOW Level
↑ = Transition from LOW-to-HIGH
↓ = Transition from HIGH-to-LOW
⎍ = One HIGH Level Pulse
⎎ = One LOW Level Pulse
X = Don't Care

Connection Diagrams (Continued)



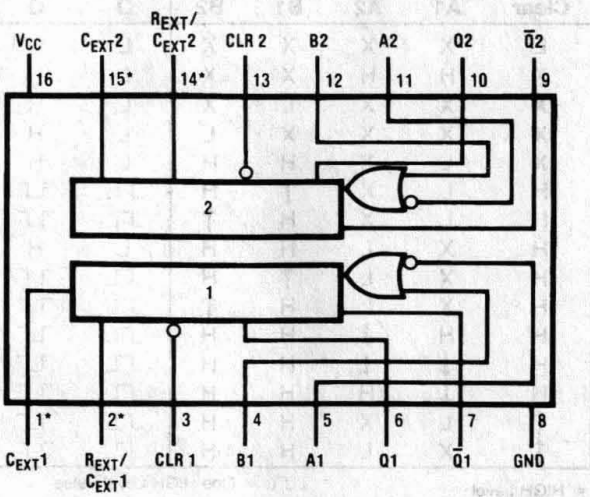
TL/F/7508–17

Top View
54LS123 (J, W); 74LS123 (N)



TL/F/7508–18

Top View
9602 (J, W); 8602 (N)



TL/F/7508–19

Top View

*Pins for external timing.

Function Tables (Continued)

'221 Dual One-Shots with Schmitt Trigger Inputs

Inputs			Outputs	
Clear	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

8601

Inputs				Outputs	
A1	A2	B1	B2	Q	$\overline{Q}$
H	H	X	X	L	H
X	X	L	X	L	H
X	X	X	L	L	H
L	X	H	H	L	H
L	X	↑	H	⎍	⎎
L	X	H	↑	⎍	⎎
X	L	H	H	L	H
X	L	↑	H	⎍	⎎
X	L	H	↑	⎍	⎎
H	↓	H	H	⎍	⎎
↓	↓	H	H	⎍	⎎
↓	H	H	H	⎍	⎎

H = HIGH Level
L = LOW Level
↑ = Transition from LOW-to-HIGH
↓ = Transition from HIGH-to-LOW
⎍ = One HIGH Level Pulse
⎎ = One LOW Level Pulse
X = Don't Care

Applications

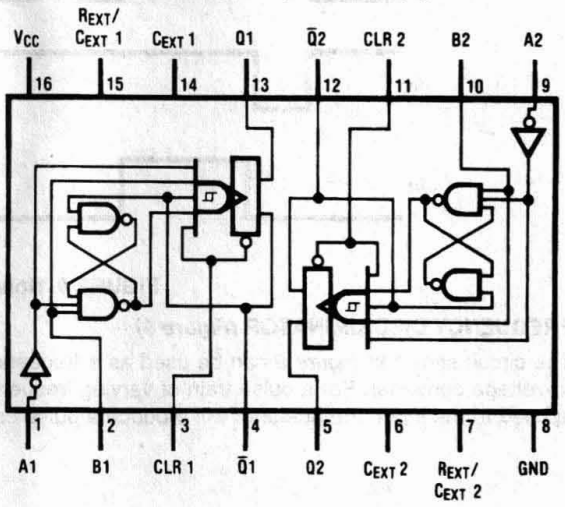
The following circuits are shown with generalized one-shot connection diagram.

NOISE DISCRIMINATOR *(Figure 8)*

The time constant of the one-shot (O-S) can be adjusted so that an input pulse width narrower than that determined by the time constant will be rejected by the circuit. Output at Q_2 will follow the desired input pulse, with the leading edge delayed by the predetermined time constant. The output pulse width is also reduced by the amount of the time constant from R_X and C_X.

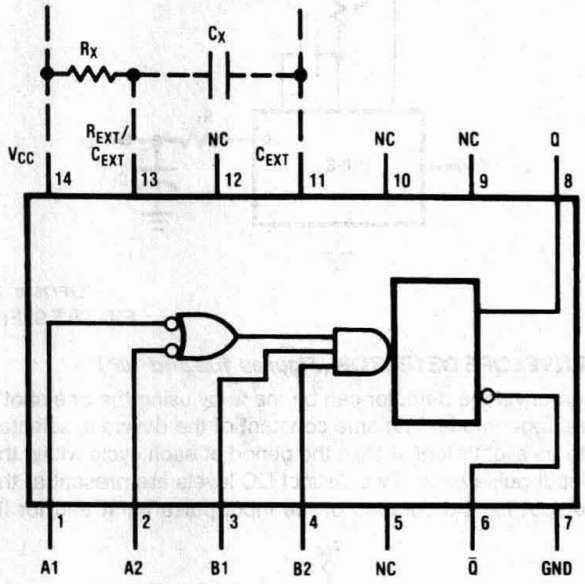
Connection Diagrams (Continued)

54LS221 (J, W); 74LS221 (N)

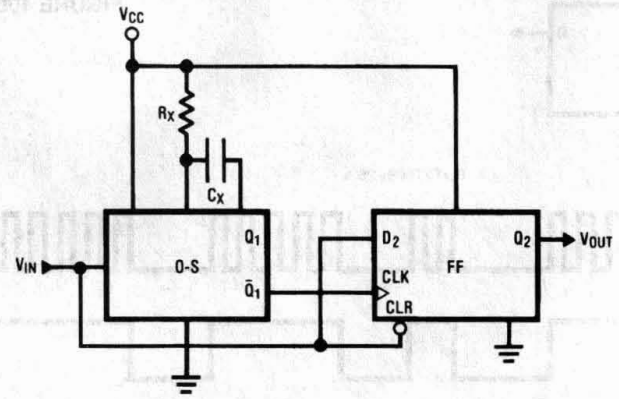


Top View TL/F/7508–20

9601 (J, W); 8601 (N)

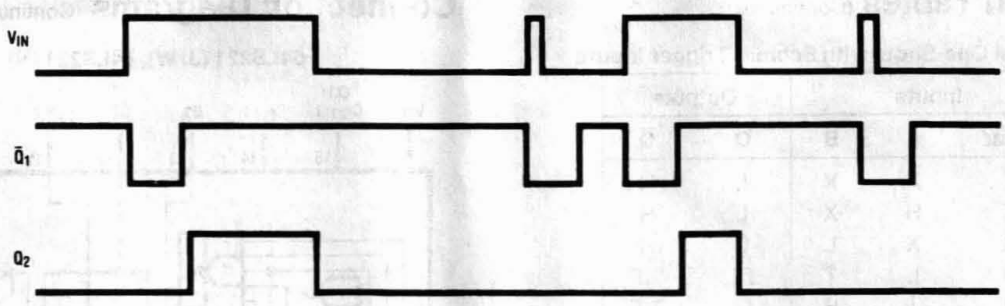


Top View TL/F/7508–21



TL/F/7508–22

FIGURE 8. Noise Discriminator

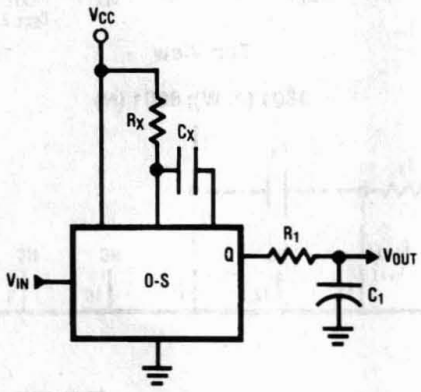


TL/F/7508–23

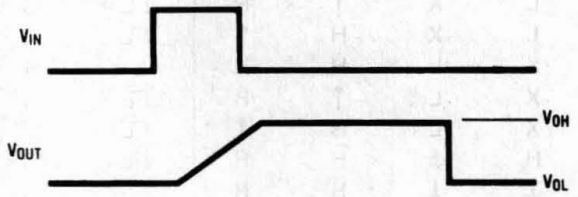
FIGURE 8. Noise Discriminator (Continued)

FREQUENCY DISCRIMINATOR ***(Figure 9)***

The circuit shown in *Figure 9* can be used as a frequency-to-voltage converter. For a pulse train of varying frequency applied to the input, the one-shot will produce a pulse constant width for each triggering transition on its input. The output pulse train is integrated by R_1 and C_1 to yield a waveform whose amplitude is proportional to the input frequency. (Retriggerable device required.)



TL/F/7508–24

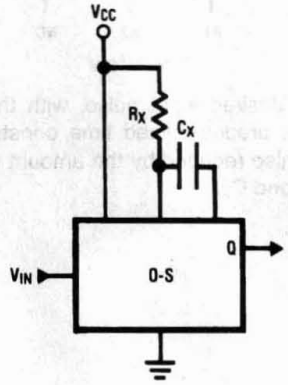


TL/F/7508–25

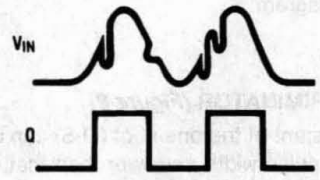
FIGURE 9. Frequency Discriminator

ENVELOPE DETECTOR ***(Figures 10a and 10b)***

An envelope detector can be made by using the one-shot's retrigger mode. The time constant of the device is selected to be slightly longer than the period of each cycle within the input pulse burst. Two distinct DC levels are present at the output for the duration of the input pulse burst and for its absence (see *Figure 10a*). The same circuit can also be employed for a specific frequency input as a Schmitt trigger to obviate input trigger problems associated with hysteresis and slow varying, noisy waveforms (see *Figure 10b*). (Retriggerable device required.)



TL/F/7508–26



TL/F/7508–27

FIGURE 10b. Schmitt Trigger

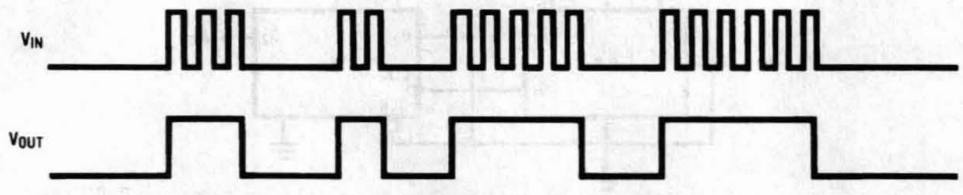


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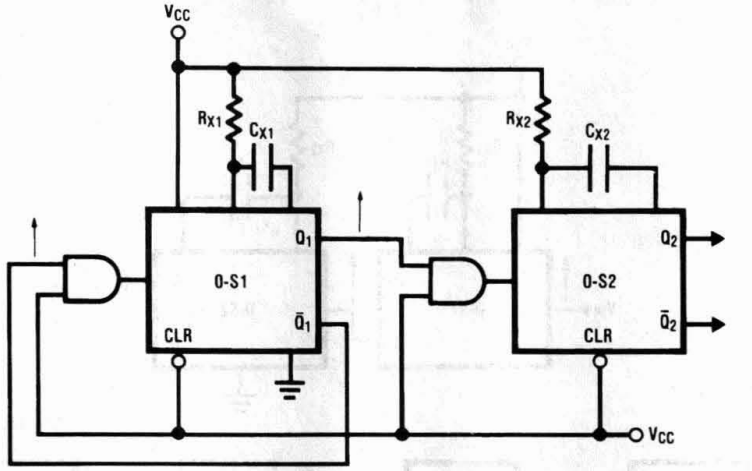
FIGURE 10a. Envelope Detector (Retriggerable Device Required)

PULSE GENERATOR *(Figure 11)*

Two one-shots can be connected together to form a pulse generator capable of variable frequency and independent duty cycle control. The R_{X1} and C_{X1} of O–S1 determine the frequency developed at output Q_1. R_{X2} and C_{X2} of O–S2 determine the output pulse width at Q_2. (Retriggerable device required.)



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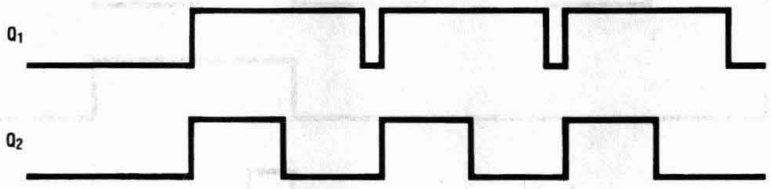

$$\text{DUTY CYCLE} = \frac{R_{X2}\,C_{X2}}{R_{X1}\,C_{X1}}$$

$$\text{FREQ} = \frac{1}{K\,R_{X1}\,C_{X1}}$$

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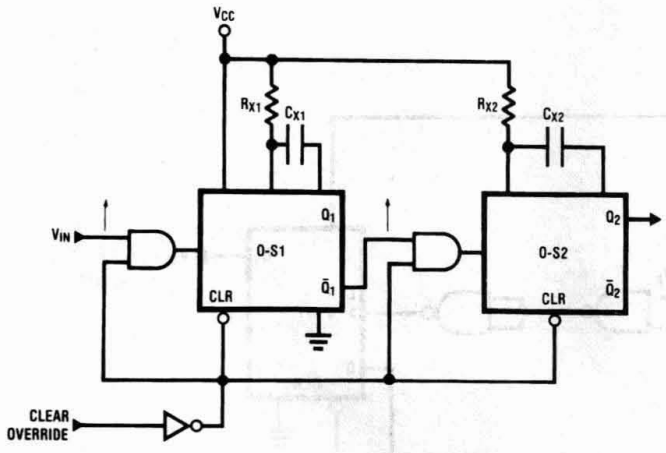
FIGURE 11. Pulse Generator (Retriggerable Device Required)

Note: K is the multiplication factor dependent of the device. Arrow indicates edge-trigger mode.

DELAYED PULSE GENERATOR WITH OVERRIDE TO TERMINATE OUTPUT PULSE *(Figure 12)*

An input pulse of a particular width can be delayed with the circuit shown in *Figure 12*. Preselected values of R_{X1} and C_{X1} determine the delay time via O–S1, while preselected values of R_{X2} and C_{X2} determine the output pulse width through O–S2. The override input can additionally serve to modify the output pulse width.



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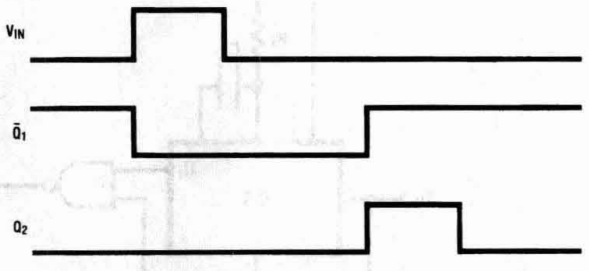

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FIGURE 12. Delayed Pulse Generator with Override to Terminate Output Pulse

MISSING PULSE DETECTOR *(Figure 13)*

By setting the time constant of O–S1 through R_{X1} and C_{X1} to be the least one full period of the incoming pulse period, the one-shot will be continuously retriggered as long as no missing pulse occurs. Hence, $\overline{Q}_1$ remains LOW until a pulse is missing in the incoming pulse train, which then triggers O–S2 and produces an indicating pulse at Q_2. (Retriggerable device required.)

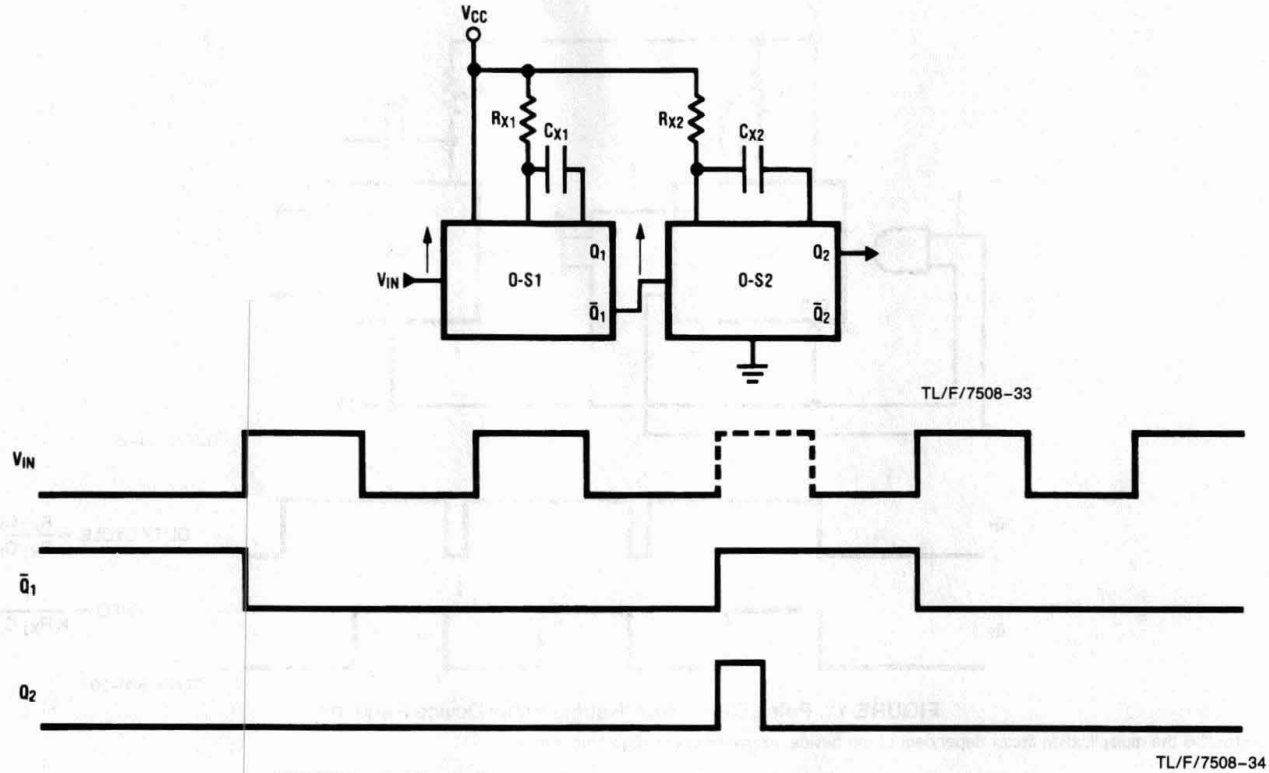

FIGURE 13. Missing Pulse Detector (Retriggerable Device Required)

PULSE WIDTH DETECTOR *(Figure 14)*

The circuit of *Figure 14* produces an output pulse at V_{OUT} if the pulse width at V_{IN} is wider than the predetermined pulse width set by R_X and C_X.

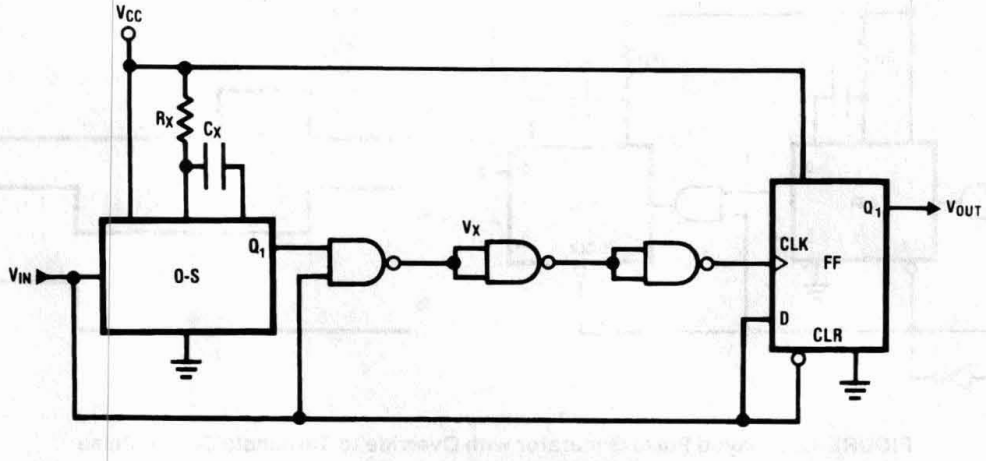

FIGURE 14. Pulse Width Detector

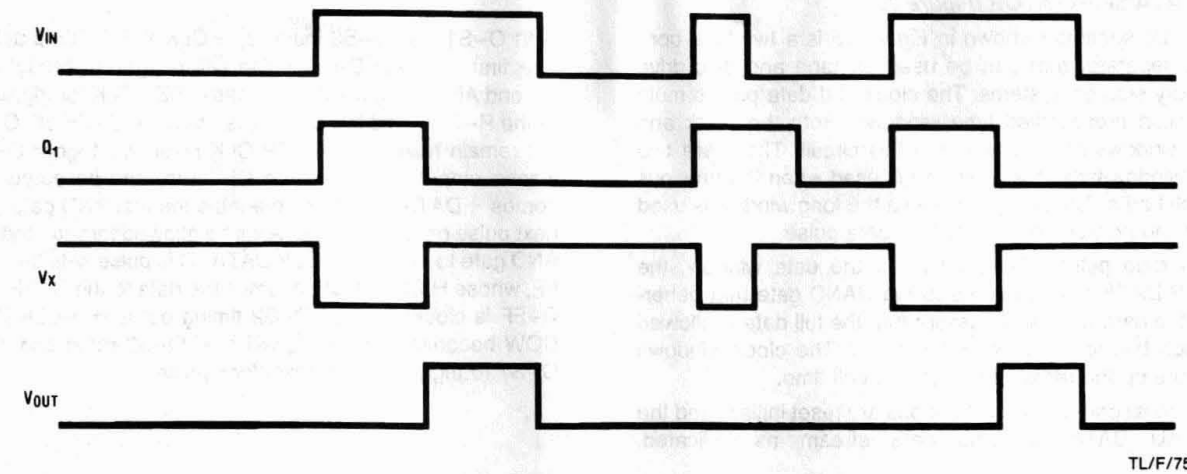

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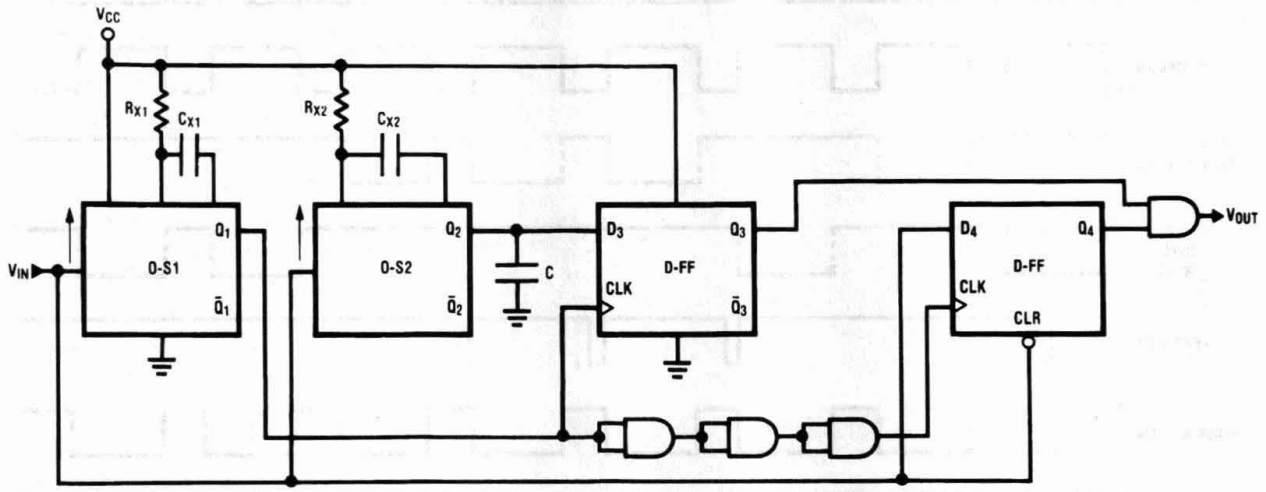
FIGURE 14. Pulse Width Detector (Continued)

BAND PASS FILTER ***(Figure 15)***

The band pass of the circuit is determined by the time constants of the two low-pass filters represented by O-S1 and O-S2. With the output at Q_2 delayed by C, the D-flip flop (D-FF) clocks HIGH only when the cutoff frequency of O-S2 has been exceeded. The output at Q_3 is gated with the delayed input pulse train at Q_4 to produce the desired output. (Retriggerable device required.)



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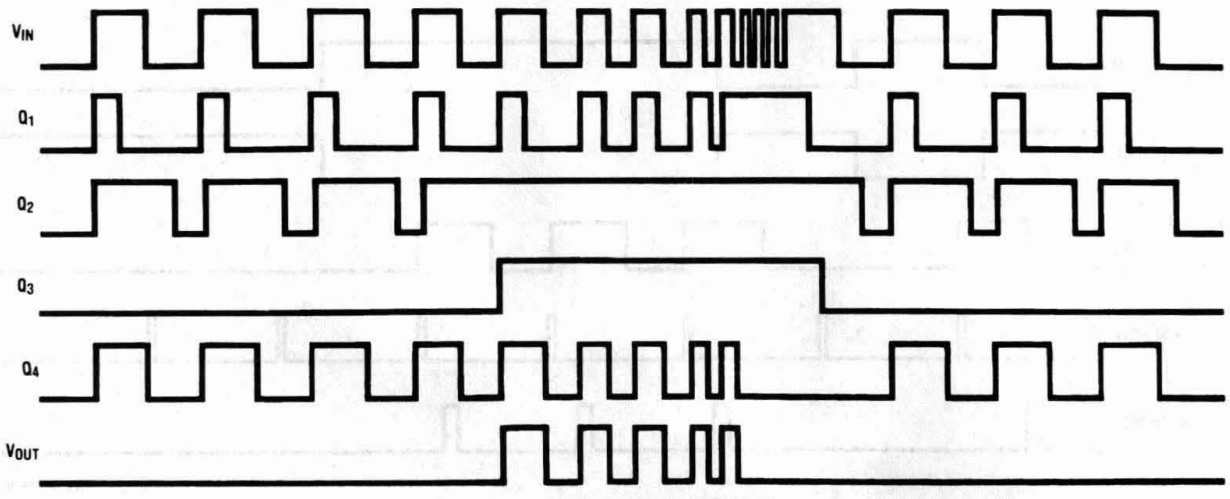

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FIGURE 15. Band Pass Filter (Retriggerable Device Required)

FM DATA SEPARATOR *(Figure 16)*

The data separator shown in *Figure 16* is a two-time constant separator that can be used on tape and disc drive memory storage systems. The clock and data pulses must fall within prespecified time windows. Both the clock and data windows are generated in this circuit. There are two data windows; the short window is used when the previous bit cell had a data pulse in it, while the long window is used when the previous bit cell had no data pulse.

If the data pulse initially falls into the data window, the —SEP DATA output returns to the NAND gate that generates the data window, to assure that the full data is allowed through before the window times out. The clock windows will take up the remainder of the bit cell time.

Assume all one-shots and flip-flops are reset initially and the +READ DATA has the data stream as indicated. With O–S1 and O–S2 inactive, +CLK WINDOW is active. The first +READ DATA pulse will be gated through the second AND gate, which becomes —SEP CLK for triggering of the R–S FF and the one-shots. With the D–FF off, O–S1 will remain reset. The —SEP CLK pulse will trigger O–S2, whose output is sent to the OR gate, and its output becomes +DATA WINDOW to enable the first AND gate. The next pulse on +READ DATA wil be allowed through the first AND gate to become —SEP DATA. This pulse sets the R–S FF, whose HIGH output becomes the data to the D–FF. The D–FF is clocked on by O–S2 timing out and +CLK WINDOW becoming active. $\overline{Q}_4$ will hold O–S2 reset and allow O–S1 to trigger on the next clock pulse.

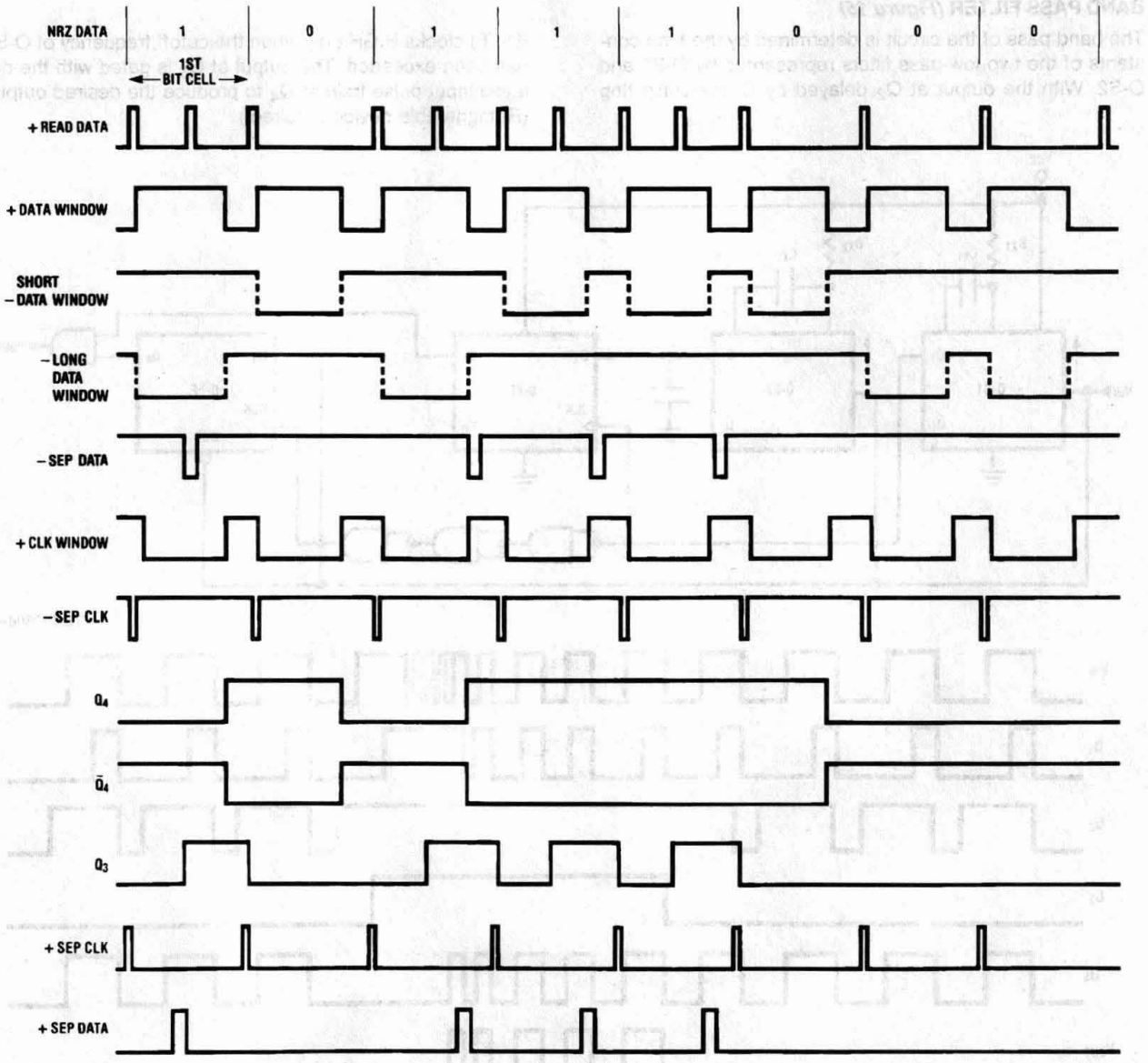

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FIGURE 16. FM Data Separator

The next clock pulse (the second bit cell) is ANDed with +CLK WINDOW and becomes the next —SEP CLK, which will reset the R–S FF and trigger O–S1. As O–S1 becomes active, the +DATA WINDOW becomes active, enabling the first AND gate. With no data bit in the second bit cell, the R–S FF will remain reset, enabling the D–FF to be clocked off when +DATA WINDOW falls. When the D–FF is clocked off, Q_4 will hold O–S1 reset and allow O–S2 to be triggered.

The third clock pulse (bit cell 3) is ANDed with +CLK WINDOW and becomes —SEP CLK, which continues resetting the R–S FF and triggers O–S2. When O–S2 becomes active, +DATA WINDOW enables the first AND gate, allowing the data pulse in bit cell 3 to become —SEP DATA. This —SEP DATA will set the R–S FF, which enables the D–FF to be clocked on when +DATA WINDOW falls. When this happens, Q_4 will hold O–S2 reset and allow O–S1 to trigger. This procedure continues as long as there is clock and data pulse stream present on the +READ DATA line.

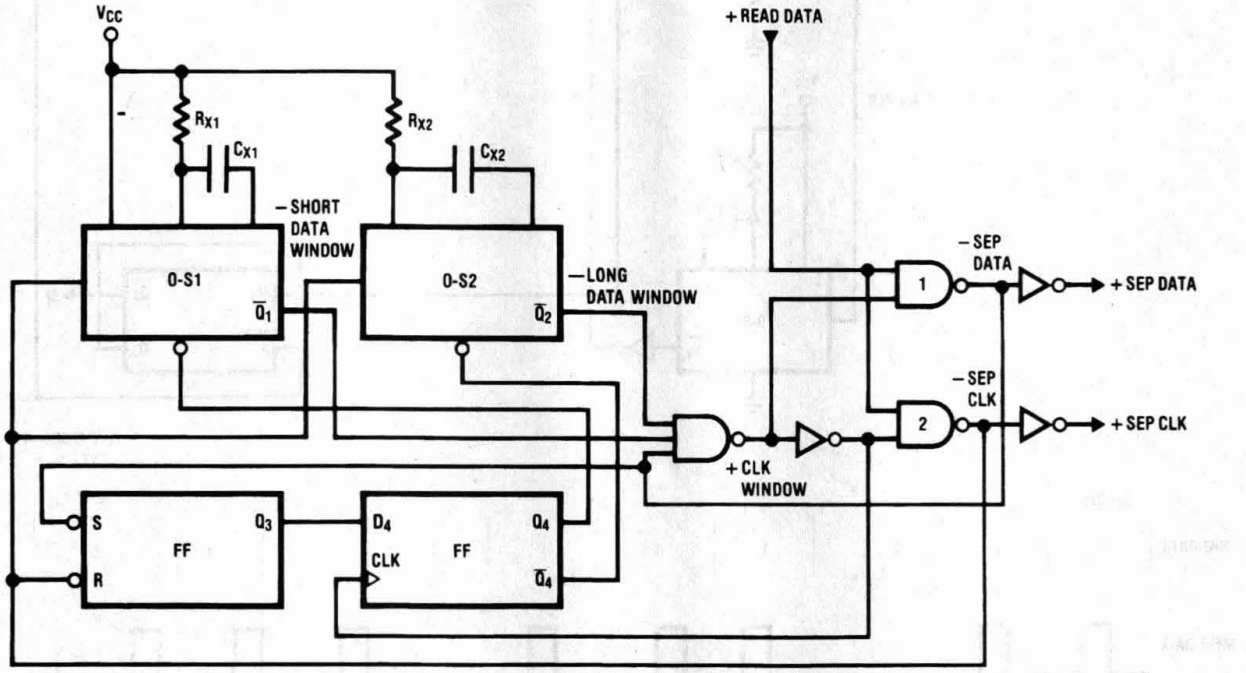

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FIGURE 16. FM Data Separator (Continued)

PHASE-LOCKED LOOP VCO *(Figure 17)*

The circuit shown in *Figure 17* represents the VCO in the data separation part of a rotational memory storage system which generates the bit rate synchronous clocks for write data timing and for establishing the read data windows.

The op-amp that performs the phase-lock control operates by having its inverting input be driven by two sources that normally buck one another. One source is the one-shot, the other source is the phase detector flip-flop. When set, the one-shot, through an inverter, supplies a HIGH-level voltage to the summing node of the op-amp and the phase detector FF, also through an inverter, supplies a canceling LOW-level input.

It is only when the two sources are out of phase with each other, that is one HIGH and the other LOW, that a positive- or negative-going phase error will be applied to the op-amp to effect a change in the VCO frequency. *Figure 17* illustrates the process of phase-error detection and correction when synchronizing to a data bit pattern. The rising edge of each pulse at DATA+PLO clocks the one-shot LOW and the phase detector FF HIGH. Since both outputs are still bucking each other, no change will be observed at the phase-error summing node. When the one-shot times out, if this occurs after the 2F clock has reset the phase detector FF to a LOW output, a positive pulse will be seen at the summing node until both the one-shot and the FF are reset. Any positive pulse will be reflected by a negative change in the op-amp output, which is integrated and reduces the positive control voltage at the VCO input in direct proportion to the duration of the phase-error pulse. A negative phase-error pulse occurs when the phase detector FF remains set longer than the one-shot.

Negative phase-error pulse causes the integrated control voltage to swing positive in direct proportion to the duration of the phase-error pulse. It is recommended that a clamping circuit be connected to the output of the op-amp to prevent the VCO control voltage from going negative or more positive than necessary. A back-to-back diode pair connected between the op-amp and the VCO is highly recommended, for it will present a high impedance to the VCO input during locked mode. This way, stable and smooth operation of the PLO circuit is assured.

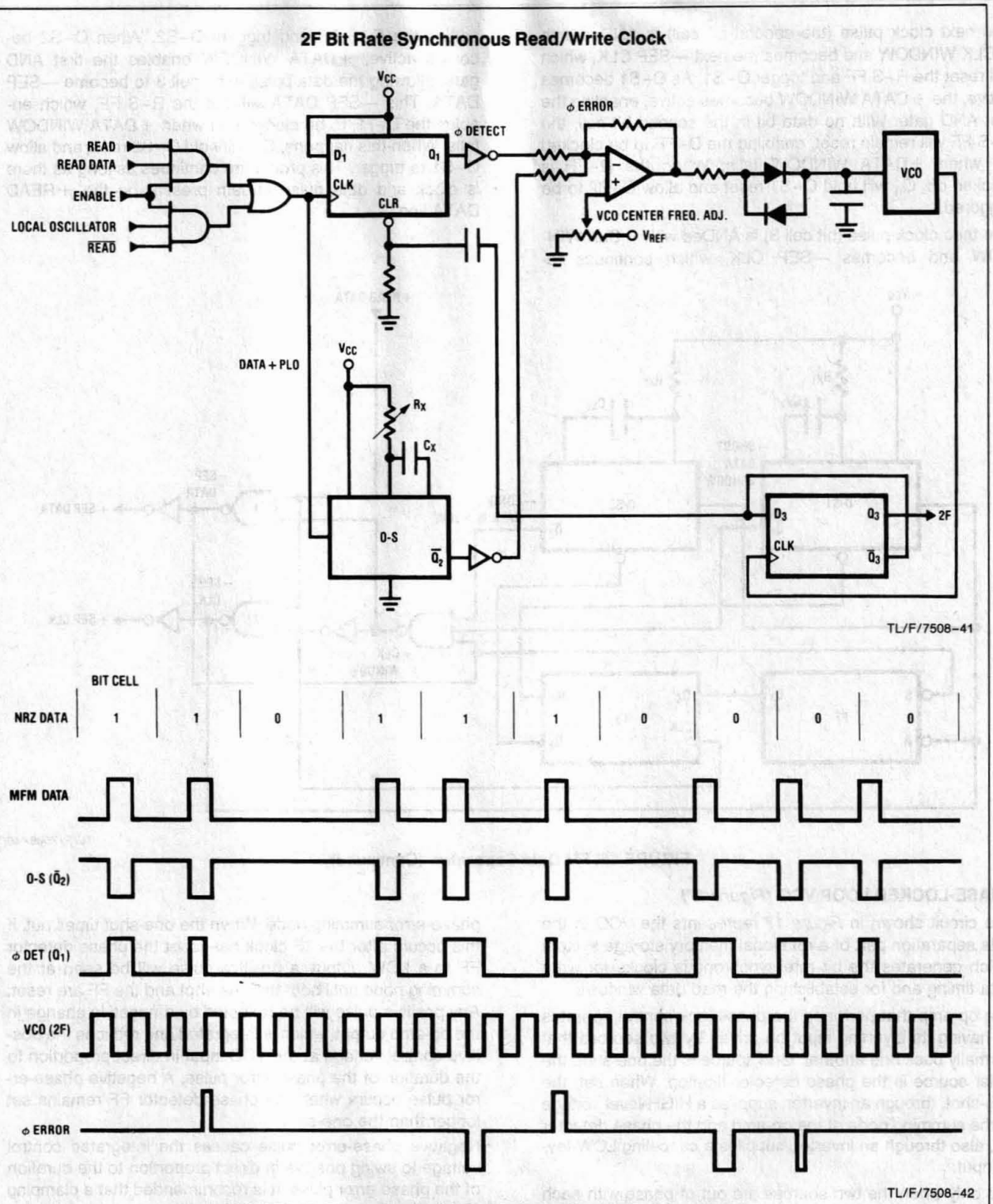

FIGURE 17. Phase-Locked Loop Voltage Controlled Oscillator

A FINAL NOTE

It is hoped that this brief note will clarify many pertinent and subtle points on the use and testing of one-shots. We invite your comments to this application note and solicit your constructive criticism to help us improve our service to you.

ACKNOWLEDGEMENT

The author wishes to thank Stephen Wong, Bill Llewellyn, Walt Sirovy, Dennis Worden, Stephen Yuen, Weber Lau, Chris Henry and Michelle Fong for their help and guidance.

Guide to ALS and AS

National Semiconductor Corp.
Application Note 476
Walt Sirovy

INTRODUCTION

Since the introduction of the first bipolar Transistor-Transistor Logic (TTL) family (DM54/74), system designers have wanted more speed, less power consumption, or a combination of the two attributes. These requirements have spawned other logic families such as the DM54/74L (low power), DM54/74LS (low power Schottky), DM54/74S (Schottky), etc., in order to give the system designers some choice.

The most common way of comparing logic families is by using their speed-power products. *Figure 1* displays a graphical representation of the logic families now available. The addition of the Advanced logic families broadens the spectrum of speed/power characteristics. This will allow the system designer to optimize his system's speed/power product by using performance budgeting. Performance budgeting is the intermixing of logic families to achieve the best speed/power product for a design. This is possible since bipolar logic families are designed to be fully compatible with each other. When the designer uses performance budgeting he is trading power consumption for speed. The designer identifies the speed critical paths and uses the fastest products to optimize the system's speed. For all other non-critical speed paths, the logic family with the best speed/power product should be used to optimize his system's power consumption. Since no other family offers the speed capability of AS and the low power of ALS, these families are the best choice when performance budgeting.

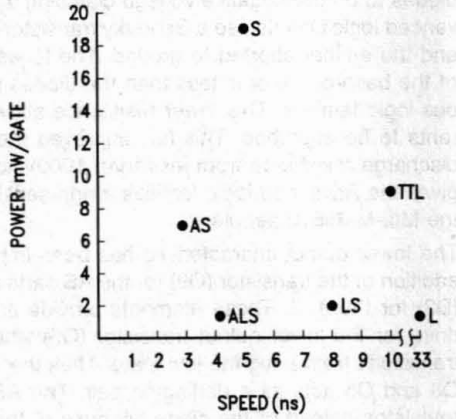

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FIGURE 1. Speed Power Product Comparison

Each of the logic families is a compromise between speed and power consumption. Since the speed/power product is approximately a constant, a decrease in the power consumption must be traded off in a slowing down of the device and vice versa. The power consumption of a device is the easiest to control. By simply increasing the resistive values in the circuit the power consumption can be decreased.

The device speed can be handled in a similar manner. The speed of a device is limited by the charge stored in the transistors of the circuits. The time to remove this charge is proportional to the capacitance of the transistor and the current supplied. In the early speed improvements, the current aspect of this relationship was involved. A simple decrease in the resistive values in the circuits was done. This did help the speed but it greatly increased the power consumption. The advent of the Schottky transistor helped increase the device speed. The Schottky transistor adds a Schottky clamp diode between the base and collector of the transistor. The Schottky clamp diode has a lower forward voltage (about 0.4V) than the base-collector junction diode (about 0.5V). When the transistor is turned on the base current drives the transistor toward saturation and the collector voltage drops. This causes the Schottky clamp diode to conduct and divert some of the base current from the base-collector junction of the transistor. This clamp diode prevents the transistor from going into deep saturation. This allows the transistor to recover quickly by decreasing the transistor storage time. The Schottky logic families (DM54/74S, DM54/74LS) used the Schottky transistor and low values of resistors to achieve their high speeds.

Now NSC has introduced the Advanced Low Power Schottky (ALS) and the Advanced Schottky (AS) logic families. These families use a reduced transistor size, advanced process technology, and innovative design techniques to achieve the improved device speeds. This article will discuss various aspects of the Advanced logic families including design goals, application goals, circuit design enhancements, family features, and some helpful application tips.

ADVANCED LOGIC FAMILIES DESIGN GOALS

For the Advanced logic families our main design goal was to reduce the power consumption while improving the speed of the parts. We also set the requirement that the Advanced logic parts be pin for pin compatible with existing logic families to allow ease of system upgrading and interfacing with existing products.

The design goals for ALS family were to produce a complete logic family which would achieve one half the propagation delays of DM54/74LS at one half the power dissipation of DM54/74LS and improve the capability of the outputs to drive 50 to 100Ω lines.

For the AS family the design goal was to produce a complete logic family which would achieve one half the propagation delays of DM54/74S at one third the power dissipation of DM54/74S.

We set some goals for both Advanced logic families that were more application related because of our experience with other logic families. These goals were to improve the input characteristics and line driving capability, reduce internally generated supply current spikes, eliminate parasitic failure modes and decoding glitches, and provide better electro-static discharge protection.

AN OVERVIEW OF THE ADVANCED LOGIC FAMILIES

The Advanced logic families (ALS & AS) have included most of the functions now present in the DM54/74LS and DM54/74S families. Some additions have been made to the Advanced families over the DM54/74LS and S families in order to make the families more complete. Both of the Advanced families have added a better (more complete) selection of octal bus transceivers, transparent latches and D-type flip-flops. A series of logic gate drivers (800 series) have been added to the ALS family. These devices have increased logic high and low current capabilities which allow the driving of high capacitive lines. These drivers have also been added to the AS family but have been designated the 1000 series. The ALS family has also added a series of gate

buffers (1000 series) which increase the fanout of these devices by increasing the logic low and high driving capabilities (but not as much as the 800 series).

The datasheets for the Advanced Logic devices have been improved in order to more accurately reflect application requirements and to reduce the need for special testing. The supply voltage range for the commercial products has been defined as 10% (4.5V to 5.5V) instead of 5% as all other bipolar logic have done in the past. The high level output voltage specification has been changed to $V_{CC}-2$ to allow easier interfacing with CMOS parts which have V_{CC} sensitive thresholds and to better reflect the actual operation of the parts. The output drive current (I_O) is measured at a forcing voltage of 2.25V instead of 0V used by other logic families. This demonstrates that the Advanced logic families have sourcing capability through the threshold level of the next gate. The low level input current (I_{IL}) specification has been reduced from $-400\ \mu A$ used for DM54/74LS to $-100\ \mu A$ for ALS. This indicates that ALS devices' I_{IL} current is less of a dominant factor in the limiting of device fanout. Current sinking capability (I_{OL}) for the AS family of TRI-STATE devices has been substantially increased (20 to 48 mA) over the DM54/74S family to allow the connection of these parts to a heavily loaded bus. The dynamic characteristics (propagation delays, etc.) have been specified over the supply voltage and temperature range. Also the output load used to test the dynamic characteristics has been simplified to allow easier construction of hardware for automatic test equipment and still reflect in-circuit operation. These items should give the designer a higher confidence level of the product used in his systems. Table 1 shows a comparison between ALS/AS and LS/S product. Appendix A includes generic datasheets for ALS and AS family of products.

TABLE 1. Family Comparison

Logic Family	Typical Delay (ns)	Typical Power (mW)	I_{OL} Max (mA)	I_{IL} Max (mA)
LS STD	8	2	8	−0.4
LS TS	8	6	24	−0.4
HC	8	—	4	−0.001
ALS STD	4	1.3	8	−0.1
ALS BUFFER	4	3	24	−0.1
54S	3	20	20	−2.0
AS	1.5	7.6	20	−0.5
AS BUFFER	2	8	48	−0.5

V_{CC} = 5V, C_L = 15 pF

CIRCUIT DESIGN ENHANCEMENTS

One of the design enhancements of the Advanced logic families is the improvement of the input threshold voltage. *Figures 4* (ALS schematic) and *5* (AS schematic) are used for reference for the following discussion. The input threshold is determined by the following equation.

$$V_{threshold} = V_{BE(Q2)} + V_{BE(Q3)} + V_{BE(Q4)} - V_{BE(Q1)}$$

The typical VBE of these transistors is 0.7V. Therefore the typical threshold voltage is 1.4V. This optimizes the threshold point between the high and low level input voltages. This provides maximum noise immunity. *Figure 2* demonstrates the threshold enhancement.

Another of the design enhancements is the use of a PNP transistor in the input circuitry. The use of the PNP transistor reduces the typical I_{IL} of these circuits ($-10\ \mu A$ for ALS and $-50\ \mu A$ for AS). When using a PNP transistor the equation for I_{IL} becomes:

$$I_{IL} = \frac{V_{CC} - V_{BE(Q1)} - V_I}{R(h_{FE(Q1)} + 1)}$$

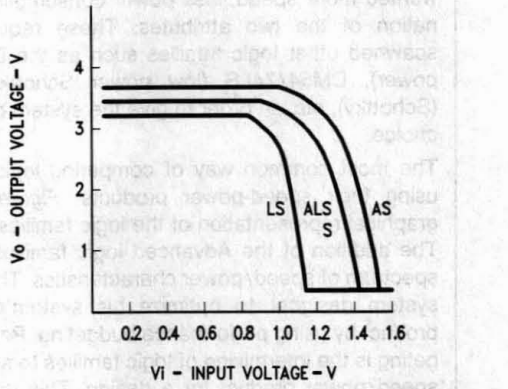

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FIGURE 2. V_{IN} vs V_{OUT}

Past logic families which used diodes or NPN transistors at the inputs had higher I_{IL} since they lacked the gain (h_{FE}) of the PNP transistor. The PNP transistor of the Advanced families effectively eliminates the I_{IL} current from being a dominant limiting factor in device fanout. The fanout constraints are now primarily associated with AC loading.

The input clamping and electrostatic discharge protection methods have also been improved. Past circuits have used diodes to do the negative voltage clamping action. The Advanced logic circuits use a Schottky transistor with the base and the emitter shorted to ground. The forward resistance of the base-collector is less than the diodes used in previous logic families. This lower resistance allows higher currents to be absorbed. This has improved the electrostatic discharge resistance from less than 1000V to 4000V. This gives the Advanced logic families a non-sensitive rating for the MIL-M-38510 people.

The lower output characteristic has been improved by the addition of the transistor (Q9) for the AS parts and the diode (D3) for the ALS. These elements provide additional base drive for the lower output transistor (Q5) when the output transitions from a high to low state. Thus the transistor pair Q3 and Q5 acts as a darlington pair. The AS parts use a transistor instead of the diode because of the higher drive requirements. *Figure 3* shows the Advance families output

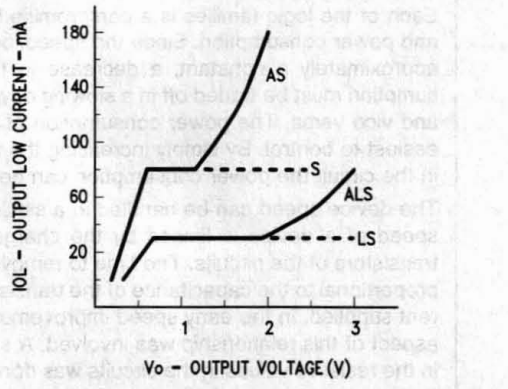

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FIGURE 3. Low Logic Level V_{OUT} vs I_{OUT}

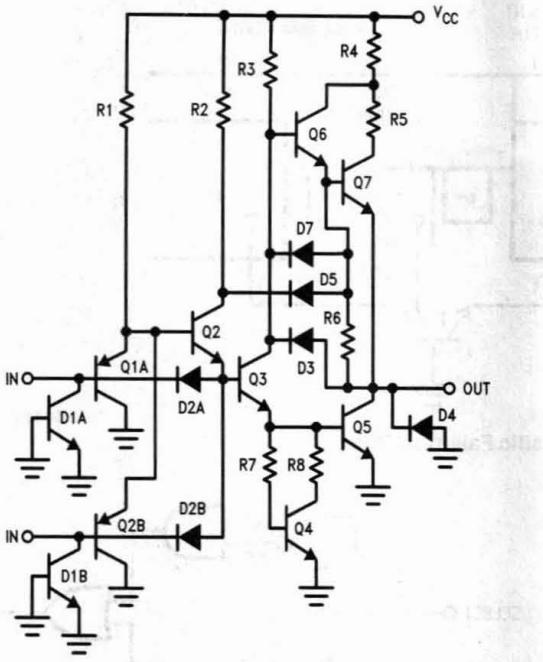

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FIGURE 4. ALS00 Schematic

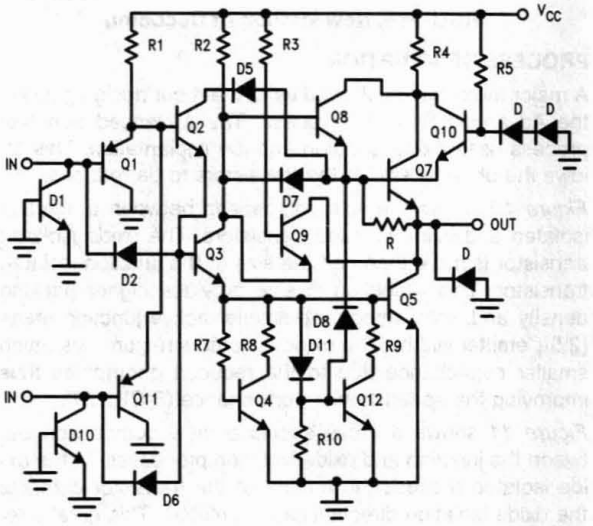

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FIGURE 5. AS00 Schematic

characteristic compared to the old Schottky families. Note that the current sink capability of the AS family takes off at 1.5V while the DM54/74S family remains flat. The ALS graph shows a similar characteristic but the break point is 1.8V.

The Advanced logic families include the output shaping circuit used in most modern bipolar logic families. This circuit consisting of transistor Q4, resistor R7 and resistor R8 helps to turn off the low output transistor Q5 during the low to high output transition. The diode D7 is used to help turn off the upper output transistor (Q7).

The AS circuits incorporate additional circuitry to reduce current supply spikes. During a low to high transition a supply current spike can be produced because the lower output transistor (Q5) remains temporarily on. This can increase the power consumed by the circuit especially at high frequencies. The lower output transistor remains on because of charge being coupled by this transistor's base-collector capacitance. The circuitry used to eliminate this problem is the addition of a transistor (Q9), two diodes (D8 & D11), and two resistors (R9 & R10). This circuit has been named the Miller killer. The diode (D8) is used as a capacitor to couple charge into the base of the transistor, Q9, during a low to high transition of the output. Thus Q9 turns on providing a means of turning off the lower output transistor (Q5). This circuitry is not required for most ALS devices due to the lower frequency of operation and smaller output structures.

APPLICATION RELATED DESIGN IMPROVEMENTS

A major consideration in the layout of the Advanced logic families was their response to negative transients. The Advanced logic families have high transition rates which can generate large reflections (−2.5 volts) when terminated into a high impedance. A method of limiting reflections is to use a clamp diode. All the Advanced logic devices include Schottky clamp diodes on both the inputs and outputs. These clamp diodes may have to handle peak currents of 30 to 60 mA. At these currents substrate junctions will become forward biased.

Figure 6 shows a cross sectional view of the area of an Advanced logic device where a negative transient may be a problem. A negative transient on an input or output tank (the structure in the center) will forward bias the substrate to N epi junction. This will form a parasitic NPN transistor between adjacent structures. If the adjacent structure is an input or output the only impact will be an increase in the leakage current. Since most of the devices have an active totem pole output design a logic state change does not happen. If the adjacent structure is a collector of an internal transistor the increase in the leakage current may cause a logic state change from a high logic state to a low logic state. This state change in a combinational logic part can propagate to the output and cause a glitch which can affect the system performance. If the adjacent transistor is part of a flip-flop a change in the logic state can happen. This can cause a sequential error in the system.

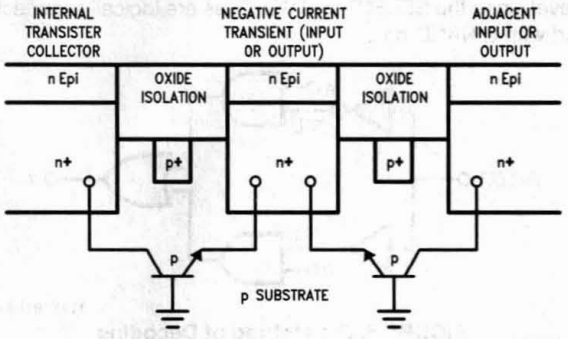

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FIGURE 6. Parasitic Failures Modes

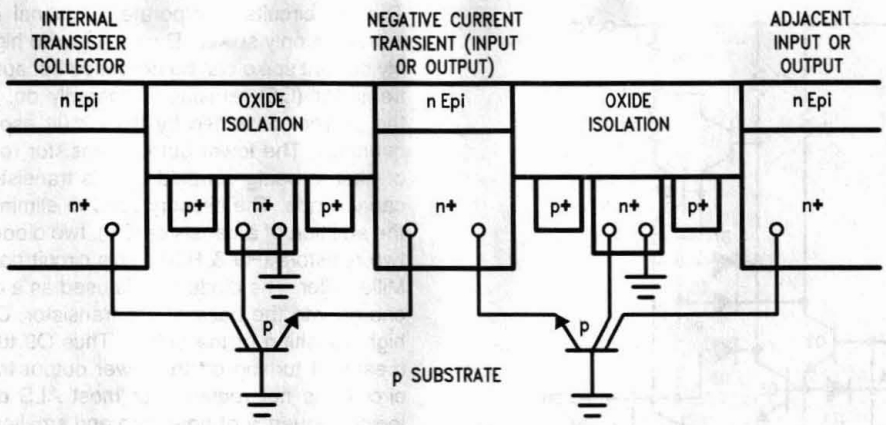

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FIGURE 7. Solution to Parasitic Failures Modes

Figure 7 demonstrates the method we use to minimize this problem. A grounded N+ guard ring around all input and output transistors is included. The guard ring increases the spacing between the two structures thus reducing the efficiency of the parasitic transistor. The grounded guard ring also acts as an energy well which collects the majority of the electrons injected by the parasitic transistor. An example of the amount of protection achieved can be demonstrated by looking at the ALS74. Without the guard ring this device will change state with only −5 mA input current. With a guard ring the device can withstand in excess of −35 mA input current with no change in logic state and only a few tenths of a volt degradation of the high state logic level.

Another problem associated with older logic families is decoding glitches. The old method of decoding is demonstrated in *Figure 8*. A decoding glitch occurs when the A and B inputs are at a high logic level and the select input transitions from a low to high logic level. The propagation delay from a high to a low logic level is faster for the inverting gate than the propagation delay from a low to high logic level is for the non-inverting gate. This causes both the SEL and the SEL′ lines to be at a low logic level for a short time. If both these lines are at a low logic level at the same time the Y output will transition to a low logic level even if the A and B inputs are at a high logic level. With the circuit used for the Advanced logic families *(Figure 9)* the SEL′ line cannot go to a low logic level until the SEL line goes to a high logic level since the SELECT and SEL lines are logically connected with a NAND gate.

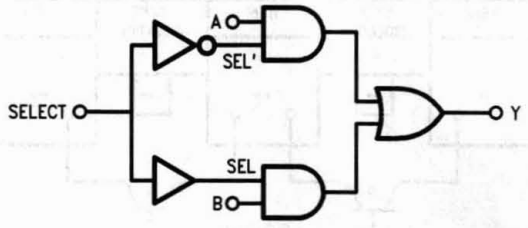

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FIGURE 8. Old Method of Decoding

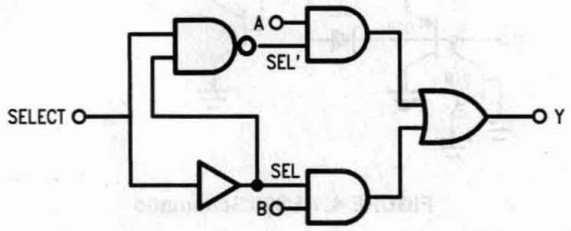

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FIGURE 9. New Method of Decoding

PROCESS DESCRIPTION

A major factor which allowed us to meet our design goals is the Advanced Schottky process. The Advanced Schottky process uses oxide isolation and ion implantation. This allows the physical size of the transistors to be reduced.

Figure 10 shows the size comparison between a junction isolated and oxide isolated transistors. The oxide isolated transistor is more than half the size of the junction isolated transistor. This reduction in size provides higher packing density and, most important, smaller active junction areas (2.5μ emitter width). The oxide isolated structure has much smaller capacitance due to the reduced geometries thus improving the speed/power performance (5 GHz FT).

Figure 11 shows a cross sectional view comparison between the junction and oxide isolation processes. In the oxide isolated process the emitter of the transistor contacts the oxide isolation directly (walled emitter). This greatly reduces the side wall capacitance since the capacitance is inversely proportional to the dielectric constant and dielectric constant between silicon/oxide is much smaller than the dielectric constant between two sections of silicon.

Ion implantation is a technique of introducing impurities by bombarding the host material with a beam of ions. This technique is superior to the deposition method used in previous processes because it is easier to control the amount of impurities introduced into the silicon. The deposition method relies on control of diffusion time, diffusion temperature, gasflow rate and surface cleaniness. Ion implantation relies on the control of only current and voltage of the machine.

Figure 12 is a lengthwise cross sectional view of the oxide isolated transistor. From this figure it can be seen that the limiting factor of the size of the transistor is the metal interconnects and the spacing between the metal.

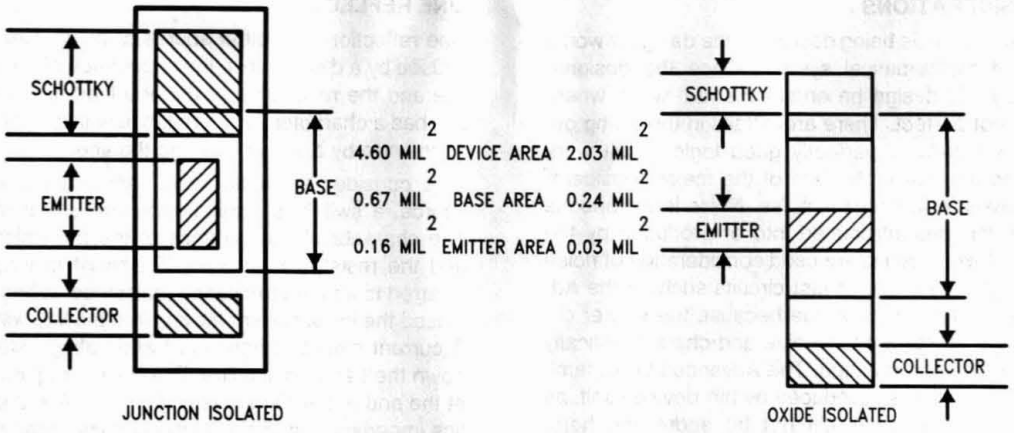

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FIGURE 10. Top View of Junction and Oxide Isolated Transistors

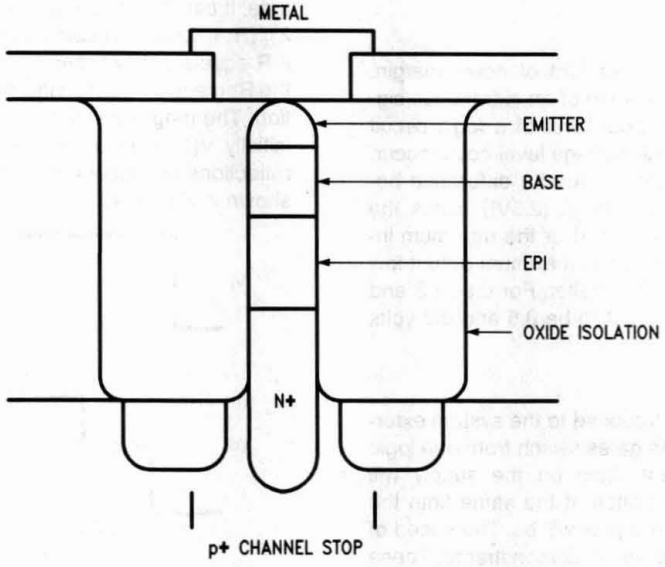

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FIGURE 11. Cross Sectional View of Oxide Isolated Transistor

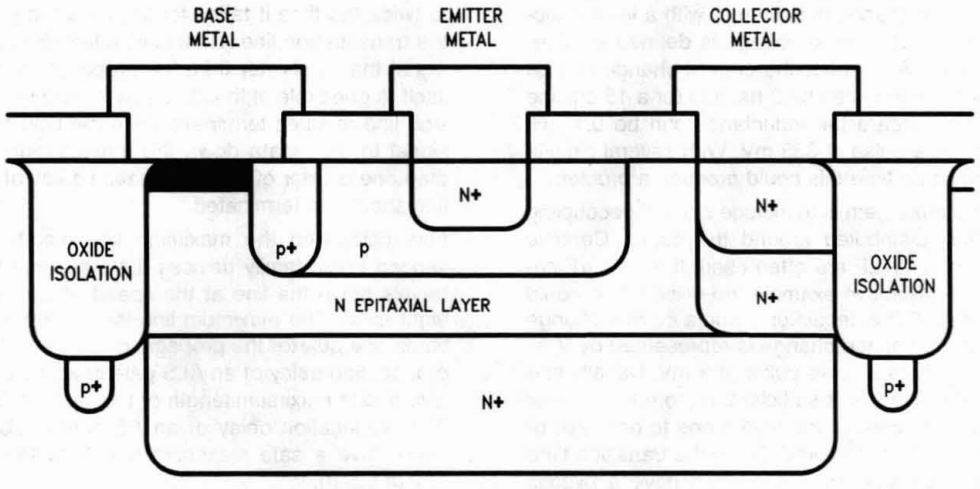

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FIGURE 12. Cross Sectional View of Oxide Isolated Transistor

NOISE CONSIDERATIONS

When a digital system is being designed, the designer works with a perfect mathematical system. Once the designer starts to layout his design he enters the real world where everything is not perfect. There are pitfalls in the laying out circuits that will make a perfectly good logic circuit work incorrectly and unpredictably. One of the major considerations in the layout of a circuit is noise. Noise is extraneous currents and voltages introduced into or produced by the circuit. When slower circuits are used consideration of noise is not as important as it is for fast circuits such as the Advanced Logic families. This is true because the slower circuits take longer to respond to noise and characteristically noise is pulses of short duration. The Advanced Logic families have addressed noise produced by the device itself, as mentioned previously, so it will not be addressed here. Noise can be introduced by several methods: external to the system, cross talk between lines, power supply spikes and line reflections. Each of these problems will be examined and solutions presented.

NOISE MARGIN

Each logic family has a certain amount of noise margin. Noise margin is the voltage amplitude of an extraneous signal that can be added to the input level of a logic circuit before change in the output logic voltage level could occur. Worst case noise margin is defined as the difference between the minimum high voltage [V_{OH} (2.5V)] minus the maximum input high voltage [V_{IH} (2V)] or the maximum input low voltage [V_{IL} (0.8V)] minus the maximum output low voltage [V_{OL} (0.5V)] whichever is smaller. For the ALS and AS families these numbers turn out to be 0.5 and 0.3 volts respectively.

POWER SUPPLY SPIKES

Power supply spikes can be introduced to the system externally or generated internally. As gates switch from one logic state to another, their current drain on the supply will change. The more gates that switch at the same time the greater the current drain on the supply will be. The speed of the changes is also a factor as will be demonstrated. These current changes produce voltage variations because of supply line resistance and inductance.

In most designs the supply lead inductance is the dominant factor. For a current change di in time dt with a lead inductance of L, the resulting noise voltage is defined as $V = L[di/dt]$. For a octal ALS buffer the current change can be 10 mA, the transition time can be 3 ns, and for a 15 cm line on a printed circuit board the inductance can be 0.1 μH. This will give a noise pulse of 333 mV. With several circuits switching at the same time this could produce a problem.

The solution to the problem is to include several decoupling capacitors evenly distributed around the board. Ceramic disc capacitors of 0.01 μF are often used. If a 0.01 μF capacitor is used in the above example the noise pulse would be greatly reduced. For a capacitor C and a current change di in the time dt the voltage change is represented by $V = [(di)(dt)]/C$. This gives a noise pulse of 3 mV. Usually one capacitor for every five ICs is sufficient. If more high power ICs (buffers and line drivers) are used a one to one ratio of capacitor to ICs might be required. Since the transition time of AS devices is so fast, each IC should have a bypass capacitor. These capacitors are inexpensive and will greatly increase the reliability of your design.

LINE REFLECTIONS

Line reflection is another source of noise. Line reflection is caused by a difference in the impedance of the transmission line and the resistance of the line load. Each transmission line has a characteristic impedance which is the initial resistance seen by a signal entering the line.

Lets consider a simple circuit which includes a voltage source, a switch, a transmission line and a resistive load. The characteristic impedance of the transmission line is Z and the resistive load is R. The resistive load, R, can be referred to as the terminating resistance. When the switch is closed the initial current flowing into the line will be $I = V/Z$. A current step of magnitude I and voltage step of V flows down the transmission line. The current required by the load at the end of the transmission line is V/R. If the characteristics impedance of the transmission line does not equal the load resistance a partial reflection of the signal will occur.

One can define a reflection coefficient (Rho) as the reflected voltage amplitude divided by the incident voltage amplitude. It can be mathematically shown that the $\text{Rho} = [R - Z]/[R + Z]$. If R equals 0 (short circuit) the Rho equals -1. If R equals infinity (open circuit) the Rho equals 1. If $R = Z$ the Rho equals 0 which indicates that there will be no reflection. The magnitude of the voltage at the load resistance is initially $V(1 + \text{Rho})$. If a reflection initially occurs, further reflections will occur until $I = V/R$. Possible waveforms are shown in *Figure 13*.

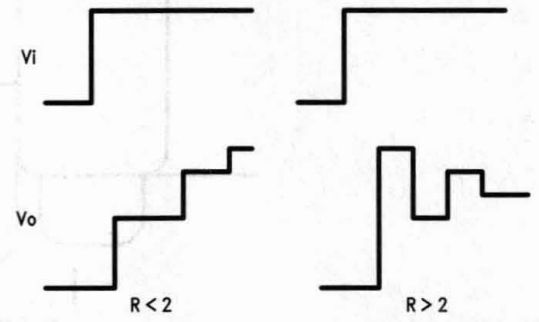

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FIGURE 13. Waveforms for Improperly Terminated Transmission Lines

It can be shown that the duration of each reflection is equal to twice the time it takes for the signal to propagate down the transmission line. Generally, gates do not respond to a signal that is shorter than the propagation delay of device itself. A good rule of thumb to use to determine if a transmission line requires termination is if the time required for the signal to propagate down the transmission line is greater than one quarter of the propagation delay of the device the line should be terminated.

Lets calculated the maximum line length for some Advanced Logic family devices. Lets assume that the signal travels down the line at the speed of light (3 X 10 to the eight m/s). The maximum line length is the speed of light times one quarter the propagation delay of the device. The propagation delay of an ALS gate is about 4 ns. This would give a safe maximum length of the line of 0.3m (about 1 ft). The propagation delay of an AS gate is about 2 ns. This would give a safe maximum length of the line of 0.15m (about 0.5 ft).

Another method of termination of a transmission line is a series termination. It can be shown that the initial step received at an open circuit termination is twice the input step.

If we have a series resistor at the transmitter that is equal to the characteristic impedance of the line the reflection would be absorbed by the series resistance. This method requires a high impedance receiver but uses less power than the previous method.

CROSS TALK

Cross talk is the coupling of a signal from one line to an adjacent line. It is caused by the mutual inductance and capacitance between signal lines. Long parallel lines are the most susceptible to this problem. To minimize the effects of cross talk, proper shielding, grounding and decoupling should be done. On lines which may be particularly sensitive to cross talk, the distance between these lines should be increased.

Use flat cable with alternate signal/ground wires, coaxial cable, signal lines (PCB track) above ground plane with the minimum distance between lines equal to the distance between ground plane and signal plane, or twisted pairs to minimize cross talk.

Unused Inputs

Unused inputs which are left open circuited can be a source of noise. An open circuited input settles at the threshold voltage of that node. It can act as an antenna and accept a signal. To avoid this problem any unused input should be tied to a potential that will not cause a logic error. For example, unused inputs of AND gates, NAND gates, and active low presets and clears of flip-flops should be tied to a high potential. Unused inputs of NOR gates should be tied to ground. Unused inputs that are tied to a high potential can be connected directly to the supply voltage as long as the 5.5V maximum is not exceeded. A better method is to connect unused inputs to a high potential through a resistor (1 kΩ or greater) to the supply voltage. This will give some protection in case this input is shorted to ground. Several inputs can be connected to this resistor.

Open-Collector Outputs

All open collector outputs, whether used alone or in a wired-OR configuration, requires an external pull-up resistor. The resistor value is dependent upon the fanout of the OR tie and the number of devices in the OR tie. R(min) is determined so that if only one output is LOW the maximum allowable OR tie fanout is not surpassed. The R(max) value is calculated with all the OR tied outputs HIGH to sustain the necessary V_{OH}.

N = # of wired-OR outputs

$$R_{(min)} = \frac{V_{CC(max)} - V_{OL}}{I_{OL} - M \times I_{IL}}$$

$$R_{(max)} = \frac{V_{CC(min)} - V_{OH}}{N \times I_{OH} + M \times I_{IH}}$$

M = # of inputs being driven
I_{IL} = LOW level input current
I_{IH} = HIGH level input current
V_{OL} = output LOW voltage (0.5V)
V_{OH} = output HIGH voltage (2.5)
I_{OL} = LOW level fanout current
$I_{OH} = I_{CEX}$ = output HIGH current

Example: Two ALS03 gate outputs driving three LS gates.

$$R_{(min)} = \frac{5.25V - 0.5V}{8\ mA - 3 \times 0.4\ mA} = 698\Omega$$

$$R_{(max)} = \frac{4.75V - 2.5V}{2 \times 0.1\ mA + 3 \times 0.02\ mA} = 16\ k\Omega$$

The R range for the pull-up is between 698 and 16 kΩ. The lower resistor values will provide faster speeds while the higher resistances give lower power dissipation.

SUMMARY

- Pin compatible with other 5V bipolar families
- Faster propagation delays
- Lower power consumption
- Better selection of octal bus transceivers, transparent latches, and D-type flip-flops
- Addition of series of line drivers
- Addition of series of buffers
- Dynamic characteristics specified over supply voltage and temperature range
- Improved input threshold voltage
- Improved ESD protection
- Better pin-to-pin isolation
- Elimination of decoding glitches

APPENDIX

Recommended Operating Conditions Advanced Low Power Schottky

Symbol	Parameter		Standard Output		Buffer Output		Bus Driver Output		Units
			Min	Max	Min	Max	Min	Max	
V_{CC}	Supply Voltage	54/74ALS	4.5	5.5	4.5	5.5	4.5	5.5	V
V_{IH}	High Level Input Voltage	54/74ALS	2		2		2		V
V_{IL}	Low Level Output Voltage	54/74ALS		0.8		0.8		0.8	V
I_{OH}	High Level Output Current	54ALS		−0.4		−1		−12	mA
		74ALS		−0.4		−2.6		−15	
V_{OH}(1)	High Level Output Voltage	54/74ALS		5.5		5.5		5.5	V
I_{OL}	Low Level Output Current (Note 2)	54/74ALS		4		12		12	mA
		74ALS		8		24		24	
		74ALS −1						48	
T_A	Operating Free-Air Temperature	54ALS	−55	125	−55	125	−55	125	°C
T_A	Temperature	74ALS	0	70	0	70	0	70	

Note 1: For open-collector outputs.

Note 2: The extended limits (−1) apply only if V_{CC} is maintained between 4.75 and 5.25V. These parts are offered as a commercial version only.

Electrical Characteristics Advanced Low Power Schottky

Symbol	Parameter	Conditions		Standard Output			Buffer Output			Bus Driver Output			Units
				Min	Typ(1)	Max	Min	Typ(1)	Max	Min	Typ(1)	Max	
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = − 18 mA				−1.5			−1.5			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, I_{OH} = Max					2.4	3.2		2	3.2		V
		V_{CC} = 4.5V, I_{OH} = −3 mA								2.4	3.2		
		V_{CC} = 4.5V to 5.5V, I_{OH} = −0.4 mA		V_{CC}−2			V_{CC}−2			V_{CC}−2			
I_{OH}	High Level Output Current	V_{CC} = 4.5V, V_{OH} = 5.5V				0.1			0.1			0.1	mA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = Max	54/74ALS		0.25	0.4		0.25	0.4		0.25	0.4	V
			74ALS		0.35	0.5		0.35	0.5		0.35	0.5	
I_I	Input Current at Maximum Input Voltage	V_{CC} = 5.5V, V_I = 7V				0.1			0.1			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_I = 2.7V				20			20			20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_I = 0.4V			−0.02	−0.1		−0.05	−0.1		−0.05	−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	−30		−112	−30		−112	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = 5.5V, V_O = 2.7V							20			20	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V, V_O = 0.4V	I/O Ports						0.1			0.1	mA
			Non I/O						−20			−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V											mA

Recommended Operating Conditions Advanced Schottky

Symbol	Parameter		Standard Output		Buffer Output		Bus Driver Output		Units
			Min	Max	Min	Max	Min	Max	
V_{CC}	Supply Voltage	54/74AS	4.5	5.5	4.5	5.5	4.5	5.5	V
V_{IH}	High Level Input Voltage	54/74AS	2		2		2		V
V_{IL}	Low Level Output Voltage	54/74AS		0.8		0.8		0.8	V
I_{OH}	High Level Output Current	54AS		−2		−12		−40	mA
		74AS		−2		−15		−48	
V_{OH}(1)	High Level Output Voltage	54/74AS		5.5		5.5		5.5	V
I_{OL}	Low Level Output Current	54/74AS		20		32		40	mA
		74AS		20		48		48	
T_A	Operating Free-Air Temperature	54AS	−55	125	−55	125	−55	125	°C
		74AS	0	70	0	70	0	70	

Note 1: For open-collector parts.

Electrical Characteristics Advanced Schottky

Symbol	Parameter	Conditions		Standard Output			Buffer Output			Bus Driver Output			Units
				Min	Typ(1)	Max	Min	Typ(1)	Max	Min	Typ(1)	Max	
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V I_I = −18 mA				−1.2			−1.2			−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V I_{OH} = Max					2.4	3.2		2	3.2		V
		V_{CC} = 4.5V to 5.5V I_{OH} = −2 mA		V_{CC}−2			V_{CC}−2			V_{CC}−2			
I_{OH}	High Level Output Current	V_{CC} = 4.5V V_{OH} = 5.5V				0.1			0.1			0.1	mA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V I_{OL} = Max			0.35	0.5		0.35	0.5		0.35	0.5	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = 5.5V V_I = 7V				0.1			0.1			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V V_I = 2.7V				20			20			20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_I = 0.4V				−0.5			−0.5			−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V V_O = 2.25V		−30		−112	−30		−112	−30		−112	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = 5.5V V_O = 2.7V							50			50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V V_O = 0.4V	I/O Ports						−0.5			−0.5	mA
			Non I/O						−50			−50	μA
I_{CC}	Supply Current	V_{CC} = 5.5V											mA

Functional Index/Selection Guide

*Several methods are used to represent typical values. For propagation delay typical values, the average of the typical values of the two delays are used.

$$\left[\frac{t_{PHL(TYP)} + t_{PLH(TYP)}}{2}\right]$$

For power dissipation, the average of the typical values of current for all states the outputs can achieve is used (I_{CCL}, I_{CCH}, I_{CCZ}.) This current value is multiplied by nominal supply voltage (5V), and in some cases divided by the number of gates, bits, etc. All other typical values are singular typicals.

Adders

Description	Device Type	Typ* Carry Time (ns)	Typ* Add Time (ns)	Typ* Power Diss./Bit (mW)	Package Availability		Page
					Mil	Com	
Single 4-Bit Full Adders	54/74LS283	12	15	24	J	N,M	†
	54/74S283	8.5	11	110	J	N	†
	54/74LS83A	12	15	24	J	N,WM	†

Arithmetic Logic Units, Carry Look-Ahead Generators

Description	Device Type	Typ* Carry Time (ns)	Typ* Add Time (ns)	Typ* Power Diss. Total (mW)	Package Availability		Page
					Mil	Com	
4-Bit ALU/ Function Generators	54/74AS181B	5	5	370	J	N	3-60
	54/74S181	7	14	600	J	N	†
	54/74181	12.5	18	455	J	N	†
	54/74S381	10	12	525	J	N	†
	54/74AS881B	5	5	370	J	N	3-193
Carry Look-Ahead Generator	54/74AS182	5	N/A	115	J	N	3-69
	54/74S182	9	N/A	345	J	N	†
	54/74AS264	6	N/A	140	J	N	3-88
	54/74AS282	6	N/A	130	J	N	3-97

Buffers/Clock Drivers with Totem-Pole Outputs

Description	Device Type	Low-Level Output Current (mA)	High-Level Output Current (mA)	Typ* Prop. Delay Time (ns)	Typ* Power Diss. /Gate (mW)	Package Availability		Page
						Mil	Com	
Dual 4-Input NAND Buffers	54ALS40A	12	−1	4	3.5	J		2-54
	74ALS40A	24	−2.6	4	3.5		N,M	2-54
	54/74S40	60	−3	4	44	J	N	†
	54ALS1020A	12	−1	4	3.6	J		2-295
	74ALS1020A	24	−2.6	4	3.6		N,M	2-295
Quad 2-Input NAND Buffers	54ALS37A	12	−1	5	5	J		2-50
	74ALS37A	24	−2.6	5	5		N,M	2-50
	54LS37	12	−1.2	10	4.3	J		†
	74LS37	24	−1.2	10	4.3		N,M	†
	54/7437	48	−1.2	10.5	27	J	N	†
	54ALS1000A	12	−1	5	3.5	J		2-279
	74ALS1000A	24	−2.6	5	3.5		N,M	2-279
	54AS1000A	40	−40	2	8.5	J	N	3-205
	74AS1000A	48	−48	2	8.5	J	N	3-205

† Please see the LS/S/TTL Logic Databook for this datasheet.

Buffers/Clock Drivers with Totem-Pole Outputs (Continued)

Description	Device Type	Low-Level Output Current (mA)	High-Level Output Current (mA)	Typ* Prop. Delay Time (ns)	Typ* Power Diss. /Gate (mW)	Package Availability		Page
						Mil	Com	
Quad 2-Input NOR Buffers	54ALS28A	12	−1	3.7	4.5	J		2-42
	74ALS28A	24	−2.6	3.7	4.5		N,M	2-42
	54ALS1002A	12	−1	3.7	4.5	J		2-281
	74ALS1002A	24	−2.6	3.7	4.5		N,M	2-281
	54AS1036A	40	−40	2	9.7	J		3-215
	74AS1036A	48	−48	2	9.7		N	3-215
Quad 2-Input OR	54ALS1032A	12	−1	5.5	5.7	J		2-297
	74ALS1032A	24	−2.6	5.5	5.7		N,M	2-297
	54AS1032A	40	−40	2.5	14	J		3-211
	74AS1032A	48	−48	2.5	14		N	3-211
Quad 2-Input AND	54ALS1008A	12	−1	5.6	4.7	J		2-289
	74ALS1008A	24	−2.6	5.6	4.7		N,M	2-289
	54AS1008A	40	−40	2.5	12	J		3-209
	74AS1008A	48	−48	2.5	12		N	3-209
Triple 3-Input NAND	54ALS1010A	12	−1	4	3.6	J		2-291
	74ALS1010A	24	−2.6	4	3.6		N,M	2-291
Triple 3-Input AND	54ALS1011A	12	−1	6.4	4.75	J		2-293
	74ALS1011A	24	−2.6	6.4	4.75		N,M	2-293
Hex Buffers	54ALS1034	12	−12	4.5	4.6	J		2-299
	74ALS1034	24	−15	4.5	4.6		N,M	2-299
	54AS1034A	40	−40	2.5	11.9	J		3-213
	74AS1034A	48	−48	2.5	11.9		N	3-213
Hex Inverter Buffers	54ALS1004	12	−12	2.6	3.3	J		2-285
	74ALS1004	24	−15	2.6	3.3		N,M	2-285
	54AS1004A	40	−40	1.7	8.5	J		3-207
	74AS1004A	48	−48	1.7	8.5		N	3-207

Buffers/Clock Drivers with Open-Collector Outputs

Description	Device Type	High-Level Output Voltage V	Low-Level Output Current (mA)	Typ* Prop. Delay Time (ns)	Typ* Power Diss. /Gate (mW)	Package Availability		Page
						Mil	Com	
Quad 2-Input NAND Buffers	54ALS38A	5.5	12	14.5	3.5	J		2-52
	74ALS38A	5.5	24	14.5	3.5		N,M	2-52
	54LS38	5.5	12	15	4.3	J		†
	74LS38	5.5	24	15	4.3		N,M	†
	54/7438	5.5	48	12.5	24.4	J	N,M	†
	54LS26	15	4	16	2	J		†
	74LS26	15	8	16	2		N,M	†
	54/7426	15	16	13.5	10	J	N	†
	54ALS1003A	5.5	12	14.5	3.5	J		2-283
	74ALS1003A	5.5	24	14.5	3.5		N,M	2-283

† Please see the LS/S/TTL Logic Databook for this datasheet.

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Buffers/Clock Drivers with Open-Collector Outputs (Continued)

Description	Device Type	High-Level Output Voltage (V)	Low-Level Output Current (mA)	Typ* Prop. Delay Time (ns)	Typ* Power Diss. /Gate (mW)	Package Availability		Page
						Mil	Com	
Quad 2-Input NOR Buffers	54ALS33A	5.5	12	13.5	4.5	J		2-48
	74ALS33A	5.5	24	13.5	4.5		N,M	2-48
Hex Buffers/ Drivers	5407	30	30	13	21	J		†
	7407	30	40	13	21		N,M	†
	5417	15	30	13	21	J		†
	7417	15	40	13	21		N	†
	54ALS1035	5.5	12	12.5	4.6	J		2-301
	74ALS1035	5.5	24	12.5	4.6		N,M	2-302
Hex Inverter Buffers/ Drivers	5406	30	30	12.5	26	J		†
	7406	30	40	12.5	26		N,M	†
	5416	15	30	12.5	26	J		†
	7416	15	40	12.5	26		N	†
	54ALS1005	5.5	12	12.5	3.3	J		2-287
	74ALS1005	5.5	24	12.5	3.3		N, M	2-287

Buffer Gates with TRI-STATE® Totem-Pole Outputs

Description	Device Type	Max Source Current (mA)	Max Sink Current (mA)	Typ* Prop. Delay Time (ns)	Typ* Power Diss. /Gate (mW)	Package Availability		Page
						Mil	Com	
Quad Buffers	54LS125A	−1	12	10	14.4	J		†
	74LS125A	−2.6	24	10	14.4		N,M	†
	54125	−2	16	11	40	J		†
	74125	−5.2	16	11	40		N	†
	54LS126A	−1	12	10	14.4	J		†
	74LS126A	−2.6	24	10	14.4		N,M	†
Hex Buffers	54LS365A	−1	12	10	10.8	J		†
	74LS365A	−2.6	24	10	10.8		N,M	†
	54365	−2	32	10.5	51.6	J		†
	74365	−5.2	32	10.5	51.6		N	†
	54LS367A	−1	12	10	10.8	J		†
	74LS367A	−2.6	24	10	10.8		N,M	†
	54367	−2	32	12	51.6	J		†
	74367	−5.2	32	12	51.6		N	†
Hex Inverter Buffers	54LS366A	−1	12	10	10.8	J		†
	74LS366A	−2.6	24	10	10.8		N,M	†
	54LS368A	−1	12	10	10.8	J		†
	74LS368A	−2.6	24	10	10.8		N,M	†
	54368	−2	32	10.5	51.6	J		†
	74368	−5.2	32	10.5	51.6		N	†
	70L98	−1	2	30	3	J		†
	80L98	−1	3.6	30	3		N	†

† Please see the LS/S/TTL Logic Databook for this datasheet.

Buffer Gates with TRI-STATE® Totem-Pole Outputs (Continued)

Description	Device Type	Max Source Current (mA)	Max Sink Current (mA)	Typ* Prop. Delay Time (ns)	Typ* Power Diss. /Gate (mW)	Package Availability		Page
						Mil	Com	
Octal Buffers	54ALS465A	−12	12	6.6	8.6	J		2-176
	74ALS465A	−15	24	6.6	8.6		N,M	2-176
	54LS465	−2.6	12	14.5	10	J		†
	74LS465	−5.2	24	14.5	10		N,M	†
	54ALS467A	−12	12	6.6	9.1	J		2-176
	74ALS467A	−15	24	6.6	9.1		N,M	2-176
	54LS467	−2.6	12	14.5	10	J		†
	74LS467	−5.2	24	14.5	10		N,M	†
	54ALS2541	−12	12	6	10.8	J		2-320
	74ALS2541	−15	24	6	10.8		N,M	2-320
	54ALS541	−12	12	6	10.8	J		2-195
	74ALS541	−15	24	6	10.8		N,M	2-195
Octal Inverter Buffers	54ALS466A	−12	12	4.8	7.5	J		2-176
	74ALS466A	−15	24	4.8	7.5		N,M	2-176
	54LS466	−2.6	12	9.5	8	J		†
	74LS466	−5.2	24	9.5	8		N,M	†
	54ALS468A	−12	12	4.7	7.5	J		2-176
	74ALS468A	−15	24	4.7	7.5		N,M	2-176
	54LS468	−2.6	12	9.5	8	J		†
	74LS468	−5.2	24	9.5	8		N,M	†
	54ALS540	−12	12	6.6	10.8	J		2-192
	74ALS540	−15	24	6.6	10.8		N,M	2-192
	54ALS5620	−12	12	6.6	18.3	J		2-329
	74ALS5620	−15	24	6.6	18.3		N,M	2-329
Quad Inverter Transceivers	54ALS242B	−12	12	5.6	16.3	J		2-133
	74ALS242B	−15	24	5.6	16.3		N,M	2-133
	54AS242	−12	48	3.5	33.8	J		3-76
	74AS242	−15	64	3.5	33.8		N	3-76
Quad Transceivers	54ALS243A	−12	12	6	23.3	J		2-133
	74ALS243A	−15	24	6	23.3		N,M	2-133
	54AS243	−12	48	4	45.8	J		3-76
	74AS243	−15	64	4	45.8		N	3-76
	54LS243	−15	12	12	34.5	J		†
	74LS243	−15	24	12	34.5		N,M	†
Octal Inverter Bus Buffers/ Drivers	54AS231	−12	40	3.5	18.5	J		3-73
	74AS231	−15	48	3.5	18.5		N	3-73
	54ALS240A	−12	12	2.6	6.5	J		2-129
	74ALS240A	−15	24	2.6	6.5		N,WM	2-129
	54AS240	−12	48	3.5	19.2	J		3-76
	74AS240	−15	64	3.5	19.2		N	3-76
	54LS240	−12	12	10	14.2	J		†
	74LS240	−15	24	10	14.2		N,WM	†
	54S240	−12	48	5	56.3	J		†
	74S240	−15	64	5	56.3		N,WM	†
	54S940	−12	48	5	56.3	J		†
	74S940	−15	64	5	56.3		N	†
	54ALS1240A	−12	8	9	5.9	J		2-303
	74ALS1240A	−15	16	9	5.9		N,WM	2-303

† Please see the LS/S/TTL Logic Databook for this datasheet.

Buffer Gates with TRI-STATE® Totem-Pole Outputs (Continued)

Description	Device Type	Max Source Current (mA)	Max Sink Current (mA)	Typ* Prop. Delay Time (ns)	Typ* Power Diss. /Gate (mW)	Package Availability		Page
						Mil	Com	
Octal Bus Buffers/ Drivers	54ALS241A	−12	12	4.3	8.6	J		2-129
	74ALS241A	−15	24	4.3	8.6		N,WM	2-129
	54AS241	−12	48	4	24.6	J		3-76
	74AS241	−15	64	4	24.6		N	3-76
	54LS241	−12	12	10	14.2	J		†
	74LS241	−15	24	10	14.2		N,WM	†
	54S241	−12	48	5	67.2	J		†
	74S241	−15	64	5	67.2		N	†
	54ALS244A	−12	12	4.3	8.5	J		2-137
	74ALS244A	−15	24	4.3	8.5		N,WM	2-137
	54AS244	−12	48	4	24.1	J		3-76
	74AS244	−15	64	4	24.1		N	3-76
	54LS244	−12	12	10	24.6	J		†
	74LS244	−15	24	10	24.6		N,WM	†
	54S244	−12	48	5	67.2	J		†
	74S244	−15	64	5	67.2		N	†
	54S941	−12	48	5	67.2	J		†
	74S941	−15	64	5	67.2		N,WM	†
	54ALS1241A	−12	12	9	5.9	J		2-303
	74ALS1241A	−15	24	9	5.9		N,WM	2-303
	54ALS1244A	−12	12	9	5.9	J		2-311
	74ALS1244A	−15	24	9	5.9		N,WM	2-311
Octal Transceivers	54ALS245A	−12	12	9	21.7	J		2-140
	74ALS245A	−15	24	9	21.7		N,WM	2-140
	54AS245	−12	32	5.5	49.1	J		3-82
	74AS245	−15	48	5.5	49.1		N	3-82
	54LS245	−12	12	8	36.3	J		†
	74LS245	−15	24	8	36.3		N,WM	†
	54ALS645A	−12	12	5	21.7	J		2-232
	74ALS645A	−15	24	5	21.7		N,WM	2-232
	54AS645	−12	48	5.5	49.2	J		3-145
	74AS645	−15	64	5.5	49.2		N	3-145
	54LS645	−12	12	8	36	J		†
	74LS645	−15	24	8	36		N,WM	†
	54ALS1243A	−12	8	7	19	J		2-307
	74ALS1243A	−15	16	7	19		N,WM	2-307
	54ALS1245A	−12	8	9	14	J	N,WM	2-314
	74ALS1245A	−15	16	9	14	J	N,WM	2-314
	54ALS1645A	−12	8	7.5	14.4	J		2-317
	74ALS1645A	−15	16	7.5	14.4		N,WM	2-317

† Please see the LS/S/TTL Logic Databook for this datasheet.

Buffer Gates with TRI-STATE® Totem-Pole Outputs (Continued)

Description	Device Type	Max Source Current (mA)	Max Sink Current (mA)	Typ* Prop. Delay Time (ns)	Typ* Power Diss. /Gate (mW)	Package Availability		Page
						Mil	Com	
Octal Inverter Transceivers	54ALS620A	−12	12	8	14.6	J		2-226
	74ALS620A	−15	24	8	14.6		N,WM	2-226
	54AS620	−12	48	5.5	32.7	J		3-139
	74AS620	−15	64	5.5	32.7		N	3-139
	54ALS640A	−12	12	5	15.4	J		2-229
	74ALS640A	−15	24	5	15.4		N,WM	2-229
	54AS640	−12	48	4	32.9	J		3-142
	74AS640	−15	64	4	32.9		N	3-142
	54ALS1242	−12	12	5	10.9	J		2-307
	74ALS1242	−15	24	5	10.9		N,WM	2-307
Octal Transceivers with True and Inverting Outputs	54AS230	−12	48	3.5	20.8	J		3-73
	74AS230	−15	64	3.5	20.8		N	3-73
Octal Transceivers with Register Storage	54AS646	−12	32	5	93.8	J		3-148
	74AS646	−15	48	5	93.8		N	3-148
	54AS652	−12	32	5	93.8	J		3-153
	74AS652	−15	48	5	93.8		N	3-153
Octal Inverter Transceivers with Register Storage	54AS648	−12	32	6	81.3	J		3-148
	74AS648	−15	48	6	81.3		N	3-148
	54AS651	−12	32	6	81.3	J		3-153
	74AS651	−15	48	6	81.3		N	3-153
Octal Inverting Tranceivers/ MOS Drivers	54/74AS2620	−2	1	4.5	38.3	J	N	3-225
Octal Bus Transceivers/ MOS Drivers	54/74ALS2645A	TBD	TBD	TBD	TBD	J	N,WM	2-323
	54/74AS2645	−2	1	5.5	47	J	N	3-228

Code Converters

Description	Device Type	Typ* Prop. Delay Time (ns)	Typ* Power Diss. Total (mW)	Package Availability		Page
				Mil	Com	
6-Bit Binary to 6-Bit BCD Converters	54/74185A	25	280	J	N	†
	8899	31	350		N	†
6-Bit BCD to 6-Bit Binary or 4-Line to 4-Line BCD 9's/BCD 10's Converters	54/74184	25	280	J	N	†
	8898	31	350		N	†

† Please see the LS/S/TTL Logic Databook for this datasheet.

Comparators

Description	Device Type	Typ* Prop. Delay Time (ns)	Typ* Power Diss. Total (mW)	Package Availability		Page
				Mil	Com	
4-Bit Magnitude Comparator	54/74LS85	20	52	J	N,M	†
	54/7485	21	275	J	N	†
6-Bit Magnitude Comparators	71/8131	20	250	J	N	†
	71/8136	20	250	J	N	†
	71/8160	21	205	J	N	†
8-Bit Identity Comparator	54/74ALS520	13.5	60	J	N,M	2-180
	54/74ALS521	13.5	60	J	N,M	2-180
8-Bit Identity Comparator with Open-Collector Outputs	54/74ALS518	18.2	55	J	N,M	2-180
	54/74ALS519	18	55	J	N,M	2-180
	54/74ALS522	19	45	J	N,M	2-180
	54/74ALS689	11	60	J	N,M	2-247
10-Bit Magnitude Comparators	71/8130	21	240	J	N	†

Counters, Asynchronous (Ripple Clock)/Negative-Edge-Triggered

Description	Device Type	Count Freq. (MHz)	Parallel Load	Clear	Typ* Power Diss. Total (mW)	Package Availability		Page
						Mil	Com	
4-Bit Binary	54/74LS93	32	None	High	39	J	N,M	†
	54/7493A	32	None	High	160	J	N	†
	54/74L93	6	None	High	20	J	N	†
	54/74LS293	32	None	High	45	J	N,M	†
Decade	54/74LS90	32	Set-to-9	High	40	J	N,M	†
	54/7490A	32	Set-to-9	High	160	J	N	†
	54/74LS290	32	None	High	45	J	N,M	†
Dual 4-Bit Decade	54/74LS390	25	None	High	75	J	N,M	†
Dual 4-Bit Binary	54/74LS393	25	None	High	75	J	N,M	†

† Please see the LS/S/TTL Logic Databook for this datasheet.

Counters, Synchronous/Positive-Edge-Triggered

Description	Device Type	Count Freq. (MHz)	Parallel Load	Clear	Typ* Power Diss. Total (mW)	Package Availability		Page
						Mil	Com	
4-Bit Binary	54/74ALS161B	25	Sync	Async-L	60	J	N,M	2-89
	54/74AS161		Sync	Async-L	200	J	N	3-42
	54/74LS161A	25	Sync	Async-L	93	J	N,M	†
	54/74S161	40	Sync	Async-L	475	J	N	†
	54/74161A	25	Sync	Async-L	305	J	N	†
	54/74ALS163B	25	Sync	Sync-L	60	J	N,M	2-89
	54/74AS163		Sync	Sync-L	200	J	N	3-42
	54/74LS163A	25	Sync	Sync-L	93	J	N,M	†
	54/74S163	40	Sync	Sync-L	475	J	N	†
	54/74163A	25	Sync	Sync-L	93	J	N	†
	75/8556	25	Sync	Sync-L	375	J	N	†
	93/8316	25	Sync	Async-L	305	J	N	†
4-Bit Binary Up-Down	54/74ALS169B	25	Sync	None	75	J	N,M	2-106
	54/74AS169		Sync	None	230	J	N	3-49
	54/74LS169A	25	Async	None	100	J	N,M	†
	54/74ALS191	25	Async	None	60	J	N,M	2-115
	54/74LS191	20	Async	None	90	J	N,M	†
	54/74191	20	Async	None	325	J	N	†
	54/74ALS193	25	Async	Async-H	60	J	N,M	2-122
	54/74LS193	25	Async	Async-H	85	J	N,M	†
	54/74193	20	Async	Async-H	325	J	N	†
	75/85L63	6	Async	Async-H	40	J	N	†
Decade	54/74ALS160B	25	Sync	Async-L	60	J	N,M	2-89
	54/74AS160		Sync	Async-L	200	J	N	3-42
	54/74ALS162B	25	Sync	Sync-L	60	J	N,M	2-89
	54/74AS162		Sync	Sync-L	200	J	N	3-42
	54/74162A	25	Sync	Sync-L	305	J	N	†
	93/8310	25	Sync	Async-L	305	J	N	†
Decade Up/Down	54/74ALS168B	25	Sync	None	75	J	N,M	2-106
	54/74AS168A		Sync	None	230	J	N	3-49
	54/74ALS190	20	Async	None	110	J	N,M	2-115
	54/74LS190	20	Async	None	100	J	N,M	†
	54/74ALS192	20	Async	Async-H	60	J	N,M	2-122
	75/85L60	6	Async	Async-H	40	J	N	†

† Please see the LS/S/TTL Logic Databook for this datasheet.

Data Selectors/Multiplexers

Description	Device Type	Type of Output	Data Inver. Output	Typ* Prop. Delay Time (ns)		Typ* Power Diss. Total (mW)	Package Availability		Page
				Data to Out	From Enable		Mil	Com	
Quad 2 to 1 Line	54/74ALS157	Standard	N/A	4.3	6.3	39	J	N,M	2-86
	54/74AS157	Standard	N/A	3.5	5.5	95	J	N	3-38
	54/74LS157	Standard	N/A	9	14	49	J	N,M	†
	54/74S157	Standard	N/A	5	8	250	J	N	†
	54/74157	Standard	N/A	9	14	150	J	N	†
	54/74ALS257	TRI-STATE	N/A	4.2	6	33	J	N,M	2-150
	54/74AS257	TRI-STATE	N/A	3.5	4	83	J	N	3-84
	54/74LS257B	TRI-STATE	N/A	12	12	50	J	N,M	†
	54/74S257	TRI-STATE	N/A	5	41	320	J	N	†
	93/8322	Standard	N/A	9	14	150	J	N	†
	71/8123	TRI-STATE	N/A	9.5	N/A	200	J	N	†
Quad 2 to 1 Line (Inverting)	54/74ALS158	Standard	4.2	N/A	6.1	11.5	J	N,M	2-86
	54/74AS158	Standard	2.5	N/A	4	78	J	N	3-38
	54/74LS158	Standard	7	N/A	12	24	J	N,M	†
	54/74S158	Standard	4	N/A	7	195	J	N	†
	54/74ALS258	TRI-STATE	4.2	N/A	6	29.2	J	N,M	2-150
	54/73AS258	TRI-STATE	3	N/A	4.5	58.5	J	N	3-84
	54/74LS258B	TRI-STATE	12	N/A	12	35	J	N,M	†
	54/74S258	TRI-STATE	4	N/A	14	280	J	N	†
Dual 4 to 1 Line	54/74ALS153	Standard	N/A	16.5	14.5	37.5	J	N,M	2-83
	54/74LS153	Standard	N/A	14	22	31	J	N,M	†
	54/74S153	Standard	N/A	6	9.5	225	J	N	†
	54/74153	Standard	N/A	10.5	20	170	J	N	†
	54/74ALS253	TRI-STATE	N/A	8	4.5	35	J	N,M	2-147
	54/74LS253	TRI-STATE	N/A	15	25	38	J	N,M	†
	54/74S253	TRI-STATE	N/A	6	12	275	J	N	†
	93/8309	Standard	12	20	20	135	J	N	†
Dual 4 to 1 Line (Inverting)	54/74ALS352	Standard	6		4.5	32.5	J	N,M	2-158
	54/74LS352	Standard	15	N/A	18	31	J	N,M	†
	54/74ALS353	TRI-STATE	6	N/A	4.5	37.5	J	N,M	2-161
8 to 1 Line	54/74ALS151	Standard	9.3	7.8	11	37.5	J	N,M	2-79
	54/74S151	Standard	4.5	8	9	225	J	N	†
	54/74151A	Standard	8	16	22	145	J	N	†
	54/74ALS251	TRI-STATE	9.4	7.6	7	47	J	N,M	2-143
	54/74LS251	TRI-STATE	17	21	21	35	J	N,M	†
	54/74S251	TRI-STATE	4.5	8	14	275	J	N	†
	93/8312	Standard	9	16	17	135	J	N	†
16 to 1 Line	54/74150	Standard	11	N/A	18	200	J	N	†

† Please see the LS/S/TTL Logic Databook for this datasheet.

Decoders/Demultiplexers

Description	Device Type	Type of Output	Typ* Select Time (ns)	Typ* Enable Time (ns)	Typ* Power Diss. Total (mW)	Package Availability		Page
						Mil	Com	
Dual 2 to 4 Line	54/74LS139	Totem	22	19	34	J	N,M	†
	54/74S139	Totem	7.5	6	300	J	N	†
	54/74LS155	Totem	18	15	30	J	N,M	†
	54/74155	Totem	21	16	250	J	N	†
	54/74LS156	Open-Collector	33	26	31	J	N,M	†
3 to 8 Line	54/74ALS138	Totem	8.5	9	25	J	N,M	2-76
	54/74LS138	Totem	22	21	31	J	N,M	†
	54/74S138	Totem	8	7	225	J	N	†
3 to 8 Line Decoder with Address Register	54/74ALS131	Totem	8.5	10	25	J	N,M	2-64
3 to 8 Line Decoder with Address Latch	54/74ALS137	Totem	11	10	25	J	N,M	2-73
4 to 10 Line	54/74LS42	Totem	17	N/A	35	J	N,M	†
BCD to	54/7442	Totem	17	N/A	140	J	N	†
Decimal	93/8301	Totem	20	N/A	125	J	N	†
4 to 16 Line	54/74LS154	Totem	23	19	45	J	N,WM	†
	54/74154	Totem	19.5	17.5	170	J	N	†
	93/8311	Totem	19.5	17.5	170	J	N	†
1 of 10 Decoder	93/8301	Totem	19.5	N/A	125	J	N	†

Decoder/Drivers, Display

Description	Device Type	Output Sink Current (mA)	Off-State Output Voltage (V)	Typ* Power Diss. Total (mW)	Blanking	Package Availability		Page
						Mil	Com	
BCD to	54/7446A	40	30	320	Ripple	J	N	†
7-Segment	54/7447A	40	15	320	Ripple	J	N	†
Decoder/Drivers								
BCD to	54/7442	16	5.5	140	Invalid	J	N	†
Decimal	54/7445	80	30	215	Invalid	J	N	†
Decoder/	54/74141	7	60	80	Invalid	J	N	†
Driver	54/74145	80	15	215	Invalid	J	N	†
Nixie Driver	54/7441A	7	70	105	None	J	N	†

Flip-Flops, Gated

Device Type	Clear	Preset	Typ* f_{MAX} (MHz)	Data Setup Time (ns)	Data Hold Time (ns)	Typ* Power Diss. /FF (mW)	Package Availability		Page
							Mil	Com	
54/74L72	Yes	Yes	20	0	0	3.8	J	N	†

† Please see the LS/S/TTL Logic Databook for this datasheet.

Flip-Flops, Single and Dual J-K Edge Triggered

Device Type	Clear	Preset	Typ* f_{MAX} (MHz)	Data Setup Time (ns)	Data Hold Time (ns)	Typ* Power Diss. /FF (mW)	Package Availability		Page
							Mil	Com	
54/74LS73A	Yes	No	45	25	5	10	J	N,M	†
54/74LS107A	Yes	No	45	20	0	10	J	N,M	†
54/74ALS109A	Yes	Yes	50	15	0	6	J	N,M	2-61
54/74AS109	Yes	Yes	125	3	1	28.8	J	N	3-33
54/74LS109A	Yes	Yes	33	25	0	10	J	N,M	†
54/74109	Yes	Yes	33	10	6	45	J	N	†
54/74LS112A	Yes	Yes	45	20	0	10	J	N,M	†
54/74S112	Yes	Yes	125	6	0	75	J	N	†
54/74S113	No	Yes	125	6	0	75	J	N	†
90/8024	Yes	Yes	40	15	10	45	J	N	†

Flip-Flops, Dual D Edge Triggered with Preset and Clear

Device Type	Typ* f_{MAX} (MHz)	Data Setup Time (ns)	Data Hold Time (ns)	Typ* Power Diss. /FF (mW)	Package Availability		Page
					Mil	Com	
54/74ALS74A	30	15	0	6	J	N,M	2-56
54/74AS74	125	2	1	26.3	J	N	3-28
54/74LS74A	33	20	0	10	J	N,M	†
54/74S74	110	3	2	75	J	N	†
54/7474	25	20	5	43	J	N,M	†
54/74L74	6	50	15	4	J	N	†

Flip-Flop, Octal D Edge Triggered with TRI-STATE Outputs

Device Type	Typ* f_{MAX} (MHz)	Data Setup Time (ns)	Data Hold Time (ns)	Typ* Power Diss. /FF (mW)	Package Availability		Page
					Mil	Com	
54/74ALS374	50	10	4	10.8	J	N,WM	2-168
54/74AS374	200	3	3	50.3	J	N	3-110
54/74LS374	50	20	0	15.9	J	N,WM	†
54/74S374	100	5	2	60.9	J	N	†
54/74ALS534	50	10	0	10.4	J	N,WM	2-188
54/74AS534	200	3	2	50.3	J	N	3-117
54/74ALS564A	50	15	4	8.5	J	N,WM	2-202
54/74ALS574A	50	15	4	8.5	J	N,WM	2-210
54/74AS574	200	3	3	50.4	J	N	3-124
54/74AS575	160	3	3	53	J	N	3-127
54/74ALS576A	50	15	4	8.5	J	N,WM	2-214
54/74AS576	160	3	3	52.5	J	N	3-130
54/74AS577	160	3	3	50.4	J	N	3-133
54/74ALS874B	50	15	4	10.8	J	N,WM	2-267
54/74AS874	160	2.5	1	62.5	J	N	3-176
54/74ALS876A	50	15	4	10.8	J	N,WM	2-271
54/74AS876	160	2.5	1	58	J	N	3-180
54/74AS878	160	3	3	62.5	J	N	3-183
54/74AS879	160	3	3	59	J	N	3-186

† Please see the LS/S/TTL Logic Databook for this datasheet.

Flip-Flops, Single and Dual, Pulse Triggered

Device Type	Clear	Preset	Typ* f_{MAX} (MHz)	Data Setup Time (ns)	Data Hold Time (ns)	Typ* Power Diss. /FF (mW)	Package Availability		Page
							Mil	Com	
54/7473	No	Yes	35	0	0	50.0	J	N	†
54/74L73	No	Yes	11	0	0	3.8	J	N	†
54/7476	Yes	Yes	20	0	0	50.0	J	N	†
54/74107	No	Yes	20	0	0	50.0	J	N	†

Gates, AND with Totem-Pole Outputs

Description	Device Type	Typ* Prop. Delay Time (ns)	Typ* Power Diss. /Gate (mW)	Package Availability		Page
				Mil	Com	
Dual 4-Input	54/74ALS21A	9	2.2	J	N,M	2-36
	54/74AS21	3.3	12.5	J	N	3-18
	54/74LS21	7.8	4.5	J	N,M	†
Triple 3-Input	54/74ALS11A	9	2.1	J	N,M	2-23
	54/74AS11	3.3	12.9	J	N	3-14
	54/74LS11	7.8	4.3	J	N,M	†
	54/74S11	4.8	31	J	N	†
Quad 2-Input	54/74ALS08	6.5	2.2	J	N,M	2-17
	54/74AS08	3.3	12.9	J	N	3-10
	54/74LS08	7.8	4.3	J	N,M	†
	54/74S08	4.8	31	J	N	†
	54/7408	15	19	J	N	†

Gates, AND with Open-Collector Outputs

Description	Device Type	Typ* Prop. Delay Time (ns)	Typ* Power Diss. /Gate (mW)	Package Availability		Page
				Mil	Com	
Triple 3-Input	54/74ALS15A	17	1.5	J	N,M	2-32
Quad 2-Input	54/74ALS09	17	2.2	J	N,M	2-19
	54/74LS09	19	4.3	J	N,M	†
	54/74S09	6.5	31	J	N	†
	54/7409	18.5	19.4	J	N	†

Gates, AND-OR-INVERT with Totem-Pole Outputs

Description	Device Type	Typ* Prop. Delay Time (ns)	Typ* Power Diss. /Gate (mW)	Package Availability		Page
				Mil	Com	
Dual 2-Wide 2-Input	54/74LS51	7.5	2.75	J	N,M	†
	54/74S51	3.5	28	J	N	†
4-Wide 4-2-3-2 Input	54/74S64	3.5	29	J	N	†

† Please see the LS/S/TTL Logic Databook for this datasheet.

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Gates, NAND and Inverters with Open-Collector Outputs

Description	Device Type	Typ* Prop. Delay Time (ns)	Typ* Power Diss. /Gate (mW)	Package Availability		Page
				Mil	Com	
Dual 4-Input NAND Gates	54/74ALS22B	19	1.3	J	N,M	2-38
Triple 3-Input NAND Gates	54/74ALS12A	18	1.3	J	N,M	2-25
	54/74LS12	21	2	J	N,M	†
Quad 2-Input NAND Gates	54/74ALS01	17	1.3	J	N,M	2-7
	54/7401	32	10	J	N	†
	54/74ALS03B	17	1.3	J	N,M	2-11
	54/74LS03	22	2	J	N,M	†
	54/74S03	7	17.5	J	N	†
	54/7403	10	22	J	N	†
Hex Inverters	54/74ALS05A	18	1.5	J	N,M	2-15
	54/74LS05	21	2	J	N,M	†
	54/74S05	7	17.5	J	N,M	†
	54/7405	22	10	J	N	†

Gates, NAND and Inverters with Totem-Pole Outputs

Description	Device Type	Typ* Prop. Delay Time (ns)	Typ* Power Diss. /Gate (mW)	Package Availability		Page
				Mil	Com	
Dual 4-Input NAND Gates	54/74ALS20A	6.5	1.3	J	N,M	2-34
	54/74AS20	2	8.7	J	N	3-16
	54/74LS20	8	2	J	N,M	†
	54/74S20	4.5	19	J	N	†
	54/7420	10	10	J	N	†
	54/74L20	33	1	J	N	†
Triple 3-Input NAND Gates	54/74ALS10A	7	1.3	J	N,M	2-21
	54/74AS10	2	14	J	N	3-12
	54/74LS10	8	2	J	N,M	†
	54/74S10	4.5	19	J	N	†
	54/7410	10	10	J	N	†
	54/74L10	33	1	J	N	†
Quad 2-Input NAND Gates	54/74ALS00A	3.5	1.25	J	N,M	2-5
	54/74AS00	2	8	J	N	3-4
	54/74LS00	8	2	J	N,M	†
	54/74S00	4.5	19	J	N,M	†
	54/7400	10	10	J	N	†
	54/74L00	33	1	J	N	†
	9002C	10	11	J	N	†

† Please see the LS/S/TTL Logic Databook for this datasheet.

Gates, NAND and Inverters with Totem-Pole Outputs (Continued)

Description	Device Type	Typ* Prop. Delay Time (ns)	Typ* Power Diss. /Gate (mW)	Package Availability		Page
				Mil	Com	
Hex Inverters	54/74ALS04B	3.5	1.5	J	N,M	2-13
	54/74AS04	2	7.1	J	N	3-8
	54/74LS04	8	2	J	N,M	†
	54/74S04	4.5	19	J	N,M	†
	54/7404	10	10	J	N,M	†
	54/74L04	33	1	J	N	†
	54/74ALS14	8	10	J	N,M	2-29
8-Input NAND Gates	54/74ALS30A	6.5	1.9	J	N,M	2-44
	54/74AS30	2	9.8	J	N	3-22
	54/74LS30	10	2.4	J	N,M	†
	54/74S30	4.5	19	J	N	†
	54/7420	10	10	J	N	†
13-Input NAND Gate	54/74ALS133	7	2	J	N,M	2-69
	54/74S133	6	19	J	N,M	†
Hex Non-Inverter	54/74AS34	4.5	12	J	N	3-26

Gates, Exclusive NOR, OR with Open-Collector Outputs

Description	Device Type	Typ* Prop. Delay Time (ns)	Typ* Power Diss. /Gate (mW)	Package Availability		Page
				Mil	Com	
Quad 2-Input Exclusive NOR Gates	54/74ALS811		9.1	J	N,M	2-259
	54/74AS811			J	N	3-168
Quad 2-Input Exclusive OR Gates	54/74ALS136			J	N,M	2-71
	54/74AS136			J	N	3-36

Gates, Exclusive NOR with Totem-Pole Outputs

Description	Device Type	Typ* Prop. Delay Time (ns)	Typ* Power Diss. /Gate (mW)	Package Availability		Page
				Mil	Com	
Quad 2-Input Exclusive NOR Gates	54/74ALS810	N/A	N/A	J	N,M	2-256
	54/74AS810	N/A	N/A	J	N	3-165

Gates, NOR with Totem-Pole Outputs

Description	Device Type	Typ* Prop. Delay Time (ns)	Typ* Power Diss. /Gate (mW)	Package Availability		Page
				Mil	Com	
Triple 3-Input NOR Gates	54/74ALS27	5.5	2.5	J	N,M	2-40
	54/74AS27	2	12.2	J	N	3-20
	54/74LS27	10	4.5	J	N,M	†
	54/7427	8.5	22	J	N	†
Quad 2-Input NOR Gates	54/74ALS02	5	1.9	J	N,M	2-9
	54/74AS02	2	10.1	J	N	3-6
	54/74LS02	10	2.75	J	N,M	†
	54/74S02	5	29	J	N	†
	54/7402	10	14	J	N	†
	54/74L02	33	1.5	J	N	†

† Please see the LS/S/TTL Logic Databook for this datasheet.

Gates, OR with Totem-Pole Outputs

Description	Device Type	Typ* Prop. Delay Time (ns)	Typ* Power Diss. /Gate (mW)	Package Availability		Page
				Mil	Com	
Quad 2-Input OR Gates	54/74ALS32	5.5	2.8	J	N,M	2-46
	54/74AS32	3.5	14.9	J	N	3-24
	54/74LS32	10	5	J	N,M	†
	54/74S32	5	35	J	N	†
	54/7432	12	24	J	N	†
Quad 2-Input Exclusive OR Gates	54/74ALS86	7	3.75	J	N,M	2-59
	54/74AS86			J	N	3-31
	54/74LS86	10	7.5	J	N,M	†
	54/74S86	9	62.5	J	N	†
	54/7486	14	41	J	N	†

Latches

Description	Device Type	No. of Bits	Clear	Outputs	Typ.* Prop. Delay Time (ns)	Typ* Power Diss. Total (mW)	Package Availability		Page
							Mil	Com	
Addressable Latches	54/74LS259	8	Low	Q	17	110	J	N,WM	†
	54/74259	8	Low	Q	21	150	J	N	†
	93/8334	8	Low	Q	21	280	J	N	†
DG (Clocked) Latches	54/74LS75	4	None	Q,$\overline{Q}$	11	32	J	N,M	†
	54/7475	4	None	Q,$\overline{Q}$	15	160	J	N	†
$\overline{S}$,$\overline{R}$ Latches	54/74LS279	4	None	Q	12	19	J	N,M	†
Dual 4-Bit Latches	54/74ALS880A	4	None	$\overline{Q}$	9	88.3	J	N,M	2-275
	54/74AS880	4	None	$\overline{Q}$	6	391.5	J	N	3-189
Octal Latch	54/74ALS273	8	Low	Q	12	50	J	N,M	2-154
TRI-STATE Octal Latches	54/74ALS373	8	None	Q	10	70	J	N,WM	2-164
	54/74AS373	8	None	Q	6	300	J	N	3-107
	54/74LS373	8	None	Q	17	120	J	N,WM	†
	54/74S373	8	None	Q	12	525	J	N,WM	†
	54/74ALS573B	8	None	Q	9	68.3	J	N,WM	2-206
	54/74AS573	8	None	Q	4.5	293	J	N	3-120
TRI-STATE Inverting Octal Latches	54/74ALS533	8	None	$\overline{Q}$	10	75.8	J	N,WM	2-184
	54/74AS533	8	None	$\overline{Q}$	5	328	J	N	3-114
	54/74ALS563A	8	None	$\overline{Q}$	13	68.3	J	N,WM	2-198
	54/74ALS580A	8	None	$\overline{Q}$	9	68.3	J	N,WM	2-218
	54/74AS580	8	None	$\overline{Q}$	4.5	330	J	N	3-136
Dual 4-Bit TRI-STATE Latches	54/74ALS873B	4	Low	Q	10	68.3	J	N,WM	2-236
	54/74AS873	4	Low	Q	4.5	330	J	N	3-172

† Please see the LS/S/TTL Logic Databook for this datasheet.

Line Drivers

Description	Device Type	Low-Level Output Current (mA)	High-Level Output Current (mA)	Typ* Prop. Delay Time (ns)	Typ* Power Diss. /Gate (mW)	Package Availability		Page
						Mil	Com	
Dual 4-Input NAND	54/74S140	60	−40	4	43.8	J	N	†
Hex 2-Input NAND	54ALS804A	12	−1	2.7	3.3	J		2-250
	74ALS804A	24	−2.6	2.7	3.3		N,M	2-250
	54AS804B	40	−40	2	7.7	J		3-159
	74AS804B	48	−48	2	7.7		N	3-159
	54AS1804	40	−40	2	7.7	J		3-217
	74AS1804	48	−48	2	7.7		N	3-217
Hex 2-Input NOR	54ALS805A	12	−12	3	4.1	J		2-252
	74ALS805A	24	−15	3	4.1		N,M	2-252
	54AS805B	40	−40	1.6	9.6	J		3-161
	74AS805B	48	−48	1.6	9.6		N	3-161
	54AS1805	40	−40	1.6	9.6	J		3-219
	74AS1805	48	−48	1.6	9.6		N	3-219
Hex 2-Input AND	54ALS808A	12	−12	4.3	4.6	J		2-254
	74ALS808A	24	−15	4.3	4.6		N,M	2-254
	54AS808B	40	−40	3	10.6	J		3-163
	74AS808B	48	−48	3	10.6		N	3-163
	54AS1808	40	−40	3	10.6	J		3-221
	74AS1808	48	−48	3	10.6		N	3-221
Hex 2-Input OR	54ALS832A	12	−12	4	5.6	J		2-261
	74ALS832A	24	−15	4	5.6		N,M	2-261
	54AS832B	40	−40	2.5	12.9	J		3-170
	74AS832B	48	−48	2.5	12.9		N	3-170
	54AS1832	40	−40	2.5	12.9	J		3-223
	74AS1832	48	−48	2.5	12.9		N	3-223

Multipliers

Description	Device Type	Package Availability		Page
		Mil	Com	
4-Bit by 4-Bit Parallel Binary Multipliers	78/8875A	J	N	†
	78/8875B	J	N	†

† Please see the LS/S/TTL Logic Databook for this datasheet.

One Shots, Retriggerable

Description	Device Type	No. of Inputs		Dir. Clear	Output Pulse Range (ns)	Typ* Total Power Diss. (mW)	Package Availability		Page
		Pos	Neg				Mil	Com	
Single	54/74LS122	2	2	Yes	45 ns–inf.	30	J	N,M	†
	96/8601	2	2	Yes	50 ns–inf.	90	J	N	†
Dual	54/74LS123	1	1	Yes	90 ns–inf.	60	J	N,M	†
	54/74123	1	1	Yes	45 ns–inf.	230	J	N	†
	96/8602	1	1	Yes	72 ns–inf.	195	J	N	†

One Shots with Schmitt-Trigger Inputs

Description	Device Type	No. of Inputs		Dir. Clear	Output Pulse Range (ns)	Typ* Total Power Diss. (mW)	Package Availability		Page
		Pos	Neg				Mil	Com	
Single	54/74121	1	2	Yes	40 ns–28s	90	J	N	†
Dual	54LS221	1	1	Yes	20 ns–49s	65	J		†
	74LS221	1	1		20 ns–49s	23		N,M	†

Parity Generators/Checkers

Description	Device Type	Typ* Prop. Delay Time (ns)	Typ* Power Diss. Total (mW)	Package Availability		Page
				Mil	Com	
8-Bit Odd/Even Parity Generators/Checkers	54/74180	35	170	J	N	†
9-Bit Odd/Even Parity Generators/Checkers	54/74S280	13	335	J	N,M	†
	54/74AS280	7.3	135	J	N	3-93
9-Bit Parity Generator/Checker with Bus Driver Parity I/O Port	54/74AS286	9.3	160	J	N	3-102

Priority Encoders

Description	Device Type	Typ* Prop. Delay Time (ns)	Typ* Power Diss. Total (mW)	Package Availability		Page
				Mil	Com	
Cascadable Octal Priority Encoders	54/74148	12	190	J	N	†
	93/8318	12	190	J	N	†

Register Files

Description	Device Type	Typ* Address Time (ns)	Typ* Read Enable Time (ns)	Data Input Rate (MHz)	Typ* Power Diss. Total (mW)	Package Availability		Page
						Mil	Com	
4 Words of 4 Bits with TRI-STATE Outputs	54/74LS670	24	19	20	135	J	N,M	†

† Please see the LS/S/TTL Logic Databook for this datasheet.

Registers, Other

Description	Device Type	Typ* Clock Freq. (MHz)	Asyn. Clear	Typ* Power Diss. Total (mW)	Package Availability		Page
					Mil	Com	
Quad Bus Buffer Registers	54/74LS173A	40	High	85	J	N,M	†
	54/74173	30	High	250	J	N	†
Quad D-Type Registers	54/74ALS175	60	Low	47.5	J	N,M	2-111
	54/74AS175A	160	Low	395	J	N	3-57
	54/74LS175	40	Low	55	J	N,M	†
	54/74S175	90	Low	300	J	N	†
	54/74175	40	Low	150	J	N	†
Quad Multi-plexers with Storage	54/74L98	15	None	30	J	N	†
Hex D-Type Registers	54/74ALS174	60	Low	50	J	N,M	2-111
	54/74AS174	160	Low	395	J	N	3-54
	54/74LS174	40	Low	80	J	N,M	†
	54/74S174	90	Low	450	J	N	†
	54/74174	40	Low	225	J	N	†
8-Bit Universal Shift/Storage Registers	54/74S299	60	Low	700	J	N	†
Octal D-Type Registers	54/74ALS374	50	None	86	J	N,WM	2-168
	54/74AS374	200	None	402	J	N	3-110
	54/74LS374	50	None	128	J	N,WM	†
	54/74S374	100	None	487	J	N,WM	†
	54/74ALS534	50	None	83	J	N,WM	2-188
	54/74AS534	200	None	328	J	N	3-117
	54/74ALS574A	40	None	68	J	N,WM	2-210
	54/74AS574	160	None	403	J	N	3-124
	54/74AS575	160	None	383	J	N	3-127
	54/74ALS576A	50	None	68	J	N,WM	2-214
	54/74AS576	160	None	420	J	N	3-130
	54/74AS577	160	None	420	J	N	3-133
	54/74ALS874B	50	Low	87	J	N,WM	2-267
	54/74AS874	160	Low	500	J	N	3-176
	54/74ALS876A	50	None	87	J	N,WM	2-271
	54/74AS876	160	None	500	J	N	3-180
	54/74AS878	160	Low	500	J	N	3-183
	54/74AS879	160	Low	500	J	N	3-186
8-Bit Dual Rank Shift Register	54/74LS952	36	None	305	J	N,M	†
	54/74LS962	36	None	305	J	N,M	†
Successive Approximation Registers	2502C	21	None	325	J	N	†
	2503C	21	None	300	J	N	†
	2504C	21	None	450	J	N	†
Octal Bus Transceivers And 8-Bit Storage Register	54/74ALS646	40	None	255	J	N,WM	2-235
	54/74ALS648	40	None	260	J	N,WM	2-239
	54/74ALS652	40	None	255	J	N,WM	2-243

† Please see the LS/S/TTL Logic Databook for this datasheet.

Registers, Shift

Description	Device Type	No. of Bits	Typ* Shift Freq. (MHz)	Ser. Data Input	Asyn. Clear	Modes				Typ* Power Diss. Total (mW)	Package Availability		Page
						S-R	S-L	Load	Hold		Mil	Com	
Parallel-In Parallel-Out (Bidirectional)	54/74LS194A	4	25	D	Low	x	x	x	x	75	J	N,M	†
	54/74S194	4	90	D	Low	x	x	x	x	450	J	N	†
	54/74194	4	36	D	Low	x	x	x	x	195	J	N	†
Parallel-In Parallel-Out	54/7495	4	36	D	None	x	x	x	x	195	J	N	†
	54/74L95	4	14	D	None	x	x	x	x	24	J	N	†
	54/74LS195A	4	39	J-$\overline{K}$	Low	x		x		70	J	N,M	†
	54/74S195	4	90	J-$\overline{K}$	Low	x		x		375	J	N	†
	93/8300	4	39	J-$\overline{K}$	Low	x		x	x	356	J	N	†
Parallel-In Serial-Out	76/86L90	8	14	D	None	x		x	x	30	J	N	†
	54/74LS165	8	30	D	None	x		x	x	125	J	N,WM	†
	54/74ALS165	8	60	D	None	x		x	x	80	J	N,WM	2-97
	54/74LS166	8	35	D	Low	x		x	x	110	J	N,WM	†
	54/74166	8	35	D	Low	x		x	x	360	J	N	†
	54/74ALS166	8	60	D	Low	x		x	x	80	J	N,WM	2-102
Serial-In Parallel-Out	54/74LS164	8	36	Gated D	Low	x				80	J	N,M	†
	54/74164	8	36	Gated D	Low	x				175	J	N	†

Schmitt-Triggers with Totem-Pole Outputs

Description	Device Type	Typ* Prop. Delay Time (ns)	Typ.* Hysteresis (V)	Package Availability		Page
				Mil	Com	
Dual 4-Input NAND Schmitt Triggers	54/74ALS13		0.8	J	N,M	2-27
Quad 2-Input NAND Schmitt Triggers	54/74LS132	15	0.8	J	N,M	†
	54/74132	15	0.8	J	N	†
	54/74ALS132		0.8	J	N,M	2-67
Hex Schmitt Trigger Inverters	54/74LS14	15	0.8	J	N,M	†
	54/7414	15	0.8	J	N	†
	54/74ALS14		0.8	J	N,M	2-29

† Please see the LS/S/TTL Logic Databook for this datasheet.

Glossary of Terms

DC Operating Conditions and Characteristics

GENERAL DEFINITIONS

I: Current is the flow of electric charge from one potential to another through a conductor. The unit of measure is the Ampere, or Amp, abbreviated A. One Amp is equal to the current flowing through one ohm of resistance when one volt is applied across that resistance. Common units found in the semiconductor industry are the milliampere, abbreviated mA, equal to 0.001A and the microampere, abbreviated μA, equal to 0.000001A. Negative current is defined as current flowing out of a device terminal and positive current is defined as current flowing into a device terminal.

V: Voltage, or the electromotive force which causes current to flow through a conductor. One Ampere of current flowing through one ohm of resistance develops a potential difference of one volt across that resistance. The unit of measure is the Volt, abbreviated V, and a common unit is the millivolt, abbreviated mV, equal to 0.001V.

INPUT CURRENT PARAMETERS

I_I Maximum High Level Input Current: Current flowing into an input when that input has the maximum voltage specified for the family applied to it. This test is used to guarantee the minimum reverse breakdown voltage of the input structure.

I_{IH} High Level Input Current: The current flowing into an input when that input has a high level voltage equal to the minimum high level output voltage specified for the family. This test is used to check the emitter-to-emitter leakage and the inverse transistor action of a multi-emitter transistor input, the input leakage of a diode, PNP transistor, or C-B short type of input, and to guarantee the fan-in specified for the family.

I_{IK} Input Clamp Current: The current flowing out of an input when that input is pulled below ground. This test is used to guarantee the integrity of the input clamp diode. The input clamp diode is used to limit the voltage swings on the input by clamping the negative excursions to a level equal to one diode drop below ground. This serves to reduce ringing on an incoming signal. Pulling the input below ground for an extended length of time can cause parasitic transistor action to occur between adjacent tanks on the die which can cause erroneous data to occur on the outputs of the device. To prevent this, voltages on the inputs during operation (other than high speed ringing) should be limited to no more than 0.5V below ground at all times.

I_{IL} Low Level Input Current: The current flowing out of an input when a low level voltage equal to the maximum low level output voltage specified for the family is applied to the input. This test is used to check the input pullup resistor on an MET or a diode input and to guarantee the specified fan-in of the family.

I_T+ Current at Positive-Going Threshold Point: The current flowing out of a transition-operated (Schmitt trigger) input when a voltage equal to the positive going threshold voltage is applied to the input.

I_T- Current at Negative-Going Threshold Point: The current flowing out of a transition-operated (Schmitt trigger) input when a voltage equal to the negative going threshold voltage is applied to the input.

OUTPUT CURRENT PARAMETERS

I_{CEX} Output Leakage Current: The current flowing into an open collector output when input conditions have been applied that, according to the product specification, will cause the output to be in the logic high state. This test checks the reverse breakdown of the output transistor.

I_O(off) Off-State Output Current: The current flowing into an output with input conditions applied that, according to the product specification, will cause the output switching element to be in the off state.

NOTE: This parameter is usually specified for open collector outputs intended to drive devices other than logic circuits, such as displays. Any leakage current applied to a display may cuase the display to be activated.

I_{OH} High Level Output Current: The current flowing out of an output with input conditions applied that, according to the product specification, will establish a logic high level at the output. This test guarantees the current sourcing (drive) capability of the output and the fan-out specified for the family.

I_{OL} Low Level Output Current: The current flowing into an output with input conditions applied that, according to the product specification, will establish a logic low level at the output. This test guarantees the current sinking capability of the output and the fan-out specified for the family.

I_{OS} Output Short-Circuit Current: The current out of an output when that output is shorted to ground, or another specified potential, with input conditions applied that, according to the product specification, will establish a logic high level at the output.

I_{OZ} High-Impedance State Output Current: These tests guarantee that the device will not excessively load a bus line when the device output is put into the TRI-STATE® mode.

I_{OZH} (or I_{SINK}): The current flowing into an output with input conditions applied to the output control pin such that the output is in the high impedance state and input conditions applied to the other inputs that, according to the product specification, will establish a logic low level at the output.

I_{OZL}(or I_{SOURCE}): The current flowing out of an output with input conditions applied to the output control pin such that the output is in the high impedance state and input conditions applied to the other inputs that, according to the product specification, will establish a logic high level at the output.

SUPPLY CURRENT PARAMETERS

I_{CCH} Supply Current (outputs in the high state): The current flowing into the V_{CC} terminal of a device with input conditions applied that, according to the product specification, will establish a logic high level at the output(s).

I_{CCL} Supply Current (outputs in the low state): The current flowing into the V_{CC} terminal of a device with input conditions applied that, according to the product specification, will establish a logic low level at the output(s).

DC Operating Conditions and Characteristics (Continued)

I_{CCZ} Supply Current (outputs in the high-impedance state): The current flowing into the V_{CC} terminal of a device with input conditions applied that, according to the product specification, will establish a high impedance state at the output.

INPUT VOLTAGE PARAMETERS

BV_{IN} Input Breakdown Voltage: The maximum voltage that the device is guaranteed to be able to withstand without exceeding the maximum input current specification.

V_F Input Forward Voltage: The voltage applied to the input of a device that causes the input structure to become forward biased; usually equal to the maximum output low voltage specified for the family.

V_{IH} High Level Input Voltage: The minimum positive voltage level that can be applied to an input terminal of a device and be recognized as a logic high level.

V_{IK} Input Clamp Voltage: The input clamp voltage specification checks the quality of the input diode whose purpose is to damp out ringing. This is not intended to be an operating condition and if this voltage is allowed to persist for any length of time, parasitic transistor action will occur between adjacent geometry tanks and circuit performance will be degraded, in some cases to the point of failure.

V_{IL} Low Level Input Voltage: The maximum positive voltage level that can be applied to an input terminal of a device and be recognized as a logic low level.

V_R Input Reverse Voltage: The voltage applied to an input of a device that causes the input structure to become reverse biased; usually equal to the minimum high level output voltage specified for the family.

V_T+ Positive-Going Threshold Voltage: The voltage level at a transition-operated (Schmitt trigger) input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V_T-.

V_T- Negative-Going Threshold Voltage: The voltage level at a transition-operated (Schmitt trigger) input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V_T+.

OUTPUT VOLTAGE PARAMETERS

V_{OH} High Level Output Voltage: The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a high level at the output.

V_{OL} Low Level Output Voltage: The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a low level at the output.

V_O(off) Off-State Output Voltage: The voltage at an output terminal with input conditions applied that, according to the product specification, will cause the output switching element to be in the off state.

NOTE: This characteristic is usually specified only for outputs without internal pull-up elements intended for driving devices other than logic circuits.

V_O(on) On-State Output Voltage: The voltage at an output terminal with input conditions applied that, according to the product specification, will cause the output switching element to be in the on state.

NOTE: This characteristic is usually specified only for outputs without internal pull-up elements intended for driving devices other than logic circuits.

AC Operating Conditions and Characteristics

INPUT PARAMETERS

f_{MAX} Maximum Clock Frequency: The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic levels at the output with input conditions established that should cause changes of output logic level in accordance with the specification. Unless otherwise specified, this test is performed with no restrictions on input rise and fall times or duty cycle.

NOTE: A minimum value is specified that is the highest frequency at which all devices are guaranteed to function correctly.

t_H Hold Time: The interval during which a signal must be maintained at a given data input after an active transition at another given input.

NOTE: A minimum value is specified that is the smallest time interval above which all devices are guaranteed to function correctly.

t_W Pulse Width: The time interval between specified voltage reference points on the leading and trailing edges of a pulse waveform.

NOTE: A minimum value is specified that is the smallest time interval at which correct operation of the logic element is guaranteed.

t_{REC} Recovery Time: The time interval needed to switch a memory-type device from a write mode to a read mode and to obtain valid data signals at the output.

NOTE: A minimum value is specified that is the smallest time interval at which correct operation of the device is guaranteed.

t_{REL} Release Time: The time interval between one control input going inactive and another input going active after which the inactive input no longer has any influence on the device operation.

NOTE: A minimum value is specified that is the smallest time interval at which correct operation of the logic element is guaranteed.

t_S Set-Up Time: The time interval during which a stable signal must be maintained at a specified input terminal before an active transition at another specified input terminal.

NOTE: A minimum value is specified that is the smallest time interval at which correct operation of the logic element is guaranteed.

t_R Rise Time: The time interval between a specified low-level voltage and a specified high-level voltage on a waveform that is changing from a defined low level to a defined high level. Common defined levels are from 10% of the signal amplitude to 90% of the signal amplitude.

t_F Fall Time: The time interval between a specified high-level voltage and a specified low-level voltage on a waveform that is changing from a defined high level to a defined low level. Common defined levels are from 90% of the signal amplitude to 10% of the signal amplitude.

OUTPUT PARAMETERS

t_{PZH} Output Enable Time to a High Logic Level: The propagation delay time between the specified voltage reference points on the input and output waveforms with a TRI-STATE output changing from a high impedance (off) state to the defined high state.

t_{PZL} Output Enable Time to a Low Logic Level: The propagation delay time between the specified voltage reference points on the input and output waveforms with a TRI-STATE output changing from a high impedance (off) state to the defined low state.

t_{PHZ} Output Disable Time from a High Logic Level: The propagation delay time between the specified voltage reference points on the input and output waveforms with a TRI-STATE output changing from the defined high state to the high impedance (off) state .

t_{PLZ} Output Disable Time from a Low Logic Level: The propagation delay time between the specified voltage reference points on the input and output waveforms with a TRI-STATE output changing from the defined low state to the high impedance (off) state .

t_{WOUT} Output Pulse Width: The time interval between specified voltage reference points on the leading and trailing edges of an output waveform.

NOTE: This is usually only specified for monostable elements.

t_{PLH} Propagation Time, Low to High: The time between the specified voltage reference points on the input and output waveforms with the output changing from a low logic level to a high logic level.

t_{PHL} Propagation Delay, High to Low: The time between the specified voltage reference points on the input and output waveforms with the output changing from a high logic level to a low logic level.

t_{TLH}, t_r Transition Time, or Rise Time: The time interval between a specified low-level voltage and a specified high-level voltage on a waveform that is changing from a defined low level to a defined high level. Common defined levels are from 10% of the signal amplitude to 90% of the signal amplitude, or from 0.6V to 2.6V.

t_{THL}, t_f Transition Time, or Fall Time: The time interval between a specified high-level voltage and a specified low-level voltage on a waveform that is changing from a defined high level to a defined low level. Common defined levels are from 90% of the signal amplitude to 10% of the signal amplitude, or from 2.6V to 0.6V.

EXPLANATION OF DEVICE FUNCTIONS

Circuit Complexity

SSI: Small Scale Integration; the lowest level of complexity in integrated circuits.

MSI: Medium Scale Integration; small subsystems integrated into a single microcircuit.

LSI: Large Scale Integration; large subsystems or small systems integrated into a single microcircuit.

FUNCTIONAL DESCRIPTIONS

Buffer: A logic gate with high output drive capability, or fan-out. Buffers are used where a single circuit must drive a large number of loads.

Comparator: A logic circuit that will compare two separate input signals and produce an output based on that comparison. A simple comparator is the Exclusive-NOR gate, which produces a high level output only when its two inputs are identical.

Counter: A logic circuit that counts the number of input pulses it receives. Counters can be used for frequency division, counting, and sequencing digital operations. Common counter configurations are Binary, where the device counts from 0 to 15 and Decade, where the device counts from 0 to 9.

AC Operating Conditions and Characteristics (Continued)

Data Selector/Multiplexer: A logic circuit that will select one of several input signals and feed that signal onto a common bus line. It can be thought of as a multipole, multiposition switch with each switch pole representing one output and each switch position representing one input.

Decoder/Demultiplexer: A logic circuit that is the complement of the Data Selector/Multiplexer; that is, this circuit takes an input signal and feeds it to any one of several output lines depending on the information placed on its steering, or control, inputs.

Driver: Same as Buffer, above.

Flip-Flop: A logic circuit that is used to store information. A flip-flop is called "bistable" since it has two stable states.

Gate: The basic building block of all logic circuits; an element whose output is a Boolean function of its inputs. The basic functions are the AND, OR, and NOT. By combining these functions, NAND, NOR, and Exclusive-OR and Exclusive-NOR gates are built.

Latch: A bistable element that latches, or holds, data which is present at its input at the time the Enable input goes to its inactive state. When the Enable input is active, the data, present at the input, is passed directly to the output, similar to the operation of a gate.

One-Shot: Monostable multivibrator; a flip-flop that only has one stable state. When triggered by an input transient, it flips to its unstable state for a time period determined by an external R-C network connected to its timing inputs, and then returns to its stable state.

Shift Register: A series of flip-flops in which the data signal is shifted out of one flip-flop and into the succeeding flip-flop during an active transition on the clock input.

Transceiver: A logic circuit that can transmit data onto a bus line and receive data off of the bus line using the same terminal as an input and output. The direction of signal flow is determined by logic levels present at a Direction Control input.

OTHER TERMS

Asynchronous: A mode of operation that does not require any specific timing relationship between different control inputs.

Open Collector: Output configuration that has no internal pullup. This configuration enables outputs that are connected together (wired-OR) to assume opposite states without incurring damage.

Schmitt Trigger: An input configuration that has a different threshold point depending on whether the input signal is rising or falling. This is especially useful in electrically noisy environments.

Synchronous: A mode of operation where specific timing requirements must be met between control inputs before an indicated action can occur.

Totem Pole: An output configuration that contains an internal pullup structure, usually a transistor pullup allowing higher output drive capability than is available with open collector outputs.

TRI-STATE: A registered trademark for a circuit configuration in which the device can be switched 'off' during which time the output presents a very high impedance to the bus it is connected to. This allows multiple outputs to be connected to a bus line while only one output drives the line, the other outputs being switched into their high impedance states.

EXPLANATION OF FUNCTION TABLES

The following symbols are used in the function tables found in NSC data sheets:

H = high logic level (steady state)
L = low logic level (steady state)
↑ = transition from low to high logic level
↓ = transition from high to low logic level
X = irrelevant (any level, including transitions)
Z = off (high impedance) state of a TRI-STATE output
a . . . h = the level of steady state inputs at inputs A through H respectively
Q_0 = the level of Q before the indicated steady state input conditions were established
$\overline{Q}_0$ = complement of Q_0 or level of Q before the indicated steady state input conditons were established
Q_n = level of Q before the most recent active transition indicated by ↑ or ↓
⎍ = one high level pulse
⎍ = one low level pulse
toggle = each output changes to the complement of its previous level on each active transition indicated by ↑ or ↓

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady state levels. If the output is shown as a level (H, L, Q_0, or $\overline{Q}_0$), it persists so long as the steady state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect on the output. If the output is shown as a pulse, ⎍ or ⎍, the pulse follows the indicated input transition and persists for an interval dependent on the circuit.

Among the most complex function tables in this book are those of the shift registers. These embody most of the symbols used in any of the function tables, plus more. As an example, *Figure 1* is the function table for a 4-bit bidirectional universal shift register, similar to the DM54LS194.

The first line of the table represents "asynchronous" clearing of the register and indicates that if CLEAR is low, all four outputs will be reset low regardless of the states of the other inputs. In the succeeding lines, CLEAR is inactive (high) and consequently has no effect.

AC Operating Conditions and Characteristics (Continued)

The second line indicates that so long as the CLOCK input remains low (while CLEAR is high), no other input has any effect and the outputs maintain the levels they assumed before the steady-state combination of CLEAR high and CLOCK low was established. Since on all the other lines of the table only the rising edge of the CLOCK is shown to be active, the second line implicitly shows that no further change in the outputs will occur while the CLOCK remains high or on the high-to-low transition of the CLOCK.

The third line of the table represents "synchronous" parallel loading of the register and indicates that if S1 and S0 are both high, then regardless of the levels at the SERIAL inputs, the data present at A will transfer to QA, the data present at B will transfer to QB, and so forth, following a low-to-high transition on CLOCK.

The fourth and fifth lines represent the "synchronous" loading of high and low level data, respectively, from the SHIFT RIGHT SERIAL input and the shifting one bit to the right of previously entered data; data previously at QA is now at QB, data previously at QB and QC is now at QC and QD respectively, and the data previously at QD has been shifted out of the register. This entry of data and shifting takes place on the low-to-high level transition of CLOCK when S1 is low and S0 is high and as shown, the levels at the PARALLEL inputs, A through D, have no effect.

The sixth and seventh lines represent the "synchronous" loading of high and low level data respectively, from the SHIFT LEFT SERIAL input and the shifting one bit to the left of previously entered data; data previously at QD is now at QC, data previously at QC and QB is now at QB and QA respectively, and the data previously at QA has been shifted out of the register. This entry of serial data and shifting to the left takes place on the low-to-high level transition of CLOCK when S1 is high and S0 is low and as seen, the levels at the PARALLEL inputs, A through D, have no effect.

The last line indicates that so long as both MODE inputs are low, no other input has any effect and, as in the second line, the outputs maintain the levels they assumed before the steady state combination of CLEAR high and both MODE inputs low was established.

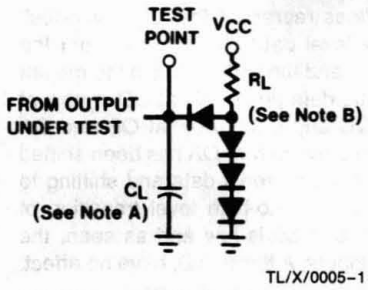
Clear	Mode		Inputs							Outputs			
			Clock	Serial		Parallel							
	S1	S0		Left	Right	A	B	C	D	Q_A	Q_B	Q_C	Q_D
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

FIGURE 1. Function Table

DM54/74, 54S/74S Test Waveforms

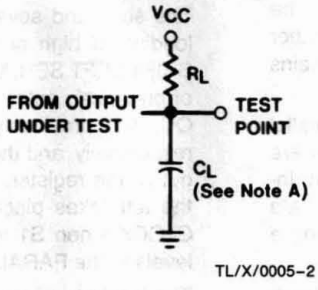
Parameter Measurement Information

Load Circuit for Bi-State Totem-Pole Outputs



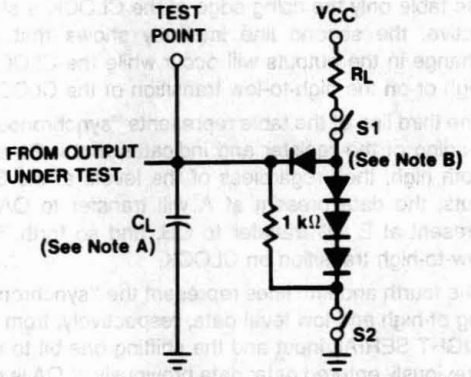
TL/X/0005–1

Load Circuit for Open-Collector Outputs



TL/X/0005–2

Load Circuit for TRI-STATE® Outputs

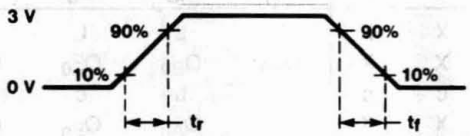


TL/X/0005–3

Note A: C_L includes probe and jig capacitance.

Note B: All diodes are 1N916 or 1N3064.

Input Waveform



TL/X/0005–4

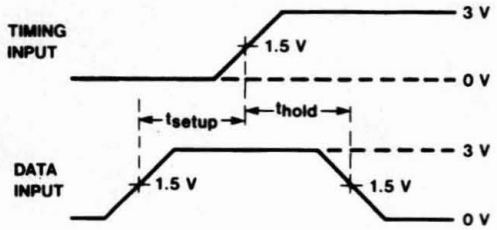
54/74 $t_r \leq 7$ ns; $t_f \leq 7$ ns

54S/74S $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns

Generator: $Z_{OUT} \approx 50\Omega$

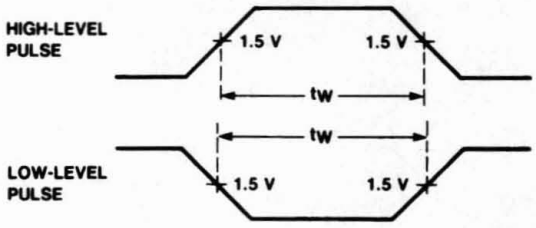
PRR ≤ 1 MHz

Voltage Waveforms Setup and Hold Times



TL/X/0005–5

Voltage Waveforms Pulse Widths

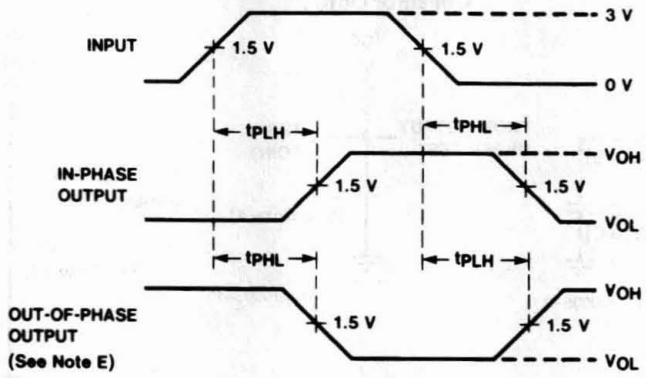


TL/X/0005–6

DM54/74, 54S/74S Test Waveforms (Continued)

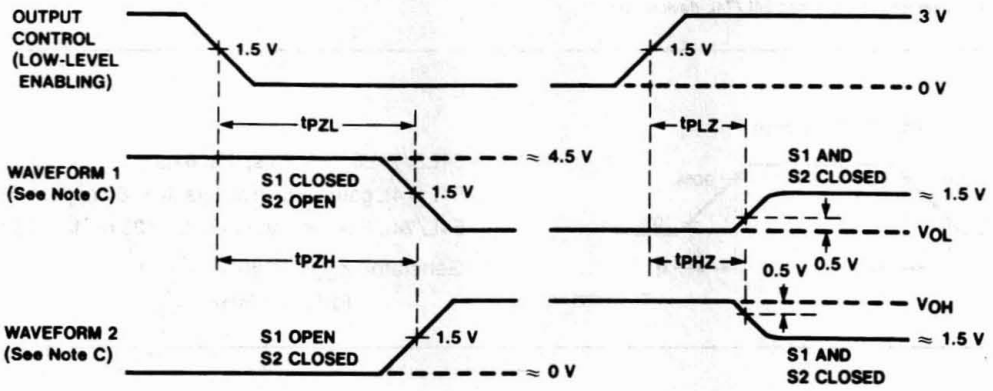
Parameter Measurement Information (Continued)

Voltage Waveforms Propagation Delay Times



TL/X/0005–7

Voltage Waveforms Enable and Disable Times, TRI-STATE Outputs



TL/X/0005–8

Note C: Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

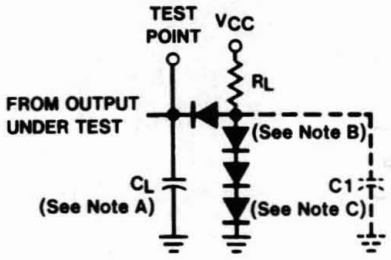
Note D: In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

Note E: When measuring propagation delay times of TRI-STATE outputs, switches S1 and S2 are closed.

DM54L/74L, 54LS/74LS Test Waveforms

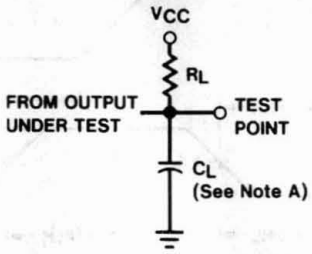
Parameter Measurement Information

Load Circuit for Bi-State Totem-Pole Outputs



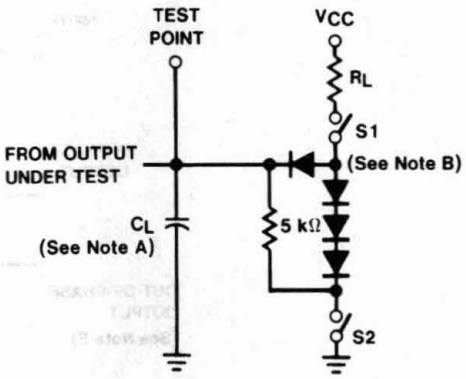
TL/X/0005-9

Load Circuit for Open-Collector Outputs



TL/X/0005-10

TRI-STATE Outputs



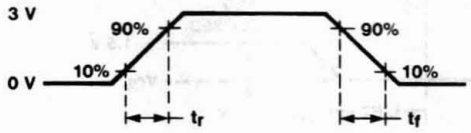
TL/X/0005-11

Note A: C_L includes probe and jig capacitance.

Note B: All diodes are 1N916 or 1N3064.

Note C: C1 (30 pF) is used for testing Series 54L/74L devices only.

Input Waveform



TL/X/0005-12

54LS/74LS: $t_r \leq 6$ ns, $t_f \leq 6$ ns

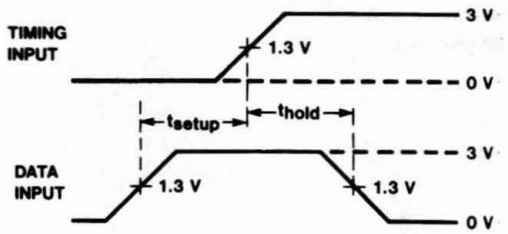
54L/74L gates and inverters: $t_r \leq 60$ ns, $t_f \leq 60$ ns

54L/74L flip-flops and MSI: $t_r \leq 25$ ns, $t_f \leq 25$ ns

Generator: $Z_{OUT} \approx 50\Omega$

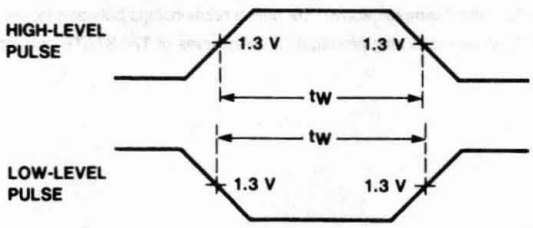
PRR $\leq$ 1 MHz

Voltage Waveforms Setup and Hold Times



TL/X/0005-13

Voltage Waveforms Pulse Widths

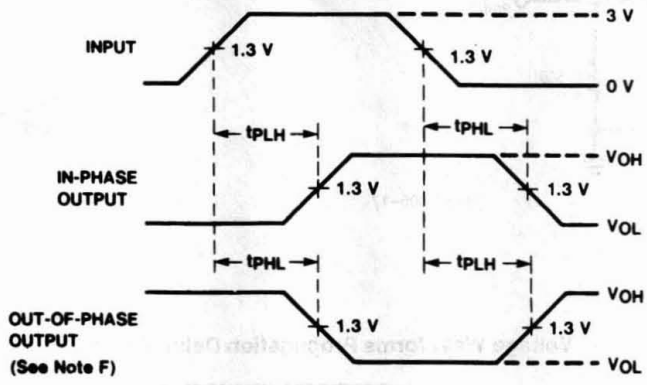


TL/X/0005-14

DM54L/74L, 54LS/74LS Test Waveforms (Continued)

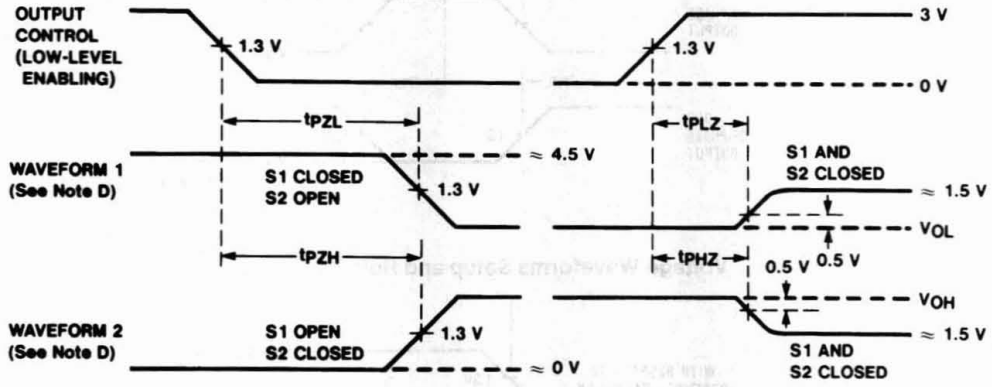
Parameter Measurement Information (Continued)

Voltage Waveforms Propagation Delay Times



TL/X/0005–15

Voltage Waveforms Enable and Disable Times, TRI-STATE Outputs



TL/X/0005–16

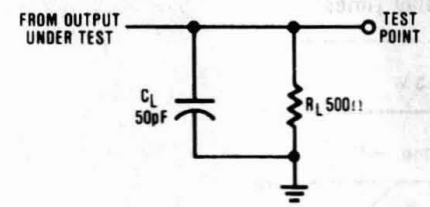
Note D: Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Note E: In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

Note F: When measuring propagation delay times of TRI-STATE outputs, switches S1 and S2 are closed.

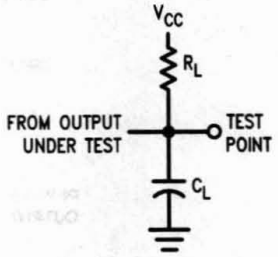
Test Waveforms DM54ALS/74ALS, 54AS/74AS

Load Circuit for Bi-State Totem-Pole Outputs



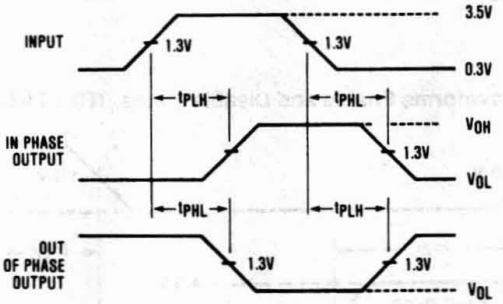
TL/X/0005–17

Load Circuit for Open-Collector Outputs



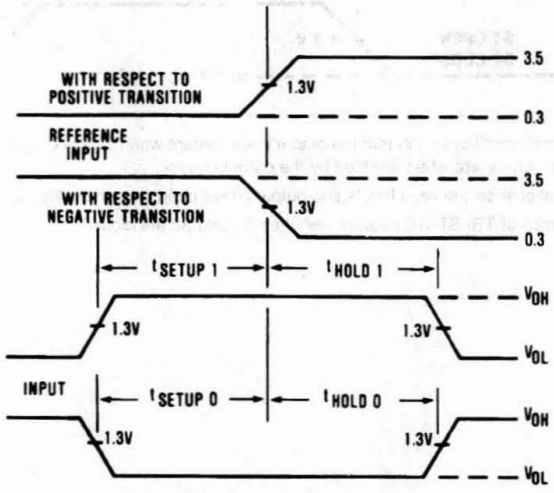
TL/X/0005–33

Voltage Waveforms Propagation Delay Times



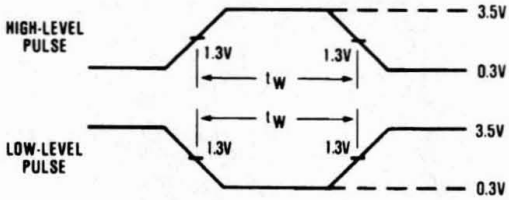
TL/X/0005–18

Voltage Waveforms Setup and Hold Times



TL/X/0005–19

Voltage Waveforms Pulse Widths

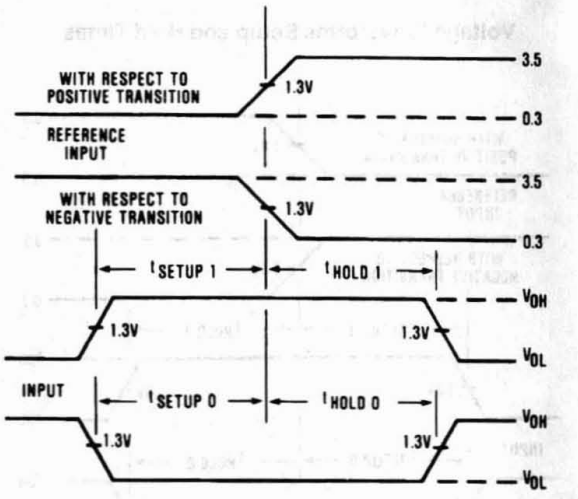


TL/X/0005–22

Note: All input pulses are supplied by generators having the following characteristics: frequency = 1 MHz, Z_{OUT} = 50Ω, t_r = t_f = 2 ns.

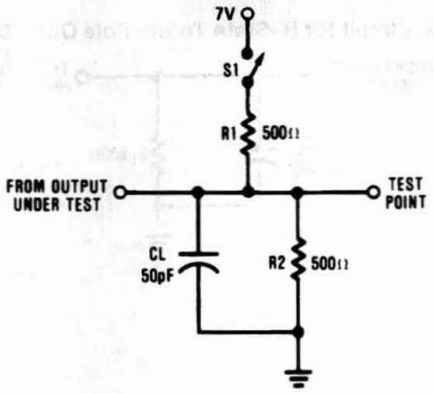
Test Waveforms DM54ALS/74ALS, 54AS/74AS (Continued)

Voltage Waveforms Setup and Hold Times



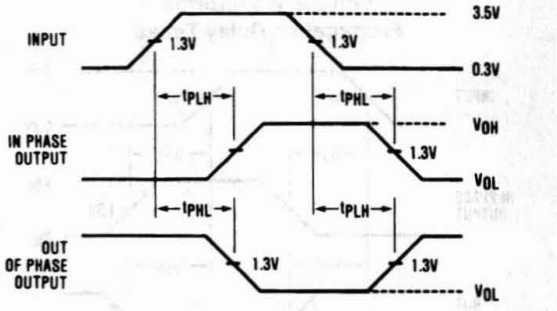
TL/X/0005–19

Load Circuit for TRI-STATE Outputs



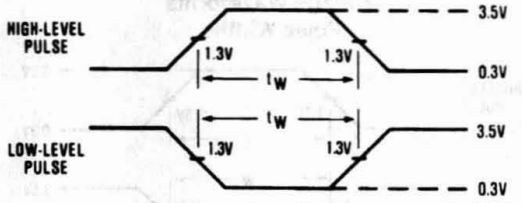
TL/X/0005–20

Voltage Waveforms Propagation Delay Times



TL/X/0005–21

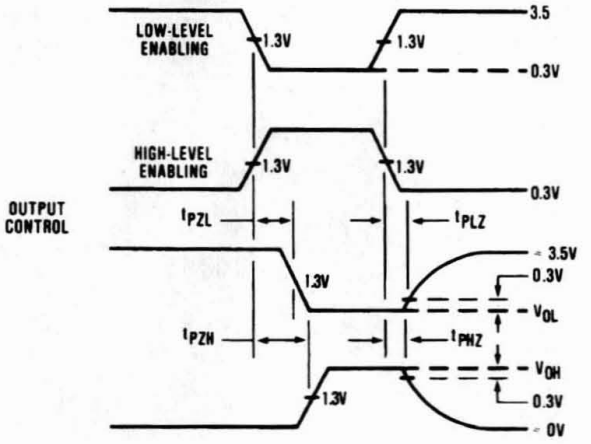
Voltage Waveforms Pulse Widths



TL/X/0005–22

Parameter	S1 Switch Position
T_{PLH}	OPEN
T_{PHL}	OPEN
T_{PHZ}	OPEN
T_{PZH}	OPEN
T_{PLZ}	CLOSED
T_{PZL}	CLOSED

Voltage Waveforms Enable and Disable Times, TRI-STATE Outputs



TL/X/0005–23

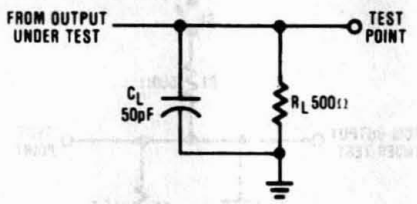
NOTE: All input pulses are supplied by generators having the following characteristics: frequency = 1 MHz, $Z_{OUT} = 50\Omega$, $t_r = t_f = 2$ ns.

Group 4 Test Waveforms DM54ALS/74ALS, 54AS/74AS

54ALS74, 109, 112, 113, 114, 131, 137, 160, 161, 162, 163, 168, 169, 174, 175, 273

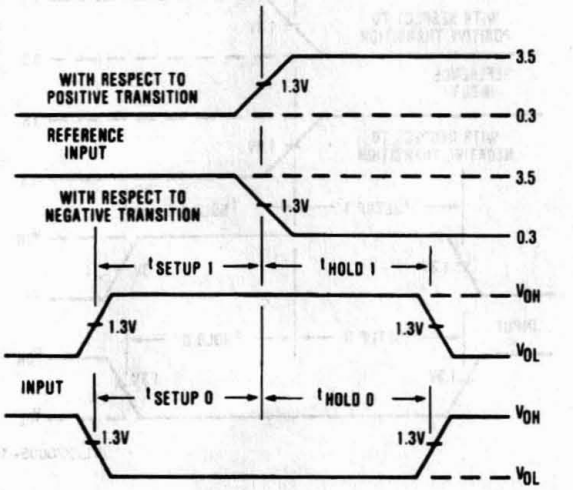
54AS74, 109, 112, 113, 114, 160, 161, 162, 163, 168, 169, 174, 175, 273

Load Circuit for Bi-State Totem-Pole Outputs



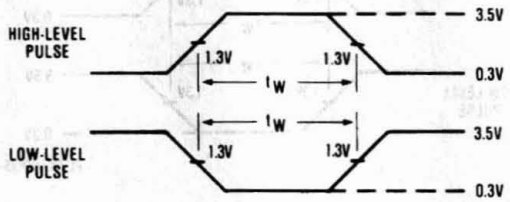
TL/X/0005–27

Voltage Waveforms Setup and Hold Times



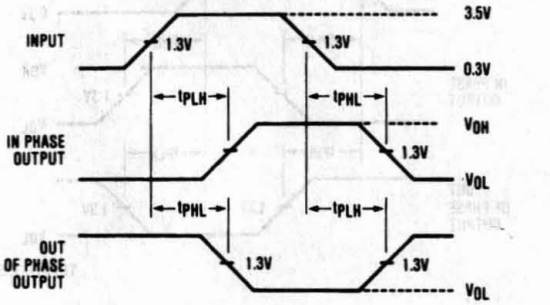
TL/X/0005–28

Voltage Waveforms Pulse Widths



TL/X/0005–29

Voltage Waveforms Propagation Delay Times



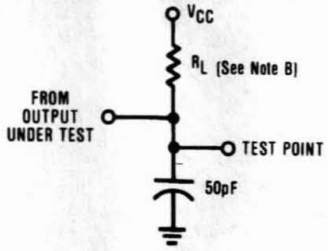
TL/X/0005–30

NOTE: All input pulses are supplied by generators having the following characteristics: frequency = 1 MHz, $Z_{OUT} = 50\Omega$, $t_r = t_f = 2$ ns.

Group 5 Test Waveforms DM54ALS/74ALS, 54AS/74AS

54ALS01, 03, 05, 09, 12, 15, 22, 33, 38, 518, 519, 522, 689, 1003, 1005, 1035

Load Circuit for Open-Collector Outputs



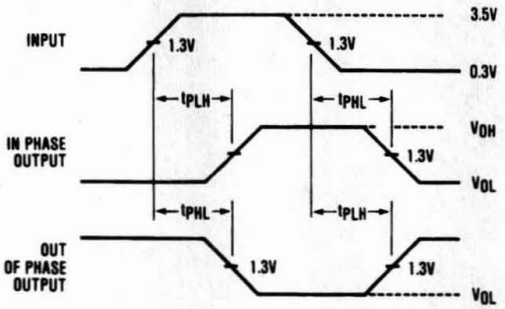
TL/X/0005–31

NOTES: A. C_L includes probe and jig capacitance

B. R_L = 2 kΩ for standard outputs

R_L = 667Ω for buffered outputs

Voltage Waveforms Propagation Delay Times



TL/X/0005–32

Note: All input pulses are supplied by generators having the following characteristics: frequency = 1 MHz, Z_{OUT} = 50Ω, $t_r = t_f$ = 2 ns.

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Advanced Low Power Schottky

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National Semiconductor Corporation

DM54ALS00A/DM74ALS00A Quad 2-Input NAND Gates

General Description

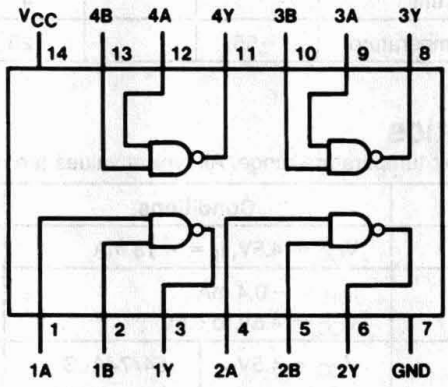
This device contains four independent gates, each of which performs the logic NAND function.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky and low power Schottky TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts

Connection Diagram

Dual-In-Line Package



TL/F/6270–1

Order Number DM54ALS00AJ, DM74ALS00AM or DM74ALS00AN
See NS Package Number J14A, M14A or N14A

Function Table

$$Y = \overline{AB}$$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS00A			DM74ALS00A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		0.43	0.85	mA
			Outputs Low		1.62	3	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	DM54ALS00A		DM74ALS00A		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	3	16	3	11	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		2	13	2	8	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM54ALS01/DM74ALS01 Quad 2-Input NAND Gates with Open-Collector Outputs

General Description

This device contains four independent gates, each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

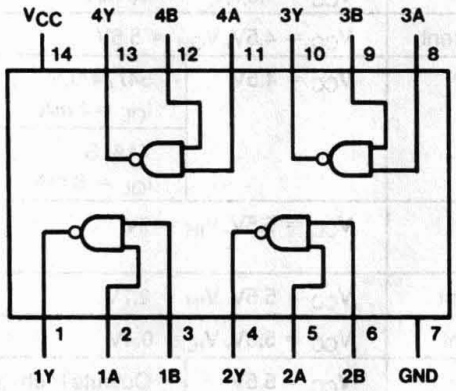
$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky and low power Schottky TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts

Connection Diagram

Dual-In-Line Package



TL/F/6174–1

Order Number DM54ALS01J, DM74ALS01M or DM74ALS01N
See NS Package Number J14A, M14A or N14A

Function Table

$$Y = \overline{AB}$$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level

L = Low Logic Level

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
High Level Output Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS01			DM74ALS01			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
I_{OH}	High Level Output Current	V_{CC} = 4.5V, V_{OH} = 5.5V				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Input Current @ Max. Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		0.43	0.85	mA
			Outputs Low		1.62	3	mA

Switching Characteristics

over recommended operating free air temperature range (Note 1).

Symbol	Parameter	Conditions	DM54ALS01		DM74ALS01		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V, R_L = 2 kΩ, C_L = 50 pF	23	66	23	54	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		8	39	4	28	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM54ALS02/DM74ALS02 Quad 2-Input NOR Gates

General Description

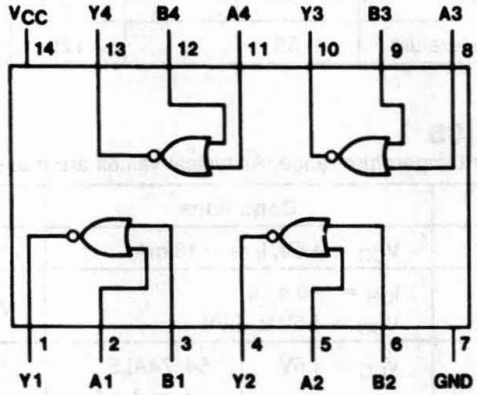
This device contains four independent gates, each of which performs the logic NOR function.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky and low power Schottky TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts

Connection Diagram

Dual-In-Line Package



TL/F/6175–1

Order Number DM54ALS02J, DM74ALS02M or DM74ALS02N
See NS Package Number J14A, M14A or N14A

Function Table

$$Y = \overline{A + B}$$

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS02			DM74ALS02			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Input Current @ Max. Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		0.85	2.2	mA
			Outputs Low		2.16	4	mA

Switching Characteristics

over recommended operating free air temperature range (Note 1).

Symbol	Parameter	Conditions	DM54ALS02		DM74ALS02		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	1	18	3	12	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		1	11	3	10	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM54ALS03B/DM74ALS03B Quad 2-Input NAND Gates with Open Collector Outputs

General Description

This device contains four independent gates, each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

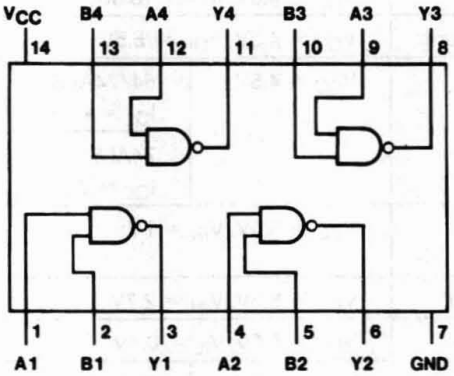
$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky and low power Schottky TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts

Connection Diagram

Dual-In-Line Package



TL/F/6176–1

Order Number DM54ALS03BJ, DM74ALS03BM or DM74ALS03BN
See NS Package Number J14A, M14A or N14A

Function Table

$$Y = \overline{AB}$$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level

L = Low Logic Level

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
High Level Output Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS03B			DM74ALS03B			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
I_{OH}	High Level Output Current	V_{CC} = 4.5V, V_{OH} = 5.5V				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Input Current @ Max. Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		0.43	0.85	mA
			Outputs Low		1.62	3	mA

Switching Characteristics

over recommended operating free air temperature range (Note 1).

Symbol	Parameter	Conditions	DM54ALS03B		DM74ALS03B		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 2 kΩ C_L = 50 pF	20	59	20	50	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		3	23	3	13	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM54ALS04B/DM74ALS04B Hex Inverters

General Description

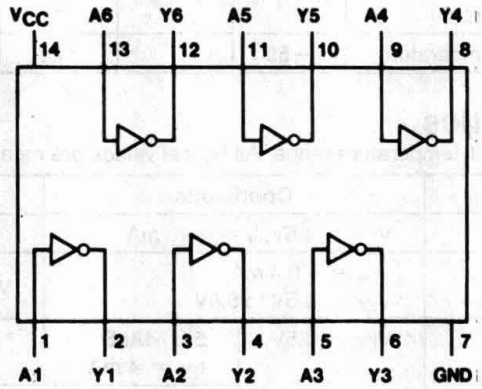
This device contains six independent gates, each of which performs the logic INVERT function.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky and low power Schottky TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts

Connection Diagram

Dual-In-Line Package



TL/F/6177–1

Order Number DM54ALS04BJ, DM74ALS04BM or DM74ALS04BN
See NS Package Number J14A, M14A or N14A

Function Table

$Y = \overline{A}$

Input	Output
A	Y
L	H
H	L

H = High Logic Level

L = Low Logic Level

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS04B			DM74ALS04B			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Input Current @ Max. Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		0.65	1.1	mA
			Outputs Low		2.4	4.2	mA

Switching Characteristics

over recommended operating free air temperature range (Note 1).

Symbol	Parameter	Conditions	DM54ALS04B		DM74ALS04B		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	3	14	3	11	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		2	12	2	8	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM54ALS05A/DM74ALS05A Hex Inverters with Open Collector Outputs

General Description

This device contains six independent gates, each of which performs the logic INVERT function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

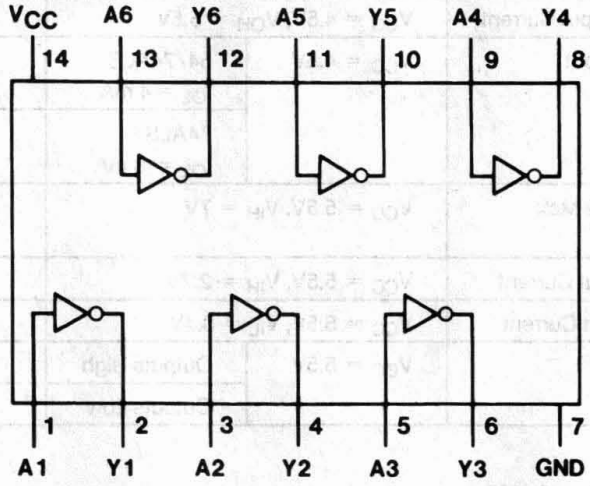
$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky and low power Schottky TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts

Connection Diagram

Dual-In-Line Package



TL/F/6178–1

Order Number DM54ALS05AJ, DM74ALS05AM or DM74ALS05AN
See NS Package Number J14A, M14A or N14A

Function Table

$$Y = \overline{A}$$

Input	Output
A	Y
L	H
H	L

H = High Logic Level

L = Low Logic Level

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
High Level Output Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS05A			DM74ALS05A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
I_{OH}	High Level Output Current	V_{CC} = 4.5V, V_{OH} = 5.5V				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		0.65	1.1	mA
			Outputs Low		2.4	4.2	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	DM54ALS05A		DM74ALS05A		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 2 kΩ C_L = 50 pF	23	84	23	54	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		4	24	4	14	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM54ALS08/DM74ALS08 Quad 2-Input AND Gates

General Description

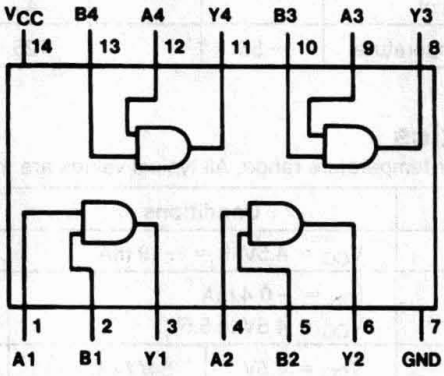
This device contains four independent gates, each of which performs the logic AND function.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky and low power Schottky TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts

Connection Diagram

Dual-In-Line Package



TL/F/6271–1

Order Number DM54ALS08J, DM74ALS08M or DM74ALS08N
See NS Package Number J14A, M14A or N14A

Function Table

$Y = AB$

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = High Logic Level

L = Low Logic Level

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS08			DM74ALS08			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Input Current @ Max. Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		1.3	2.4	mA
			Outputs Low		2.2	4	mA

Switching Characteristics

over recommended operating free air temperature range (Note 1).

Symbol	Parameter	Conditions	DM54ALS08		DM74ALS08		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	4	18	4	14	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		3	15	3	10	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM54ALS11A/DM74ALS11A Triple 3-Input AND Gates

General Description

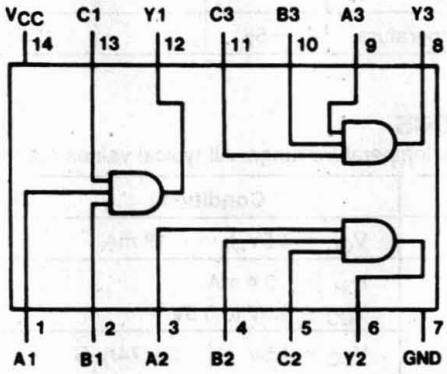
This device contains three independent gates, each of which performs the logic AND function.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky and low power Schottky TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts

Connection Diagram

Dual-In-Line Package



TL/F/6181–1

Order Number DM54ALS11AJ, DM74ALS11AM or DM74ALS11AN
See NS Package Number J14A, M14A or N14A

Function Table

$Y = ABC$

Inputs			Output
A	B	C	Y
X	X	L	L
X	L	X	L
L	X	X	L
H	H	H	H

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS11A			DM74ALS11A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		1	1.8	mA
			Outputs Low		1.6	3	mA

Switching Characteristics

over recommended operating free air temperature range (Note 1).

Symbol	Parameter	Conditions	DM54ALS11A		DM74ALS11A		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	2	17	2	13	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		2	14	2	10	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM54ALS12A/DM74ALS12A Triple 3-Input NAND Gates with Open Collector Outputs

General Description

This device contains three independent gates, each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

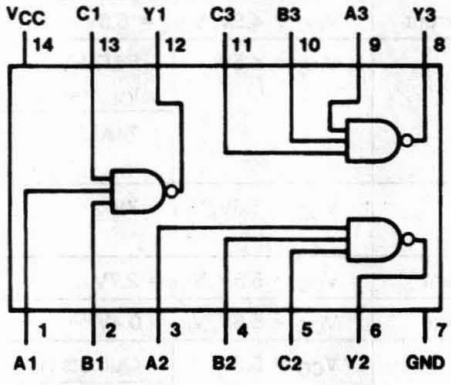
$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky and low power Schottky TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts

Connection Diagram

Dual-In-Line Package



TL/F/6182–1

Order Number DM54ALS12AJ, DM74ALS12AM or DM74ALS12AN
See NS Package Number J14A, M14A or N14A

Function Table

$$Y = \overline{ABC}$$

Inputs			Output
A	B	C	Y
X	X	L	H
X	L	X	H
L	X	X	H
H	H	H	L

H = High Logic Level

L = Low Logic Level

X = Either Low or High Logic Level

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
High Level Output Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS12A			DM74ALS12A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
I_{OH}	High Level Output Current	V_{CC} = 4.5V, V_{OH} = 5.5V				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		0.32	0.6	mA
			Outputs Low		1.2	2.2	mA

Switching Characteristics

over recommended operating free air temperature range (Note 1).

Symbol	Parameter	Conditions	DM54ALS12A		DM74ALS12A		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 2 kΩ C_L = 50 pF	23	59	23	54	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		5	26	5	18	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM54ALS13/DM74ALS13 Dual 4-Input NAND Gates with Schmitt Trigger Inputs

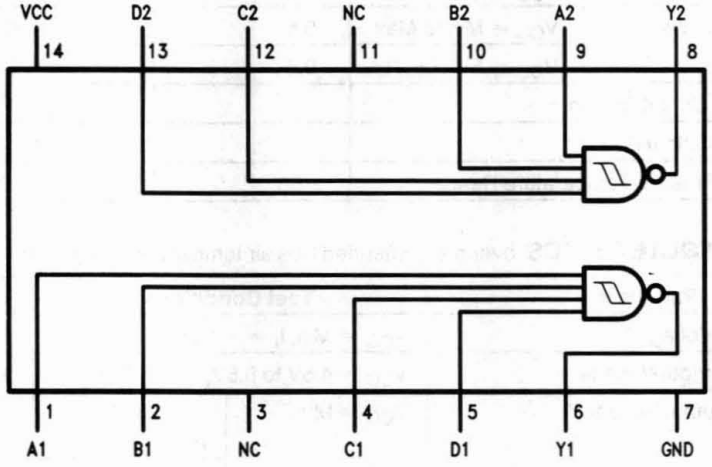
General Description

This device contains two independent gates, each of which performs the logic NAND function. Each input has hysteresis which increases the noise immunity and transforms a slowly changing input signal to a fast changing, jitter-free output.

Features

- Switching specification at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin-for-pin compatible with Schottky and Low Power Schottky TTL counterparts
- Improved AC performance over low power Schottky counterpart

Connection Diagram



TL/F/8772–1

Order Number DM54ALS13J, DM74ALS13M or DM74ALS13N
See NS Package Number J14A, M14A or N14A

Function Table

$$Y = \overline{ABCD}$$

Inputs				Output
A	B	C	D	Y
X	X	X	L	H
X	X	L	X	H
X	L	X	X	H
L	X	X	X	H
H	H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to +150°C
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54ALS13			DM74ALS13			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.5	5	5.5	V
V_{T+}	Positive-Going Input Threshold Voltage	V_{CC} = Min to Max	1.4		2	1.4		2	V
		V_{CC} = 5V	1.55		1.85	1.55		1.85	
V_{T-}	Negative-Going Input Threshold Voltage	V_{CC} = Min to Max	0.75		1.2	0.75		1.2	V
		V_{CC} = 5V	0.85		1.1	0.85		1.1	
HYS	Input Hysteresis	V_{CC} = Min to Max	0.5			0.5			V
		V_{CC} = 5V	0.6			0.6			
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
T_A	Operating Free Air Temperature Range		−55		125	0		70	°C

Electrical Characteristics over recommended free air temperature range (unless otherwise noted)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V, I_{OH} = Max		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	
I_{T+}	Input Current at Positive-Going Threshold Voltage	V_{CC} = 5V, V_I = V_{T+}				20	μA
I_{T-}	Input Current at Negative-Going Threshold Voltage	V_{CC} = 5V, V_I = V_{T-}				−100	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 7V				100	μA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−100	μA
I_O	Output Drive Current	V_{CC} = Max, V_O = 2.25V		−30		−112	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max				4	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max				4	mA

Switching Characteristics over recommended operating free air temperature range

Symbol	Parameter	Conditions (Note 1)	DM54ALS13		DM74ALS13		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V RL = 500Ω, CL = 50 pF	2	13	2	12	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		2	13	2	12	

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM54ALS14/DM74ALS14 Hex Inverters with Schmitt Trigger Inputs

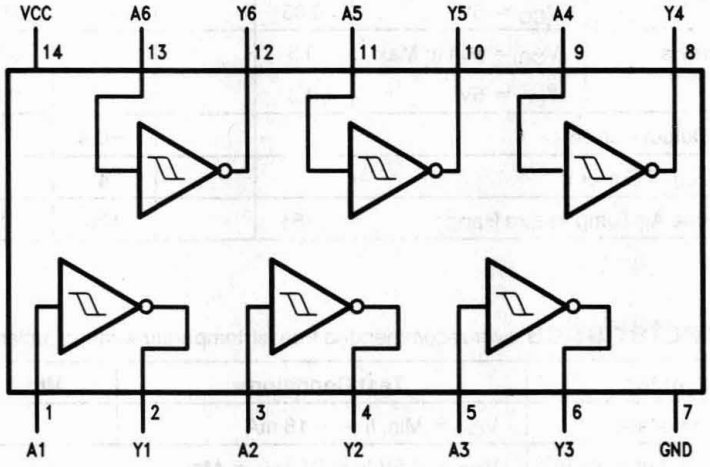
General Description

This device contains six independent gates, each of which performs the logic INVERT function. Each input has hysteresis which increases the noise immunity and transforms a slowly changing input signal to a fast changing, jitter-free output.

Features

- Switching specification at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin-for-pin compatible with Schottky and Low Power Schottky TTL counterparts
- Improved AC performance over low power Schottky counterpart

Connection Diagram



TL/F/8773–1

Order Number DM54ALS14J, DM74ALS14M or DM74ALS14N
See NS Package Number J14A, M14A or N14A

Function Table

$Y = \overline{A}$

Input A	Output Y
L	H
H	L

H = High Logic Level

L = Low Logic Level

2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to +150°C
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C

NOTE: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54ALS14			DM74ALS14			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.5	5	5.5	V
V_{T+}	Positive-Going Input Threshold Voltage	V_{CC} = Min to Max	1.4		2	1.4		2	V
		V_{CC} = 5V	1.55		1.85	1.55		1.85	
V_{T-}	Negative-Going Input Threshold Voltage	V_{CC} = Min to Max	0.75		1.2	0.75		1.2	V
		V_{CC} = 5V	0.85		1.1	0.85		1.1	
HYS	Input Hysteresis	V_{CC} = Min to Max	0.5			0.5			V
		V_{CC} = 5V	0.6			0.6			
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
T_A	Operating Free Air Temperature Range		−55		125	0		70	°C

Electrical Characteristics over recommended free air temperature range (unless otherwise noted)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V, I_{OH} = Max		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_{T+}	Input Current at Positive-Going Threshold Voltage	V_{CC} = 5V, V_I = V_{T+}				20	μA
I_{T-}	Input Current at Negative-Going Threshold Voltage	V_{CC} = 5V, V_I = V_{T-}				−100	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 7V				100	μA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−100	μA
I_O	Output Drive Current	V_{CC} = Max, V_O = 2.25V		−30		−112	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max				12	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max				12	mA

Switching Characteristics over recommended operating free air temperature range

Symbol	Parameter	Conditions (Note 1)	DM54ALS14		DM74ALS14		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω, C_L = 50 pF	2	13	2	12	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		2	11	2	10	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM54ALS15A/DM74ALS15A Triple 3-Input AND Gates with Open Collector Outputs

General Description

This device contains three independent gates, each of which performs the logic AND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

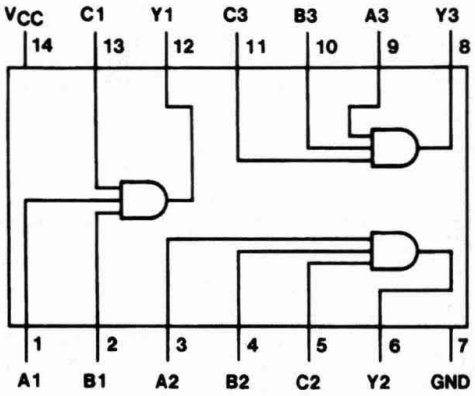
$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Features

- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky and low power Schottky TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts

Connection Diagram

Dual-In-Line Package



TL/F/6183–1

Order Number DM54ALS15AJ, DM74ALS15AM or DM74ALS15AN
See NS Package Number J14A, M14A or N14A

Function Table

Y = ABC

Inputs			Output
A	B	C	Y
X	X	L	L
X	L	X	L
L	X	X	L
H	H	H	H

H = High Logic Level

L = Low Logic Level

X = Either Low or High Logic Level

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
High Level Output Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS15A			DM74ALS15A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
I_{OH}	High Level Output Current	V_{CC} = 4.5V, V_{OH} = 5.5V				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		1.0	1.8	mA
			Outputs Low		1.66	3	mA

Switching Characteristics

over recommended operating free air temperature range (Note 1).

Symbol	Parameter	Conditions	DM54ALS15A		DM74ALS15A		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V, R_L = 2 kΩ, C_L = 50 pF	20	59	20	45	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		6	25	6	20	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM54ALS20A/DM74ALS20A Dual 4-Input NAND Gates

General Description

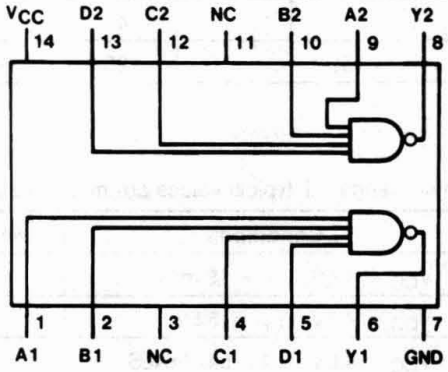
This device contains two independent gates, each of which performs the logic NAND function.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky and low power Schottky TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts

Connection Diagram

Dual-In-Line Package



TL/F/6184–1

Order Number DM54ALS20AJ, DM74ALS20AM or DM74ALS20AN
See NS Package Number J14A, M14A or N14A

Function Table

$$Y = \overline{ABCD}$$

Inputs				Output
A	B	C	D	Y
X	X	X	L	H
X	X	L	X	H
X	L	X	X	H
L	X	X	X	H
H	H	H	H	L

H = High Logic Level

L = Low Logic Level

X = Either Low or High Logic Level

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS20A			DM74ALS20A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		0.22	0.4	mA
			Outputs Low		0.81	1.5	mA

Switching Characteristics

over recommended operating free air temperature range (Note 1).

Symbol	Parameter	Conditions	DM54ALS20A		DM74ALS20A		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	1	18	3	11	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		1	15	3	10	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM54ALS21A/DM74ALS21A Dual 4-Input AND Gates

General Description

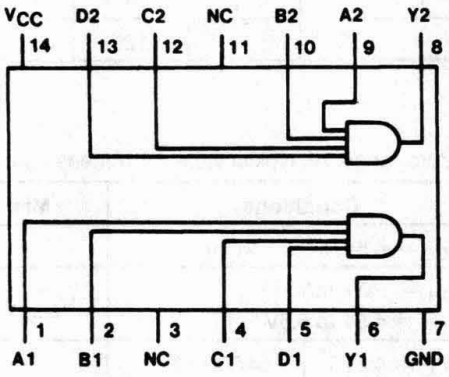
This device contains two independent gates, each of which performs the logic AND function.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky and low power Schottky TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts

Connection Diagram

Dual-In-Line Package



TL/F/6185–1

Order Number DM54ALS21AJ, DM74ALS21AM or DM74ALS21AN
See NS Package Number J14A, M14A or N14A

Function Table

$Y = ABCD$

Inputs				Output
A	B	C	D	Y
X	X	X	L	L
X	X	L	X	L
X	L	X	X	L
L	X	X	X	L
H	H	H	H	H

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS21A			DM74ALS21A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		0.85	1.4	mA
			Outputs Low		1.4	2.3	mA

Switching Characteristics

over recommended operating free air temperature range (Note 1).

Symbol	Parameter	Conditions	DM54ALS21A		DM74ALS21A		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	4	18	4	15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		2	12	2	10	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM54ALS22B/DM74ALS22B Dual 4-Input NAND Gates with Open Collector Outputs

General Description

This device contains two independent gates, each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

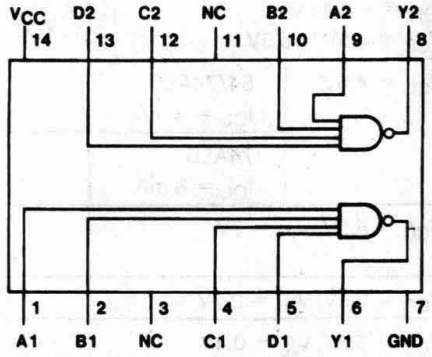
$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Features

- Switching specifications at 50 pF.
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky and low power Schottky TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts

Connection Diagram

Dual-In-Line Package



TL/F/6186–1

Order Number DM54ALS22BJ, DM74ALS22BM or DM74ALS22BN
See NS Package Number J14A, M14A or N14A

Function Table

$$Y = \overline{ABCD}$$

Inputs				Output
A	B	C	D	Y
X	X	X	L	H
X	X	L	X	H
X	L	X	X	H
L	X	X	X	H
H	H	H	H	L

H = High Logic Level

L = Low Logic Level

X = Either Low or High Logic Level

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
High Level Output Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS22B			DM74ALS22B			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
I_{OH}	High Level Output Current	V_{CC} = 4.5V, V_{OH} = 5.5V				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		0.22	0.4	mA
			Outputs Low		0.80	1.5	mA

Switching Characteristics

over recommended operating free air temperature range (Note 1).

Symbol	Parameter	Conditions	DM54ALS22B		DM74ALS22B		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V, R_L = 2 kΩ, C_L = 50 pF	23	65	23	45	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		4	32	4	18	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM54ALS27/DM74ALS27 Triple 3-Input NOR Gates

General Description

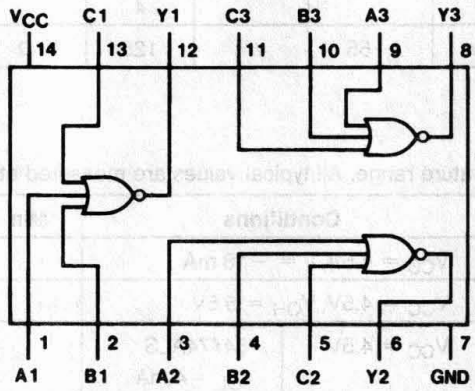
This device contains three independent gates, each of which performs the logic NOR function.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky and low power Schottky TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts

Connection Diagram

Dual-In-Line Package



TL/F/6187–1

Order Number DM54ALS27J, DM74ALS27M or DM74ALS27N
See NS Package Number J14A, M14A or N14A

Function Table

$$Y = \overline{A + B + C}$$

Inputs			Output
A	B	C	Y
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS27			DM74ALS27			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		0.97	1.8	mA
			Outputs Low		2	4	mA

Switching Characteristics

over recommended operating free air temperature range (Note 1).

Symbol	Parameter	Conditions	DM54ALS27		DM74ALS27		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	4	26	4	15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		1	11	3	9	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM54ALS28A/DM74ALS28A Quadruple 2-Input NOR Buffers

General Description

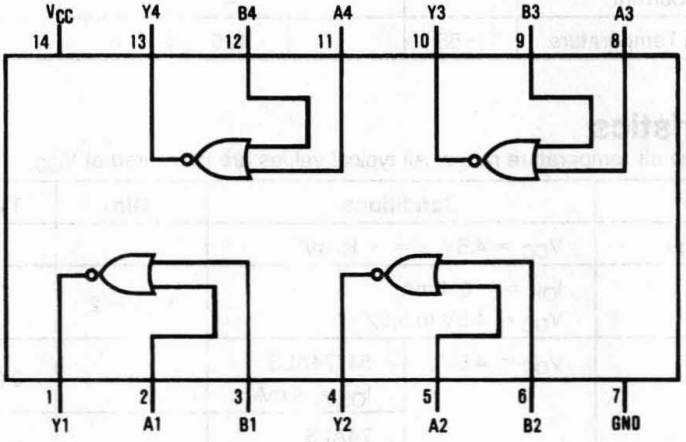
This device contains four independent gates, each of which performs the logic NOR function.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced, oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with LS TTL counterpart
- Improved AC performance over LS28
- Improved line receiving characteristics

Connection Diagram

Dual-In-Line Package



TL/F/6188–1

Order Number DM54ALS28AJ, DM74ALS28AM or DM74ALS28AN
See NS Package Number J14A, M14A or N14A

Function Table

$$Y = \overline{A+B}$$

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS28A	−55°C to +125°C
DM74ALS28A	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS28A			DM74ALS28A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, V_{IL} = V_{IL} Max	54ALS I_{OH} = −1 mA	2.4	3.2		V
			74ALS I_{OH} = −2.6 mA	2.4	3.3		V
		I_{OH} = −400 μA	54/74ALS	V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, V_{IH} = 2V	54/74ALS I_{OL} = 12 mA		0.25	0.4	V
			74ALS I_{OL} = 24 mA		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = 5.5V, V_I = 0V			1.7	2.8	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = 5.5V, V_I = 4.5V			4.8	9	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	DM54ALS28A		DM74ALS28A		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V, R_L = 500Ω, C_L = 50 pF	1	6	2	8	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		1	10	2	7	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM54ALS30A/DM74ALS30A 8-Input NAND Gate

General Description

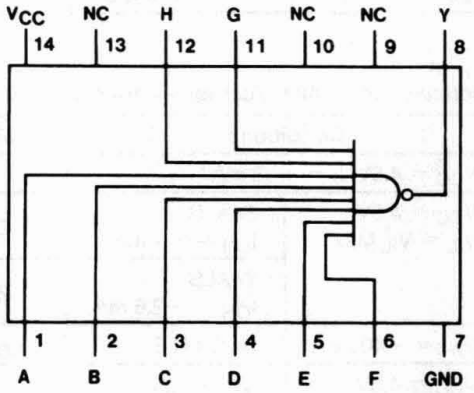
This device contains a single gate, which performs the logic NAND function.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky and low power Schottky TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts

Connection Diagram

Dual-In-Line Package



TL/F/6189–1

Order Number DM54ALS30AJ, DM74ALS30AM or DM74ALS30AN
See NS Package Number J14A, M14A or N14A

Function Table

$$Y = \overline{ABCDEFGH}$$

Inputs A thru H	Output Y
All Inputs H	L
One or More Input L	H

H = High Logic Level

L = Low Logic Level

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS30A			DM74ALS30A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		0.22	0.36	mA
			Outputs Low		0.54	0.90	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	DM54ALS30A		DM74ALS30A		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	3	15	3	10	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		3	15	3	12	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM54ALS32/DM74ALS32 Quad 2-Input OR Gates

General Description

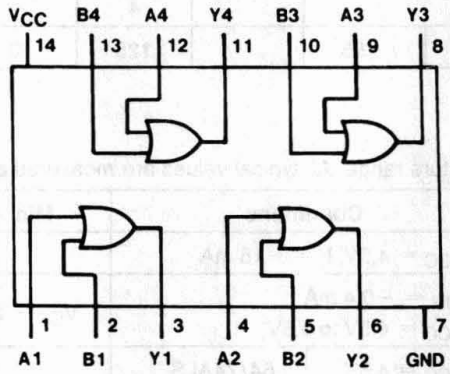
This device contains four independent gates, each of which performs the logic OR function.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky and low power Schottky TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts

Connection Diagram

Dual-In-Line Package



TL/F/6190–1

Order Number DM54ALS32J, DM74ALS32M or DM74ALS32N
See NS Package Number J14A, M14A or N14A

Function Table

$$Y = A + B$$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

H = High Logic Level

L = Low Logic Level

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS32			DM74ALS32			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Input Current @ Max. Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		1.9	4	mA
			Outputs Low		2.6	4.9	mA

Switching Characteristics

over recommended operating free air temperature range (Note 1).

Symbol	Parameter	Conditions	DM54ALS32		DM74ALS32		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	3	18	3	14	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		3	16	3	12	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM54ALS33A/DM74ALS33A Quadruple 2-Input NOR Buffers with Open-Collector Outputs

General Description

This device contains four independent gates, each of which performs the logic NOR function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

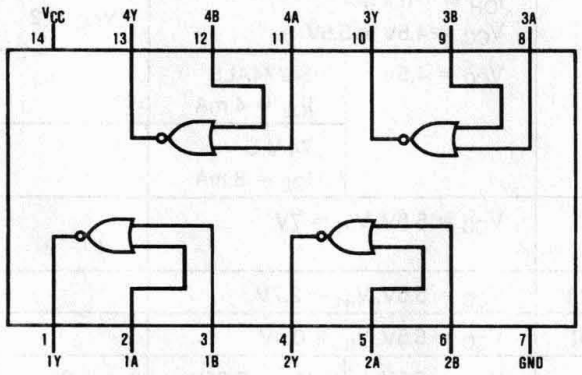
$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with LS TTL counterpart
- Improved AC performance over LS33
- Improved line receiving characteristics

Connection Diagram

Dual-In-Line Package



TL/F/6191–1

Order Number DM54ALS33AJ, DM74ALS33AM or DM74ALS33AN
See NS Package Number J14A, M14A or N14A

Function Table

$$Y = \overline{A + B}$$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level

L = Low Logic Level

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
High Level Output Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS33A			DM74ALS33A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
I_{OH}	High Level Output Current	V_{CC} = 4.5V, V_{OH} = 5.5V				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, V_{IH} = 2V	54/74ALS I_{OL} = 12 mA		0.25	0.4	V
			74ALS I_{OL} = 24 mA		0.35	0.5	V
I_I	Input Current @ Max. Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = 5.5V, V_I = 0V			1.7	2.8	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = 5.5V, V_I = 4.5V			4.8	9	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	DM54ALS33A		DM74ALS33A		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V, R_L = 680Ω, C_L = 50 pF	10	59	10	33	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		2	18	2	12	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM54ALS37A/DM74ALS37A Quadruple 2-Input NAND Buffers

General Description

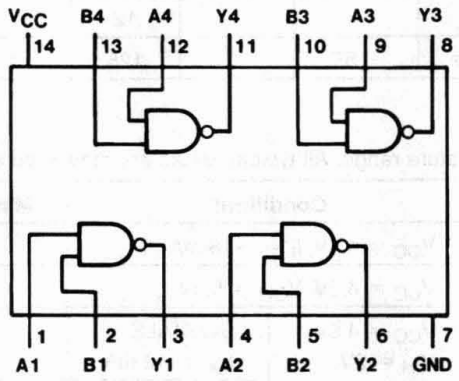
This device contains four independent gates, each of which performs the logic NAND function.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with LS TTL counterpart
- Improved AC performance over LS37
- Improved line receiving characteristics

Connection Diagram

Dual-In-Line Package



TL/F/6192–1

Order Number DM54ALS37AJ, DM74ALS37AM or DM74ALS37AN
See NS Package Number J14A, M14A or N14A

Function Table

$$Y = \overline{AB}$$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS37A			DM74ALS37A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, V_{IL} = Max	54ALS I_{OH} = −1 mA	2.4	3.2		V
			74ALS I_{OH} = −2.6 mA	2.4	3.3		V
		I_{OH} = −400 μA	54/74ALS	V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, V_{IH} = 2V	54/74ALS I_{OL} = 12 mA		0.25	0.4	V
			74ALS I_{OL} = 24 mA		0.35	0.5	V
I_I	Input Current @ Max. Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = 5.5V, V_I = 0V			0.86	1.6	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = 5.5V, V_I = 4.5V			4.0	7.8	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	DM54ALS37A		DM74ALS37A		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V, R_L = 500Ω, C_L = 50 pF	2	17	2	8	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		2	10	2	7	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM54ALS38A/DM74ALS38A Quadruple 2-Input NAND Buffers with Open-Collector Outputs

General Description

This device contains four independent gates, each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

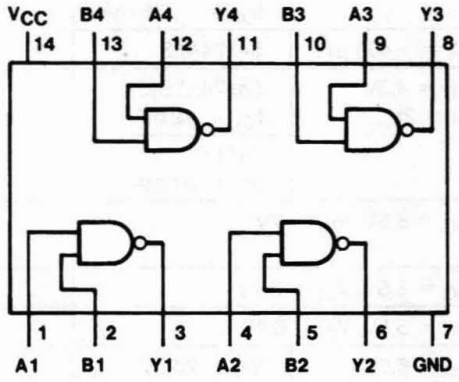
$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with LS TTL counterpart
- Improved AC performance over LS38
- Improved line receiving characteristics

Connection Diagram

Dual-In-Line Package



TL/F/6193–1

Order Number DM54ALS38AJ, DM74ALS38AM or DM74ALS38AN
See NS Package Number J14A, M14A or N14A

Function Table

$$Y = \overline{AB}$$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level

L = Low Logic Level

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
High Level Output Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS38A			DM74ALS38A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
I_{OH}	High Level Output Current	V_{CC} = 4.5V, V_{OH} = 5.5V				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, V_{IH} = 2V	54/74ALS I_{OL} = 12 mA		0.25	0.4	V
			74ALS I_{OL} = 24 mA		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = 5.5V, V_I = 0V			0.86	1.6	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = 5.5V, V_I = 4.5V			4.0	7.8	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	DM54ALS38A		DM74ALS38A		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V, R_L = 680Ω, C_L = 50 pF	10	59	10	33	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		2	18	2	12	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM54ALS40A/DM74ALS40A Dual 4-Input NAND Buffers

General Description

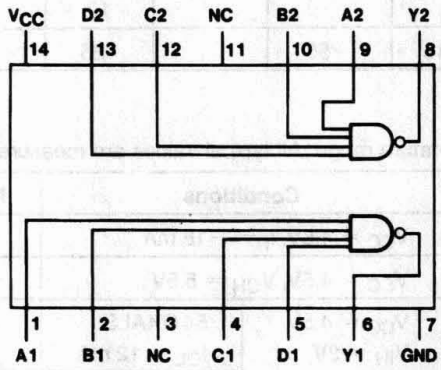
This device contains two independent gates, each of which performs the logic NAND function.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with LS TTL counterpart
- Improved AC performance over LS40
- Improved line receiving characteristics

Connection Diagram

Dual-In-Line Package



TL/F/6194–1

Order Number DM54ALS40AJ, DM74ALS40AM or DM74ALS40AN
See NS Package Number J14A, M14A or N14A

Function Table

$$Y = \overline{ABCD}$$

Inputs				Output
A	B	C	D	Y
X	X	X	L	H
X	X	L	X	H
X	L	X	X	H
L	X	X	X	H
H	H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS40A			DM74ALS40A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, V_{IL} = V_{IL} Max	54ALS, I_{OH} = −1 mA	2.4	3.2		V
			74ALS, I_{OH} = −2.6 mA	2.4	3.3		V
		I_{OH} = −400 μA	54/74ALS	V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, V_{IH} = 2V	54/74ALS, I_{OL} = 12 mA		0.25	0.4	V
			74ALS, I_{OL} = 24 mA		0.35	0.5	V
I_I	Input Current @ Max. Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = 5.5V, V_I = 0V			0.43	0.8	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = 5.5V, V_I = 4.5V			2.4	3.9	mA

Switching Characteristics

over recommended operating free air temperature range (Note 1).

Symbol	Parameter	Conditions	DM54ALS40A		DM74ALS40A		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V, R_L = 500Ω, C_L = 50 pF	2	10	2	8	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		2	10	2	7	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM54ALS74A/DM74ALS74A Dual D Positive-Edge-Triggered Flip-Flops with Preset and Clear

General Description

The 'ALS74A contains two independent positive edge-triggered flip-flops. Each flip-flop has individual D, clock, clear and preset inputs, and also complementary Q and $\overline{Q}$ outputs.

Information at input D is transferred to the Q output on the positive going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. When the clock input is at either the high or low level, the D input signal has no effect.

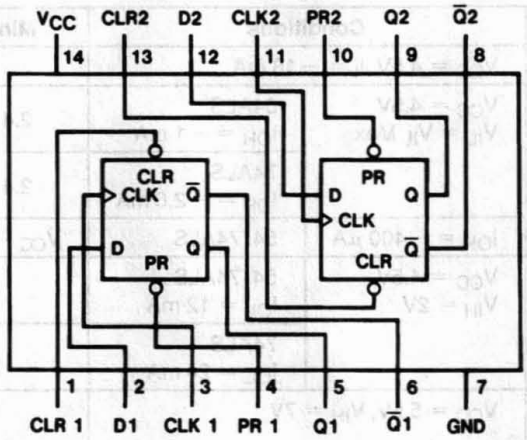
Asynchronous preset and clear inputs will set or clear Q output respectively upon the application of low level signal.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin-for-pin compatible with Schottky and LS TTL counterpart
- Improved AC performance over LS74 at approximately half the power

Connection Diagram

Dual-In-Line Package



TL/F/6109–1

Order Number DM54ALS74AJ, DM74ALS74AM or DM74ALS74AN
See NS Package Number J14A, M14A or N14A

Function Table

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

L = Low State, H = High State, X = Don't Care

↑ = Positive Edge Transition

Q_0 = Previous Condition of Q

* = This condition is nonstable; it will not persist when preset and clear inputs return to their inactive (high) level. The output levels in this condition are not guaranteed to meet the V_{OH} specification.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54ALS74A			DM74ALS74A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency		0		30	0		34	MHz
$t_{W(CLK)}$	Width of Clock Pulse	High	17.5			14.5			ns
		Low	17.5			14.5			ns
t_W	Pulse Width Preset & Clear	Low	15			14.5			ns
t_{SU}	Data Setup Time	Data	16 ↑			15 ↑			ns
		PRE or CLR Inactive	10 ↑			10 ↑			
t_H	Data Hold Time		2 ↑			0 ↑			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −400 μA V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V	Clock, D			0.1	mA
			Preset, Clear			0.2	
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V	Clock, D			20	μA
			Preset, Clear			40	
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V	Clock, D			−0.2	mA
			Preset, Clear			−0.4	
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V (Note 1)			2.4	4	mA

Note 1: I_{CC} is measured with D, CLK and PRESET grounded, then with D, CLK and CLEAR grounded.

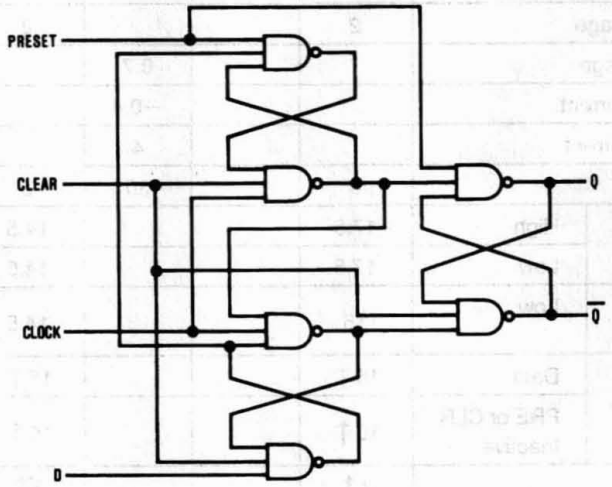
Switching Characteristics

over recommended operating free air temperature range (Note 1).

Parameter	Conditions	From	To	DM54ALS74A		DM74ALS74A		Units
				Min	Max	Min	Max	
f_{MAX}	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF			30		34		MHz
t_{PLH}		Preset or Clear	Q or $\overline{Q}$	3	18	3	13	ns
t_{PHL}				5	17	5	15	ns
t_{PLH}		Clock	Q or $\overline{Q}$	5	23	5	16	ns
t_{PHL}				5	20	5	18	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6109–2

National Semiconductor Corporation

PRELIMINARY

DM54ALS86/DM74ALS86 Quad 2-Input Exclusive-OR Gates

General Description

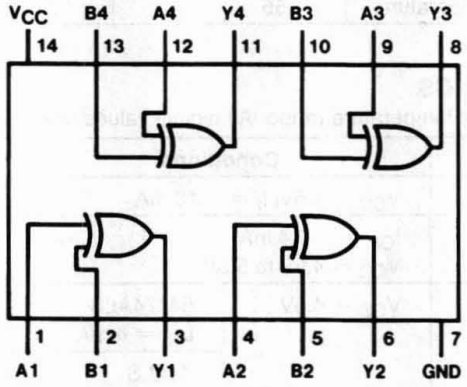
This device contains four independent gates, each of which performs the logic exclusive-OR function.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky and low power Schottky TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts

Connection Diagram

Dual-In-Line Package



TL/F/6195–1

Order Number DM54ALS86J, DM74ALS86M or DM74ALS86N
See NS Package Number J14A, M14A or N14A

Function Table

$$Y = A \oplus B = \overline{A}B + A\overline{B}$$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

2

This document contains information on a product under development. NSC reserves the right to change or discontinue this product without notice.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS86			DM74ALS86			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Input Current @ Max. Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V, All Inputs at 4.5V			3.9	5.9	mA

Switching Characteristics

over recommended operating free air temperature range (Note 1).

Symbol	Parameter	Conditions		DM54ALS86		DM74ALS86		Units
				Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	(Note 2)	A or B to Y Other Input Low	3	22	3	17	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			2	14	2	12	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		A or B to Y Other Input High	3	22	3	17	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			2	12	2	10	ns

Note 1: See Section 1 for test waveforms and output load.

Note 2: V_{CC} = 4.5V to 5.5V, R_L = 500Ω, C_L = 50 pF.

National Semiconductor Corporation

DM54ALS109A/DM74ALS109A Dual J-$\overline{K}$ Positive-Edge-Triggered Flip-Flops with Preset and Clear

General Description

The DM54ALS109A is a dual edge-triggered flip-flop. Each flip-flop has individual J, $\overline{K}$, clock, clear and preset inputs, and also complementary Q and $\overline{Q}$ outputs.

Information at input J or $\overline{K}$ is transferred to the Q output on the positive going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. When the clock input is at either the high or low level, the J, $\overline{K}$ input signal has no effect.

Asynchronous preset and clear inputs will set or clear Q output respectively upon the application of low level signal.

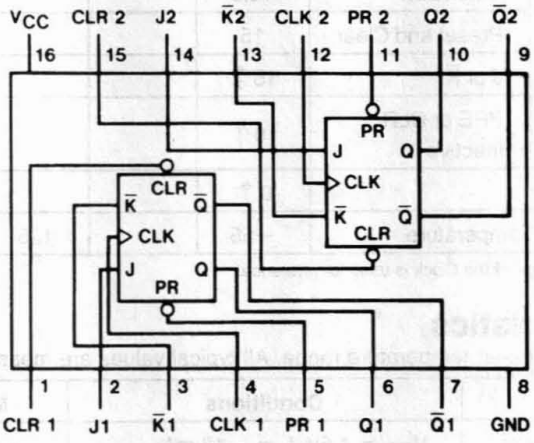
The J-$\overline{K}$ design allows operation as a D flip-flop by tying the J and $\overline{K}$ inputs together.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky and LS TTL counterpart
- Improved AC performance over LS109 at approximately half the power

Connection Diagram

Dual-In-Line Package



TL/F/6196–1

Order Number DM54ALS109AJ, DM74ALS109AM or DM74ALS109AN
See NS Package Number J16A, M16A or N16A

Function Table

Inputs					Outputs	
PR	CLR	CK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

L = Low State, H = High State, X = Don't Care

↑ = Positive Edge Transition, Q_0 = Previous Condition of Q

*This condition is nonstable; it will not persist when present and clear inputs return to their inactive (high) level. The output levels in this condition are not guaranteed to meet the V_{OH} specification.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54ALS109A			DM74ALS109A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency		0		30	0		34	MHz
$t_{W(CLK)}$	Pulse Width	Clock High	16.5			14.5			ns
		Clock Low	16.5			14.5			ns
t_W	Pulse Width	Preset and Clear	15			15			ns
t_{SU}	Data Setup Time	J or $\overline{K}$	15 ↑			15 ↑			ns
		PRE or CLR inactive	10 ↑			10 ↑			
t_H	Data Hold Time		0 ↑			0 ↑			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics

over recommended operating free-air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −400 μA V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V	Clock, J, $\overline{K}$			0.1	mA
			Preset, Clear			0.2	
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V	Clock, J, $\overline{K}$			20	μA
			Preset, Clear			40	
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V	Clock, J, $\overline{K}$			−0.2	mA
			Preset, Clear			−0.4	
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V (Note 1)			2.4	4	mA

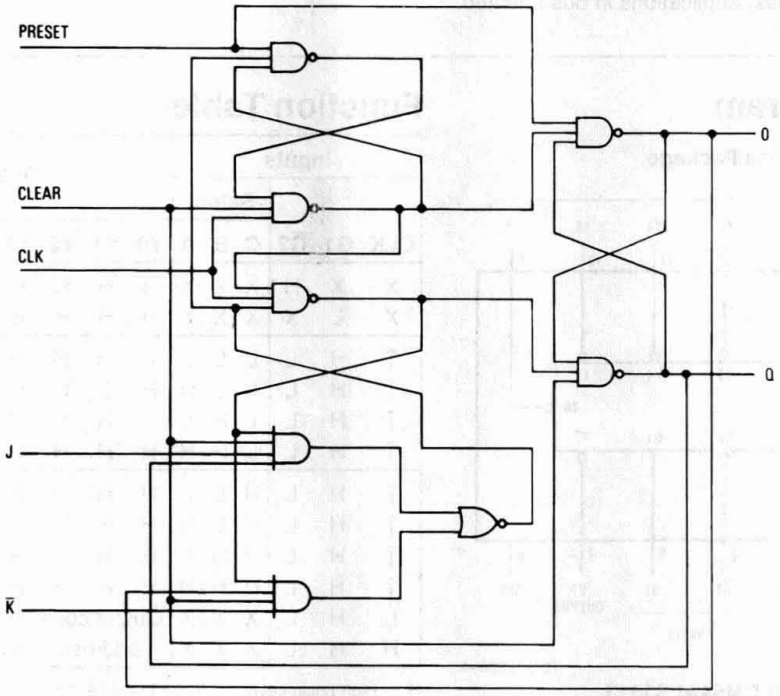
Note 1: I_{CC} is measured with J, $\overline{K}$, CLK and PRESET grounded, then with J, $\overline{K}$, CLK and CLEAR grounded.

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From	To	DM54ALS109A		DM74ALS109A		Units
					Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF			30		34		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output		Preset or Clear	Q or $\overline{Q}$	3	17	3	13	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Preset or Clear	Q or $\overline{Q}$	5	17	5	15	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		Clock	Q or $\overline{Q}$	5	21	5	16	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Clock	Q or $\overline{Q}$	5	20	5	18	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6196–2

National Semiconductor Corporation

DM54ALS131/DM74ALS131 3 to 8 Line Decoder/Demultiplexer with Address Register

General Description

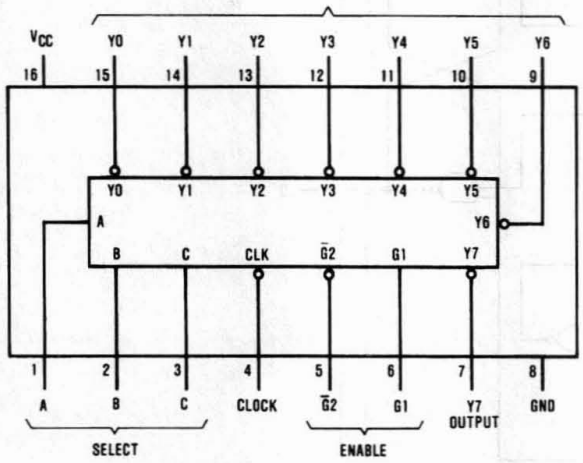
The ALS131 is a three-line to eight-line decoder/demultiplexer with registers on the three address inputs. When the clock transitions from low to high, the address present at the select inputs (A, B, and C) is stored in the latches. The output enable controls, G1 and $\overline{G2}$, control the state of the outputs independently of the select or clock inputs. All of the outputs are high unless G1 is high and $\overline{G2}$ is low. The ALS131 is ideally suited for implementing glitch-free decoders in strobed (stored-address) applications in bus-oriented systems.

Features

- Combines decoder and 3-bit address register
- Incorporates 2 enable inputs to simplify cascading
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process

Connection Diagram

Dual-In-Line Package



TL/F/6200–1

Order Number DM54ALS131J, DM74ALS131M or DM74ALS131N
See NS Package Number J16A, M16A or N16A

Function Table

Inputs						Outputs							
			Select										
CLK	G1	$\overline{G2}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
↑	H	L	L	L	L	L	H	H	H	H	H	H	H
↑	H	L	L	L	H	H	L	H	H	H	H	H	H
↑	H	L	L	H	L	H	H	L	H	H	H	H	H
↑	H	L	L	H	H	H	H	H	L	H	H	H	H
↑	H	L	H	L	L	H	H	H	H	L	H	H	H
↑	H	L	H	L	H	H	H	H	H	H	L	H	H
↑	H	L	H	H	L	H	H	H	H	H	H	L	H
↑	H	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	X	X	X	Output corresponding to stored address, L; all others, H.							
H	H	L	X	X	X								

H = High Logic Level, L = Low Logic Level, X = Don't Care

↑ = Transition from Low to High Level

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54ALS131			DM74ALS131			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLOCK}	Clock Frequency		0		40	0		50	MHz
t_{WCLK}	Width of Enabling Pulse, (High or Low)		12.5			10			ns
t_{SU}	Setup Time	A, B, C	15↑			10↑			ns
t_H	Hold Time	A, B, C	0↑			0↑			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

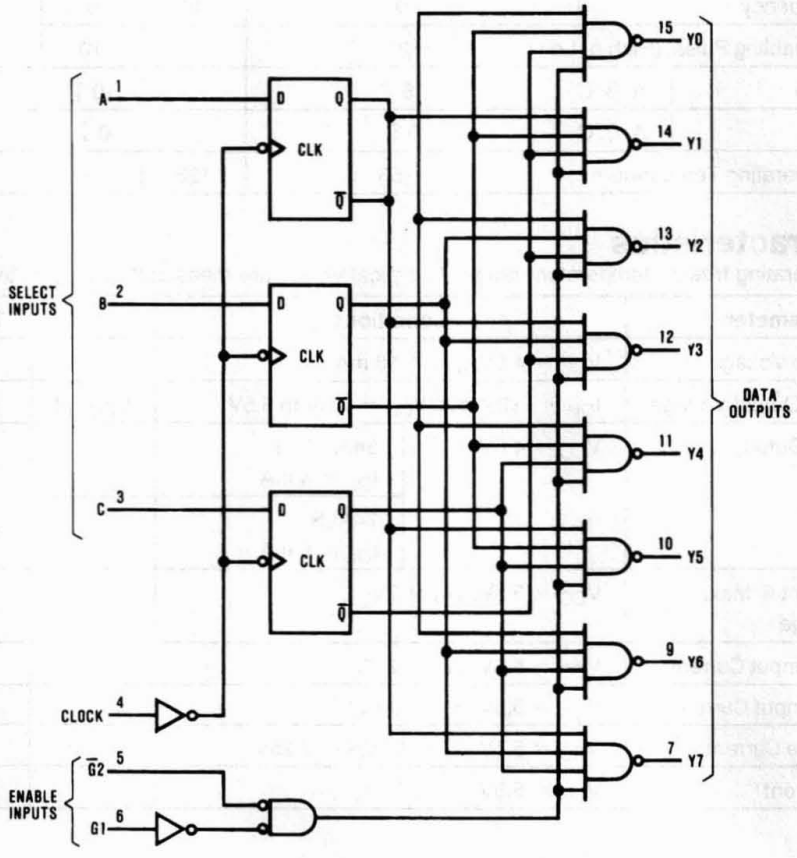
Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA, V_{CC} = 4.5V to 5.5V		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Input Current @ Max. Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V			5	11	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

Symbol	Parameter	Conditions	From (Input) to (Output)	DM54ALS131		DM74ALS131		Units
				Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF		40		50		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output		$\overline{G2}$ to Y	5	18	5	15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		$\overline{G2}$ to Y	5	18	5	15	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		G1 to Y	7	24	7	20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		G1 to Y	6	20	6	17	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		Clock to Y	8	28	8	25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Clock to Y	7	24	7	20	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6200–2

National Semiconductor Corporation

DM54ALS132/DM74ALS132 Quad 2-Input NAND Gates with Schmitt Trigger Inputs

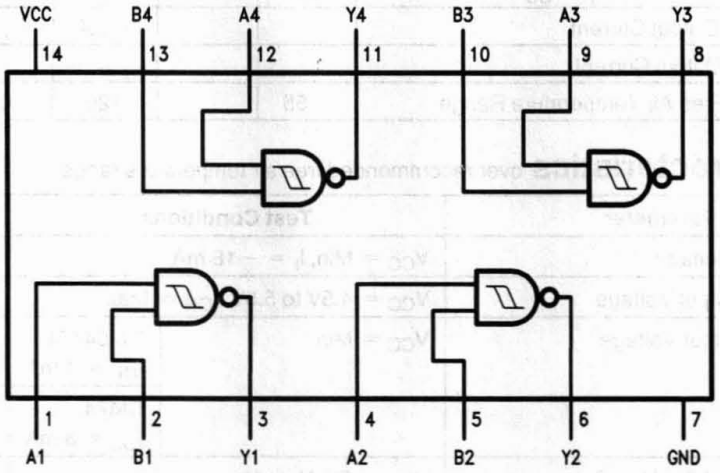
General Description

This device contains four independent gates, each of which performs the logic NAND function. Each input has hysteresis which increases the noise immunity and transforms a slowly changing input signal to a fast changing, jitter-free output.

Features

- Switching specification at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin-for-pin compatible with Schottky and Low Power Schottky TTL counterparts
- Improved AC performance over low power Schottky counterpart

Connection Diagram



TL/F/8771–1

Order Number DM54ALS132J, DM74ALS132M or DM74ALS132N
See NS Package Number J14A, M14A or N14A

Function Table

$$Y = \overline{AB}$$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level

L = Low Logic Level

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage 7V

Input Voltage 7V

Operating Free Air Temperature Range

DM54ALS −55°C to +125°C

DM74ALS 0°C to +70°C

Storage Temperature Range −65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54ALS132			DM74ALS132			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.5	5	5.5	V
V_{T+}	Positive-Going Input Threshold Voltage	V_{CC} = Min to Max	1.4		2	1.4		2	V
		V_{CC} = 5V	1.55		1.85	1.55		1.85	
V_{T-}	Negative-Going Input Threshold Voltage	V_{CC} = Min to Max	0.75		1.2	0.75		1.2	V
		V_{CC} = 5V	0.85		1.1	0.85		1.1	
HYS	Input Hysteresis	V_{CC} = Min to Max	0.5			0.5			V
		V_{CC} = 5V	0.6			0.6			
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
T_A	Operating Free Air Temperature Range		−55		125	0		70	°C

Electrical Characteristics over recommended free air temperature range

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V, I_{OH} = Max		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min	DM54/74 I_{OL} = 4 mA		0.25	0.4	V
			DM74 I_{OL} = 8 mA		0.35	0.5	
I_{T+}	Input Current at Positive-Going Threshold Voltage	V_{CC} = 5V, V_I = V_{T+}				20	μA
I_{T-}	Input Current at Negative-Going Threshold Voltage	V_{CC} = 5V, V_I = V_{T-}				−100	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 7V				100	μA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−100	μA
I_O	Output Drive Current	V_{CC} = Max, V_O = 2.25V		−30		−112	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max				8	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max				8	mA

Switching Characteristics over recommended operating free air temperature range

Symbol	Parameter	Conditions (Note 1)	DM54ALS132		DM74ALS132		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V RL = 500Ω, CL = 50 pF	2	13	2	12	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		2	12	2	11	

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM54ALS133/DM74ALS133 13-Input NAND Gate

General Description

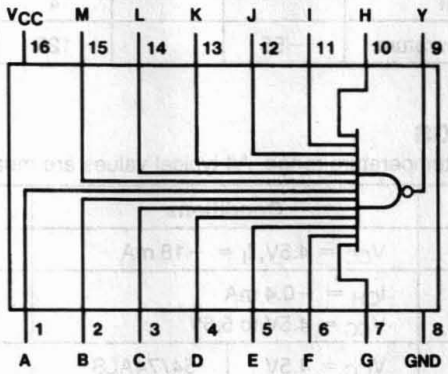
This device contains a single gate, which performs the logic NAND function.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky and low power Schottky TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts

Connection Diagram

Dual-In-Line Package



TL/F/6201–1

Order Number DM54ALS133J, DM74ALS133M or DM74ALS133N
See NS Package Number J16A, M16A or N16A

Function Table

$$Y = \overline{ABCDEFGHIJKLM}$$

Inputs	Output
A thru M	Y
All Inputs H	L
One or More Input L	H

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS133			DM74ALS133			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		0.24	0.34	mA
			Outputs Low		0.56	0.8	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	DM54ALS133		DM74ALS133		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	1	16	3	11	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		5	47	5	25	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

PRELIMINARY

DM54ALS136/DM74ALS136 Quad 2-Input Exclusive-OR Gates with Open-Collector Outputs

General Description

This device contains four independent gates, each of which performs the logic exclusive-OR function. The open-collector outputs require external pull-up resistors for proper logical operation.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with LS TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

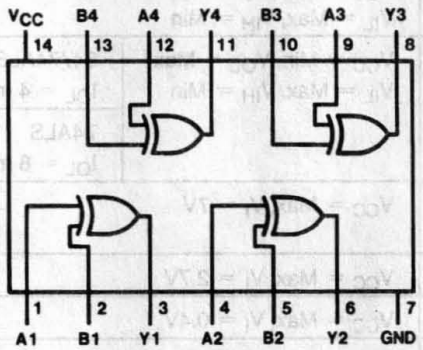
Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Connection Diagram

Dual-In-Line Package



TL/F/9161–1

Order Number DM54ALS136J, DM74ALS136M or DM74ALS136N
See NS Package Number J14A, M14A or N14A

Function Table

$$Y = A \oplus B$$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = High Logic Level

L = Low Logic Level

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
High Level Output Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS136			DM74ALS136			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max, V_{IH} = Min				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{OL} = Max, V_{IL} = Max, V_{IH} = Min	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.1	mA
I_{CC}	Supply Current	V_{CC} = Max, (Note 1)			3.9	5.9	mA

Switching Characteristics over recommended operating free air temperature range

Symbol	Parameter	Conditions	DM54ALS136		DM74ALS136		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 2 kΩ C_L = 50 pF Other Input Low	20	55	20	50	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		3	18	3	15	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 2 kΩ C_L = 50 pF Other Input High	20	55	20	50	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		3	15	3	12	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: I_{CC} is measured with all inputs at 4.5V and the outputs open.

National Semiconductor Corporation

DM54ALS137/DM74ALS137 3 to 8 Line Decoder/Demultiplexer with Address Latches

General Description

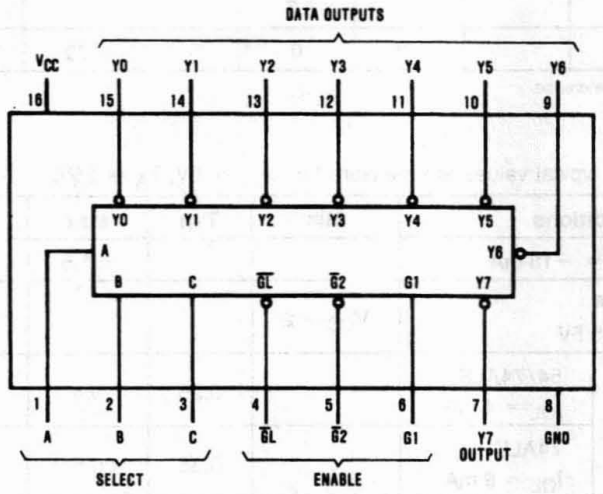
The ALS137 is a three line to eight line decoder/demultiplexer with latches on the three address inputs. When the latch-enable input ($\overline{GL}$) is low, the ALS137 acts as a decoder/demultiplexer. When $\overline{GL}$ goes from low to high, the address present at the select inputs (A, B, and C) is stored in the latches. Further address changes are ignored as long as $\overline{GL}$ remains high. The output enable controls, G1 and $\overline{G2}$, control the state of the outputs independently of the select or latch-enable inputs. All of the outputs are high unless G1 is high and $\overline{G2}$ is low. The ALS137 is ideally suited for implementing glitch-free decoders in strobed (stored-address) applications in bus-oriented systems.

Features

- Combines decoder and 3-bit address latch
- Incorporates 3 enable inputs to simplify cascading
- Low power dissipation .....28 mW typ
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process

Connection Diagram

Dual-In-Line Package



TL/F/6202–1

Order Number DM54ALS137J, DM74ALS137M or DM74ALS137N
See NS Package Number J16A, M16A or N16A

Function Table

Inputs						Outputs							
Enable			Select										
$\overline{GL}$	G1	$\overline{G2}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	Output corresponding to stored address, L; all others, H							

L = Low State, H = High State, X = Don't Care

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54ALS137			DM74ALS137			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
t_W	Width of Enabling Pulse	$\overline{GL}$ Low	15			10			ns
t_{SU}	Setup Time	A, B, C	15 ↑			10 ↑			ns
t_H	Hold Time	A, B, C	5 ↑			5 ↑			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

The arrow (↑) indicates the positive edge of the $\overline{GL}$ input pulse is used for reference.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA, V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Input Current @ Max. Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V	Enable			0.1	mA
			A, B, C			0.1	
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V	Enable			20	µA
			A, B, C			20	
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V	Enable			−0.1	mA
			A, B, C			−0.1	
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V			5	11	mA

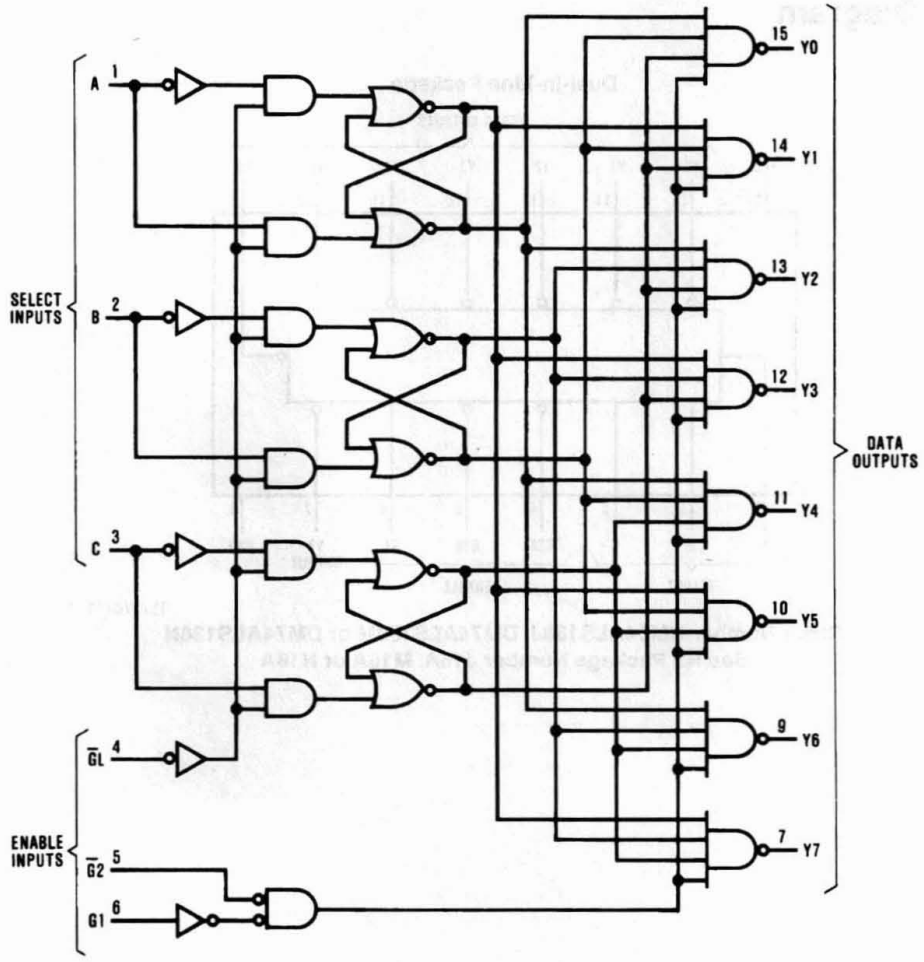
Switching Characteristics

over recommended operating free air temperature range (Note 1).

Symbol	Parameter	Conditions	From (Input) To (Output)	DM54ALS137		DM74ALS137		Units
				Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	A, B, C to Y	5	25	5	20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		A, B, C to Y	6	25	6	20	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		$\overline{G2}$ to Y	4	15	4	12	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		$\overline{G2}$ to Y	5	18	5	15	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		G1 to Y	5	21	5	17	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		G1 to Y	5	19	5	15	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		$\overline{GL}$ to Y	7	27	7	22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		$\overline{GL}$ to Y	7	25	7	20	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6202–2

National Semiconductor Corporation

DM54ALS138/DM74ALS138
3 to 8 Line Decoder/Demultiplexer

General Description

These Schottky-clamped circuits are designed to be used in high-performance memory-decoding or data-routing applications, requiring very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding. When used with high-speed memories, the delay times of these decoders are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The ALS138 decodes one-of-eight lines, based upon the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented with no external inverters, and 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

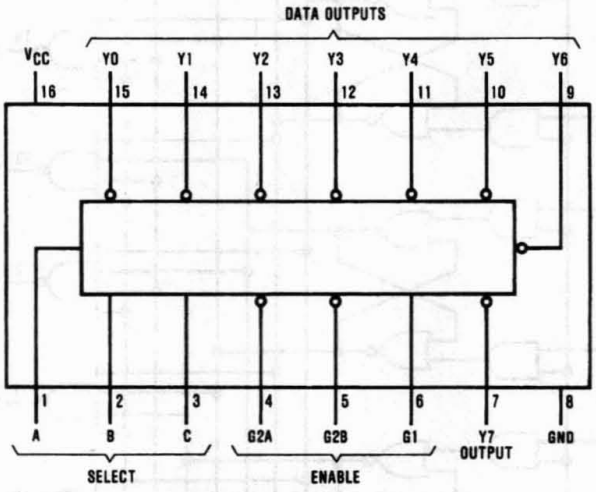
This decoder/demultiplexer features fully buffered inputs, presenting only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and simplify system design.

Features

- Designed specifically for high speed:
  - Memory decoders
  - Data transmission systems
- 3- to 8-line decoder incorporates 3 enable inputs to simplify cascading and/or data reception
- Low power dissipation . . . 23 mW typ
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process

Connection Diagram

Dual-In-Line Package



TL/F/6111–1

Order Number DM54ALS138J, DM74ALS138M or DM74ALS138N
See NS Package Number J16A, M16A or N16A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS138			DM74ALS138			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Input Current @ Max. Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V			5	10	mA

Switching Characteristics

over recommended operating free air temperature range (Note 1).

Symbol	Parameter	Conditions	From (Input) To (Output)	DM54ALS138		DM74ALS138		Units
				Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	A, B, C to Y	2	28	6	22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		A, B, C to Y	6	22	6	18	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		Enable to Y	2	22	4	17	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Enable to Y	4	21	5	17	ns

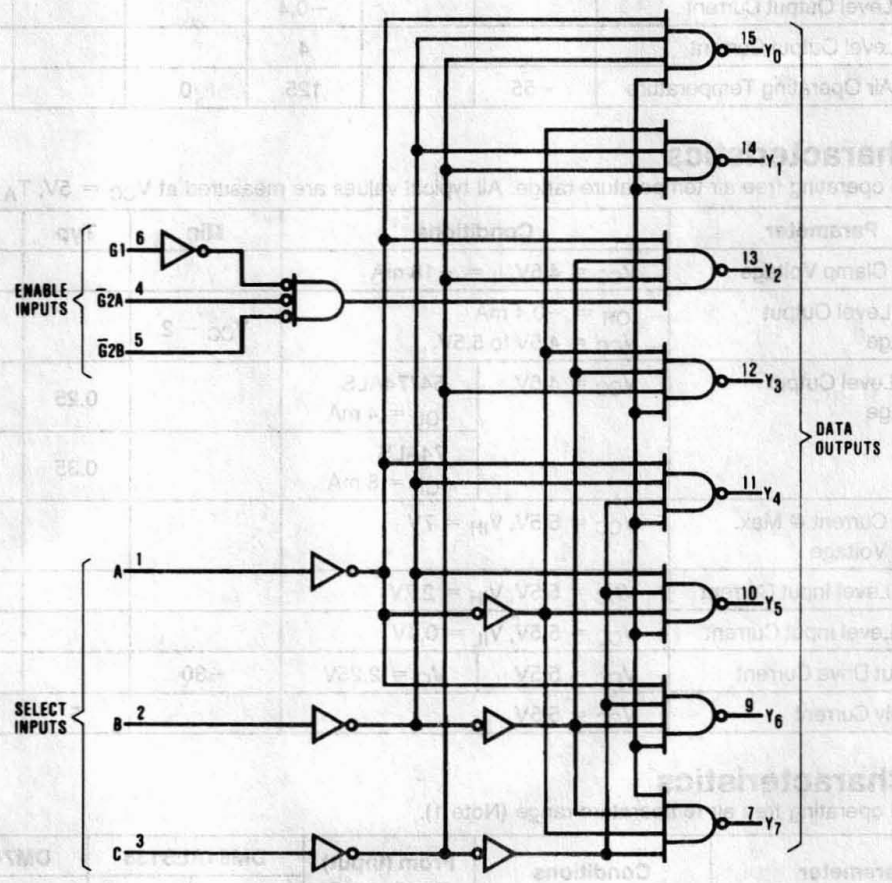
Note 1: See Section 1 for test waveforms and output load.

Function Table

Enable Inputs		Select Inputs			Outputs							
G1	$\overline{G2}$*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*$\overline{G2} = \overline{G2A} + \overline{G2B}$

Logic Diagram



TL/F/6111–2

National Semiconductor Corporation

DM54ALS151/DM74ALS151 1 of 8 Line Data Selector/Multiplexer

General Description

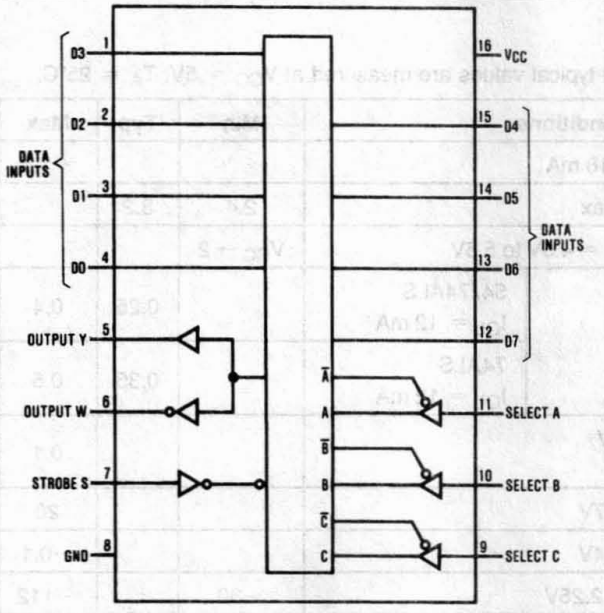
This Data Selector/Multiplexer contains full on-chip decoding to select one-of-eight data sources as a result of a unique three-bit binary code at the Select inputs. Two complementary outputs provide both inverting and non-inverting buffer operation. A Strobe input is provided which, when at the high level, disables all data inputs and forces the Y output to the low state and the W output to the high state. The Select input buffers incorporate internal overlap features to ensure that select input changes do not cause invalid output transients.

Features

- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Switching performance is guaranteed over full temperature and V_{CC} supply range
- Pin and functional compatible with LS family counterpart
- Improved output transient handling capability

Connection Diagram

Dual-In-Line Package



TL/F/6203–1

Order Number DM54ALS151J, DM74ALS151M or DM74ALS151N
See NS Package Number J16A, M16A or N16A

Function Table

Inputs				Outputs	
Select			Strobe		
C	B	A	S	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = High Level, L = Low Level, X = Don't Care
D0 thru D7 = the level of the respective D input

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS151			DM74ALS151			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free-air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

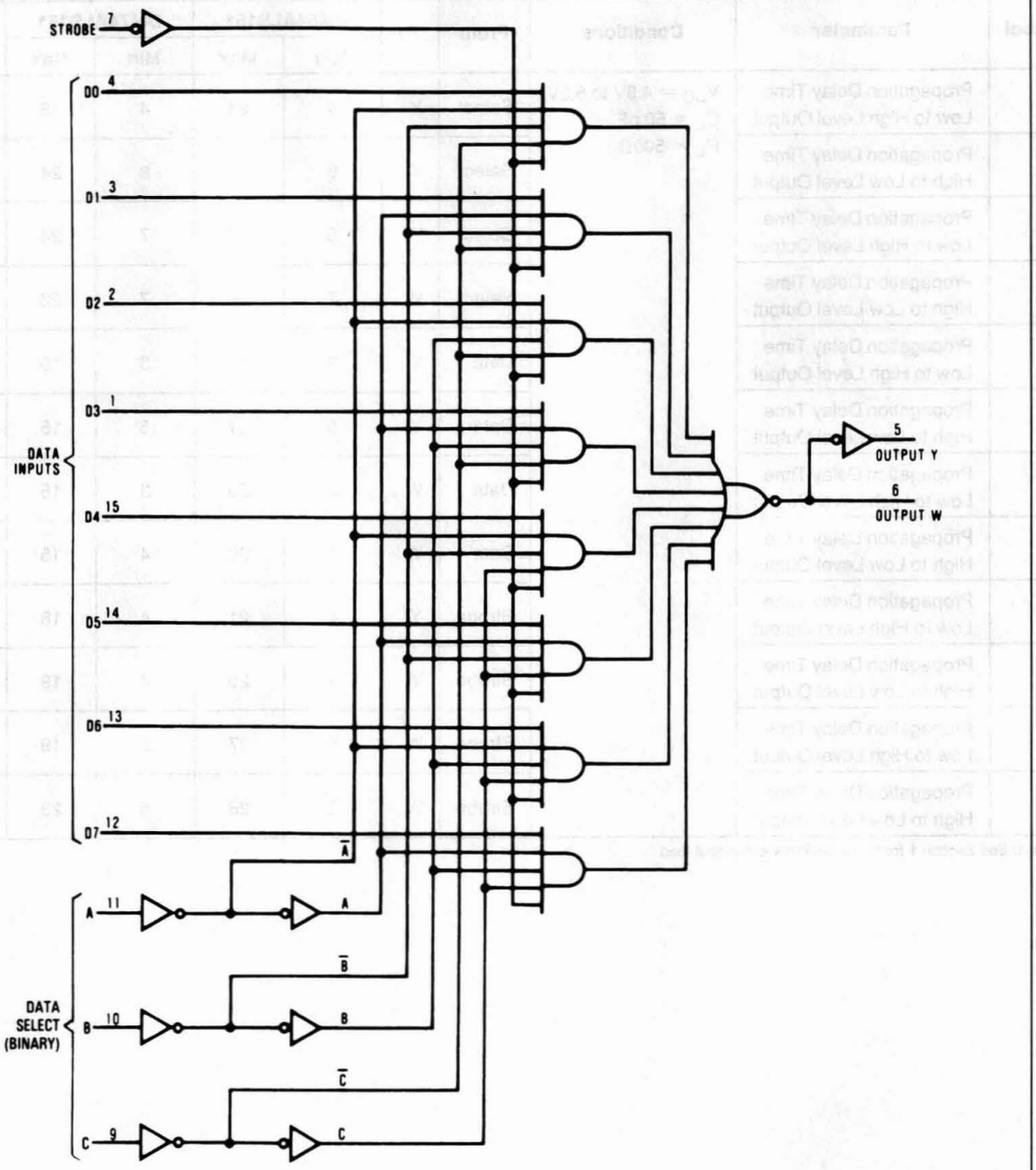
Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, I_{OH} = Max		2.4	3.2		V
		I_{OH} = −400 μA, V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 12 mA		0.25	0.4	V
			74ALS I_{OL} = 12 mA		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IN} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IN} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_{OUT} = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V All Inputs = 4.5V			7.5	12	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From	To	DM54ALS151		DM74ALS151		Units
					Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V C_L = 50 pF R_L = 500Ω	Select	Y	4	21	4	18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Select	Y	8	35	8	24	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		Select	W	5	36	7	24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Select	W	7	26	7	23	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		Data	Y	3	14	3	10	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Data	Y	5	21	5	15	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		Data	W	3	23	3	15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Data	W	4	20	4	15	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		Strobe	Y	4	21	4	18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Strobe	Y	4	25	4	19	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		Strobe	W	5	27	5	19	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Strobe	W	5	26	5	23	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6203–2

National Semiconductor Corporation

DM54ALS153/DM74ALS153 Dual 1 of 4 Line Data Selector/Multiplexer

General Description

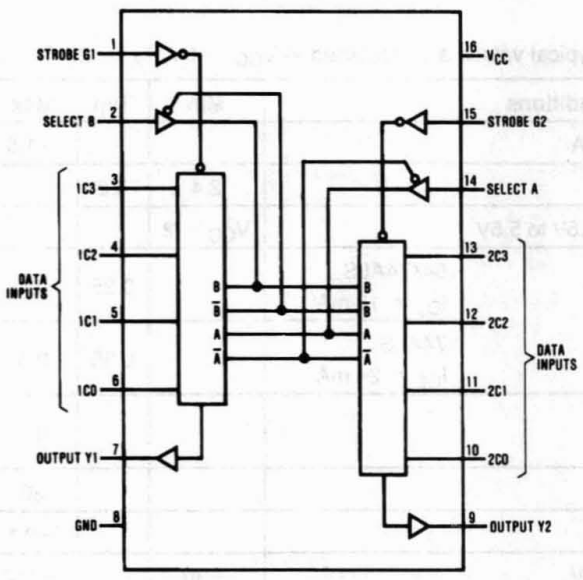
This Data Selector/Multiplexer contains full on-chip decoding to select one-of-four data sources as a result of a unique two-bit binary code at the Select inputs. Each of the two Data Selector/Multiplexer circuits have their own separate Data and Strobe inputs and a non-inverting output buffer. The Select inputs A and B are common to both sections. The Strobe inputs, when at the high level, disable their associated data inputs and force the corresponding output to the low state. The Select input buffers incorporate internal overlap features to ensure that select input changes do not cause invalid output transients.

Features

- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Switching performance is guaranteed over full temperature and V_{CC} supply range
- Pin and functional compatible with LS family counterpart
- Improved output transient handling capability

Connection Diagram

Dual-In-Line Package



TL/F/6204–1

Order Number DM54ALS153J, DM74ALS153M or DM74ALS153N
See NS Package Number J16A, M16A or N16A

Function Table

Select Inputs		Data Inputs				Strobe	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.

H = High Level, L = Low Level, X = Don't Care

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS153			DM74ALS153			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, I_{OH} = Max		2.4	3.2		V
		I_{OH} = −400 μA, V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 12 mA		0.25	0.4	V
			74ALS I_{OL} = 24 mA		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IN} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IN} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_{OUT} = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V All Inputs = 4.5V			7.5	14	mA

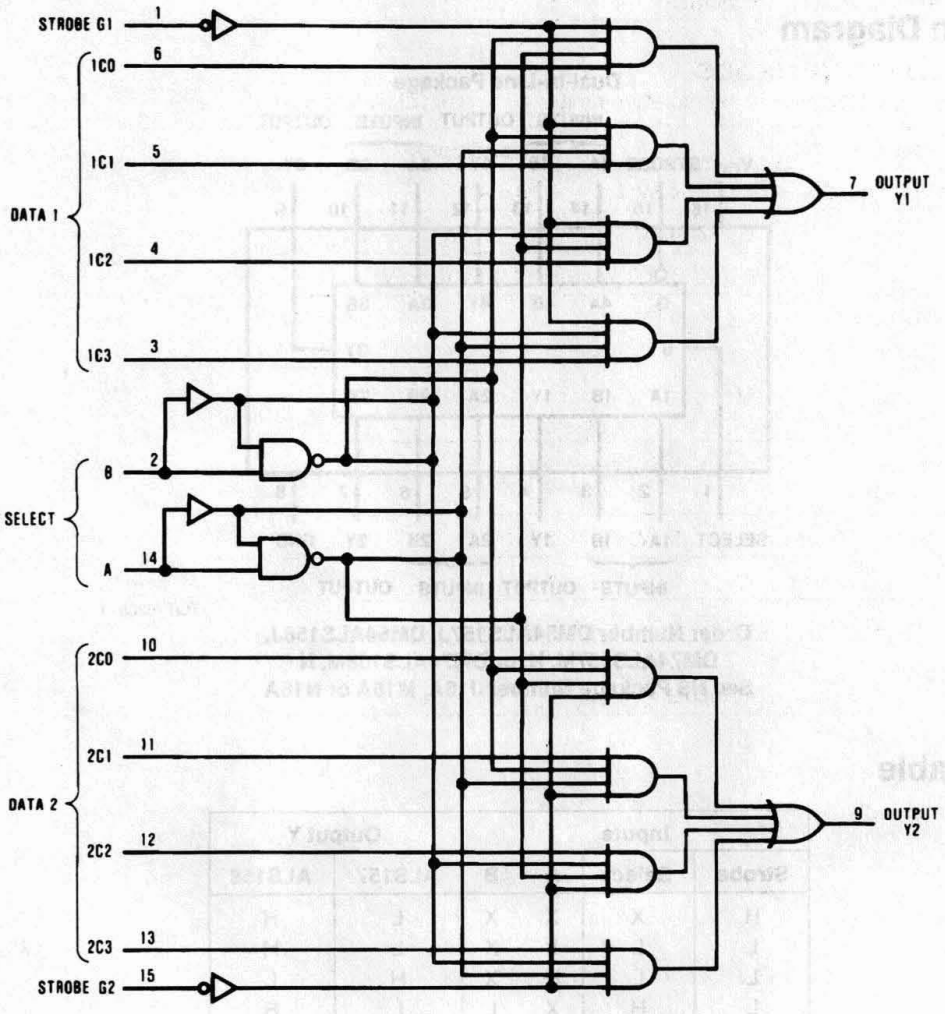
Switching Characteristics

over recommended operating free air temperature range (Note 1).

Symbol	Parameter	Conditions	From	To	DM54ALS153		DM74ALS153		Units
					Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V C_L = 50 pF R_L = 500Ω	Select	Y	5	29	5	21	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Select	Y	5	27	5	21	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		Data	Y	3	15	3	10	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Data	Y	2	18	4	15	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		Strobe	Y	5	27	5	18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Strobe	Y	3	22	5	18	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6204–2

National Semiconductor Corporation

PRELIMINARY

DM54ALS/DM74ALS157,158 Quad 1 of 2 Line Data Selectors/Multiplexers

General Description

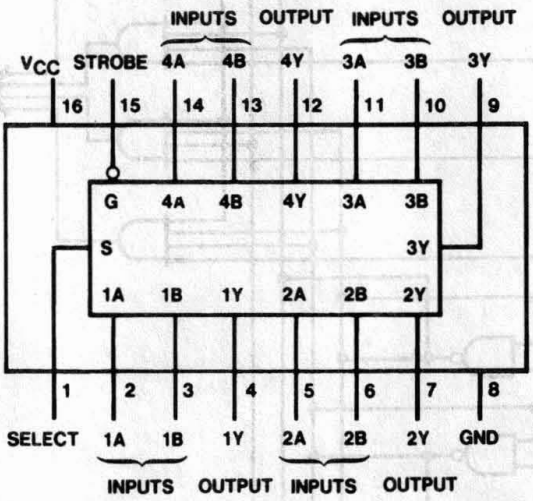
These data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The ALS157 presents true data whereas the ALS158 presents inverted data to minimize propagation delay time.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky and low power Schottky TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts
- Expand any data input point
- Multiplex dual data buses
- General four functions of two variables (one variable is common)

Connection Diagram

Dual-In-Line Package



TL/F/6205–1

Order Number DM54ALS157J, DM54ALS158J, DM74ALS157M, N, or DM74ALS158M, N
See NS Package Number J16A, M16A or N16A

Function Table

Inputs				Output Y	
Strobe	Select	A	B	ALS157	ALS158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = High Level, L = Low Level, X = Don't Care

This document contains information on a product under development. NSC reserves the right to change or discontinue this product without notice.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS157,158			DM74ALS157,158			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA, V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS, I_{OL} = 4 mA		0.25	0.4	V
			74ALS, I_{OL} = 8 mA		0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	54/74ALS157		6	11	mA
		All Inputs = 4.5V	54/74ALS158		5	10	mA

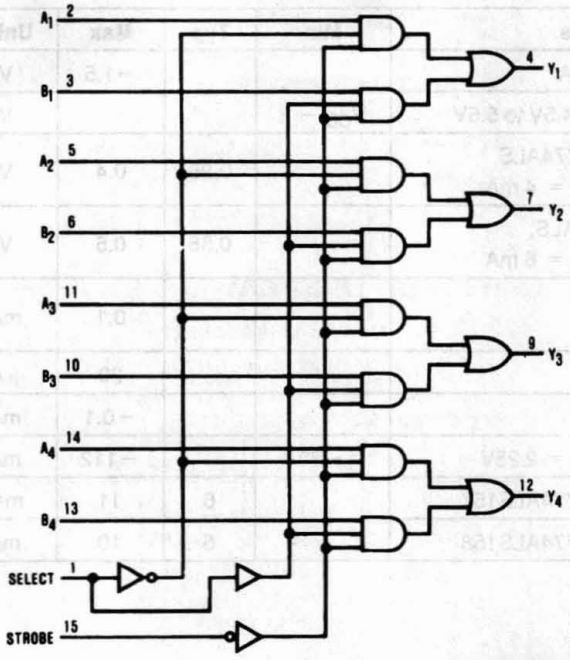
Switching Characteristics

over recommended operating free air temperature range (Note 1).

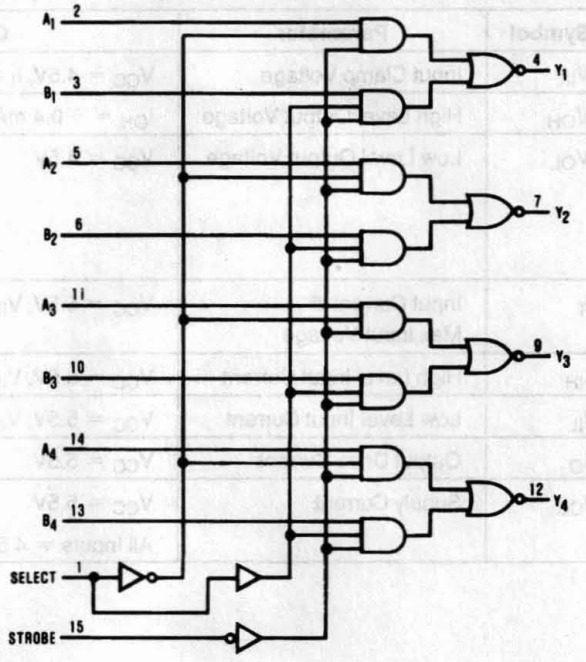
Symbol	Parameter		From (Input) To (Output)	Conditions	DM54ALS157,158		DM74ALS157,158		Units
					Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	157	Data to Y	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R_L = 500Ω	4	17	4	14	ns
		158			4	18	4	15	
t_{PHL}	Propagation Delay Time High to Low Level Output	157			2	15	2	12	ns
		158			2	12	2	8	
t_{PLH}	Propagation Delay Time Low to High Level Output	157	Strobe to Y		7	25	7	20	ns
		158			5	22	5	18	
t_{PHL}	Propagation Delay Time High to Low Level Output	157			4	18	4	13	ns
		158			5	22	5	18	
t_{PLH}	Propagation Delay Time Low to High Level Output	157	Select to Y		7	28	7	24	ns
		158			5	22	5	18	
t_{PHL}	Propagation Delay Time High to Low Level Output	157			4	16	4	13	ns
		158			5	22	5	18	

Note 1: See Section 1 for test waveforms and output load.

Logic Diagrams



TL/F/6205–2



TL/F/6205–3

National Semiconductor Corporation

DM54ALS/DM74ALS160B, 161B, 162B, 163B Synchronous Four-Bit Counters

General Description

These synchronous presettable counters feature an internal carry look ahead for application in high speed counting designs. The ALS160B and ALS162B are four-bit decade counters, while the ALS161B and ALS163B are four-bit binary counters. The ALS160B and ALS161B clear asynchronously, while the ALS162B and ALS163B clear synchronously. The carry output is decoded to prevent spikes during normal counting mode of operation. Synchronous operation is provided by having all flip-flops clocked simultaneously so that outputs change coincident with each other when so instructed by count enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable, that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with set up data after the next clock pulse regardless of the levels of enable input. Low to high transitions at the load input are perfectly acceptable regardless of the logic levels on the clock or enable inputs.

The ALS160B and ALS161B clear function is asynchronous. A low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of clock, load or enable inputs. These two counters are provided with a clear on power-up feature. The ALS162B and ALS163B clear function is synchronous; and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of enable inputs. This synchronous clear allows the count length to be modified easily, as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to all low outputs. Low to high transitions at the clear input of the ALS162B and ALS163B are also permissible regardless of the levels of logic on the clock, enable or load inputs.

The carry look ahead circuitry provides for cascading counters for n bit synchronous application without additional gating. Instrumental in accomplishing this function are two count enable inputs (P and T) and a ripple carry output. Both count enable inputs must be high to count. The T input is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high level output pulse with a duration approximately equal to the high level portion of QA output. This high level overflow ripple carry pulse can be used to enable successive cascaded stages. High to low level transitions at the enable P or T inputs of the ALS160B through ALS163B may occur regardless of the logic level on the clock.

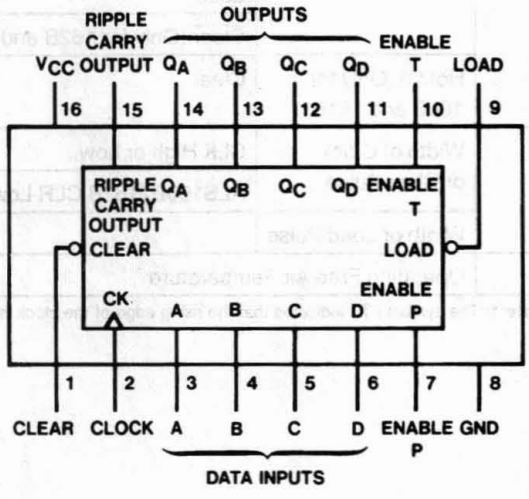
The ALS160B through ALS163B feature a fully independent clock circuit. changes made to control inputs (enable P or T, or load) that will modify the operating mode will have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading or counting) will be dictated solely by the conditions meeting the stable set-up and hold times.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin-for-pin compatible with Schottky and low power Schottky TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts
- Synchronously programmable
- Internal look ahead for fast counting
- Carry output for n-bit cascading
- Synchronous counting
- Load control line
- ESD inputs

Connection Diagram

Dual-In-Line Package



TL/F/6206–1

Order Number DM54ALS160BJ, 161BJ, 162BJ, 163BJ, DM74ALS160BM, 161BM, 162BM, 163BM or DM74ALS160BN, 161BN, 162BN, 163BN
See NS Package Number J16A, M16A or N16A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter			DM54ALS 160B, 161B, 162B, 163B			DM74ALS 160B, 161B, 162B, 163B			Units
				Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage			2			2			V
V_{IL}	Low Level Input Voltage					0.7			0.8	V
I_{OH}	High Level Output Current					−0.4			−0.4	mA
I_{OL}	Low Level Output Current					4			8	mA
f_{CLK}	Clock Frequency			0		22	0		40	MHz
t_{SETUP}	Setup Time	Data; A, B, C, D		20 ↑			15 ↑			ns
		En P, En T	ALS160B/161B	25 ↑			15 ↑			ns
			ALS162B/163B	20 ↑			15 ↑			ns
		Load		20 ↑			15 ↑			ns
		$\overline{\text{Clear}}$ (Only for 162B and 163B)	Low	20 ↑			15 ↑			ns
			High	10 ↑			10 ↑			ns
	Setup 1 (Only for 160B and 161B)	$\overline{\text{Clear}}$ Inactive		10	4		10	4		ns
t_{HOLD}	Hold Time	Data; A, B, C, D		0 ↑	−3		0 ↑	−3		ns
		En P, En T		0 ↑	−3		0 ↑	−3		ns
		Load		0 ↑	−4		0 ↑	−4		ns
		$\overline{\text{Clear}}$ (Only for 162B and 163B		0 ↑	−7		0 ↑	−7		ns
	Hold 0 (Only for 160B and 161B)	Clear		0	−4		0	−4		ns
t_W	Width of Clock or Clear Pulse	CLK High or Low		20			12.5			ns
		ALS160B/161B CLR Low		20			15			ns
	Width of Load Pulse			20			15			ns
T_A	Operating Free Air Temperature			−55		125	0		70	°C

Note 1: The symbol (↑) indicates that the rising edge of the clock is used as a reference.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V			12	21	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From	To	DM54ALS 160B, 161B		DM74ALS 160B, 161B		Units
					Min	Max	Min	Max	
f_{MAX}	Max. Clock Freq.	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF			22		40		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output		Clock	Ripple Carry	5	34	5	20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Clock	Ripple Carry	5	27	5	20	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		Clock	Any Q	4	19	4	15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Clock	Any Q	6	25	6	20	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		En T	Ripple Carry	3	18	3	13	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		En T	Ripple Carry	3	17	3	13	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Clear	Any Q	8	27	8	24	ns
			Clear	Ripple Carry	11	32	11	23	ns

Note 1: See Section 1 for test waveforms and output load.

'ALS162B, 'ALS163B Switching Characteristics

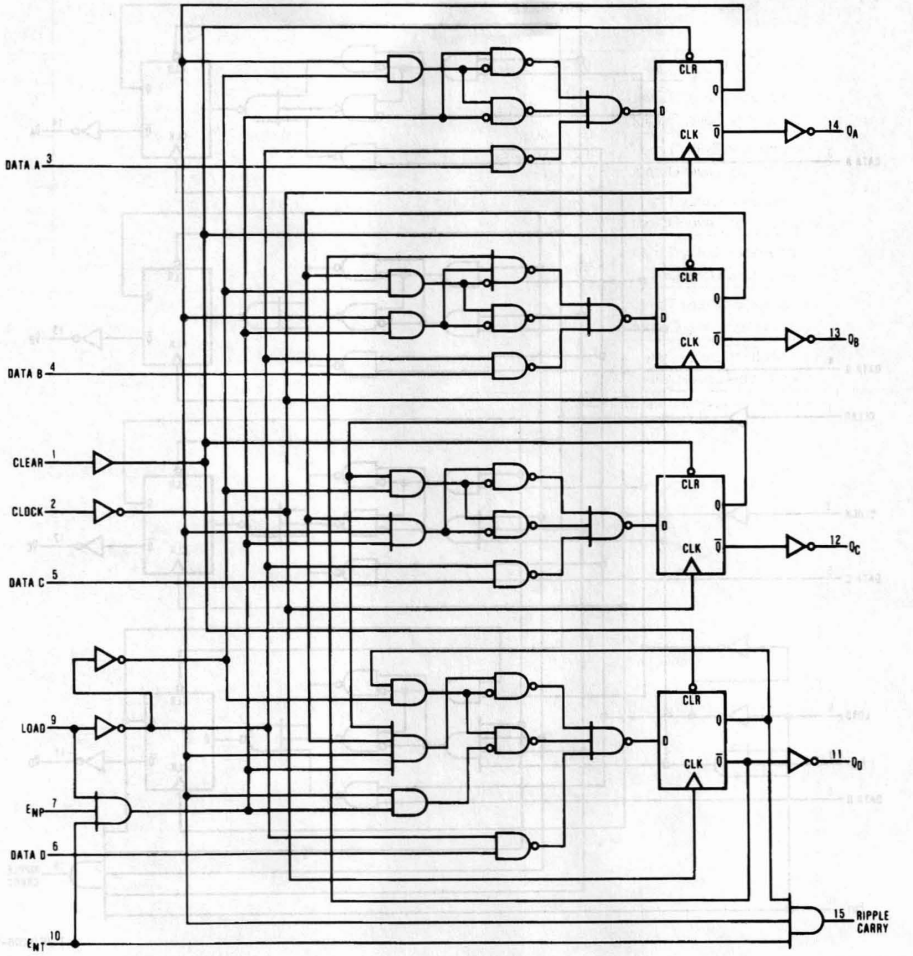
over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From	To	DM54ALS 162B, 163B		DM74ALS 162B, 163B		Units
					Min	Max	Min	Max	
f_{MAX}	Max. Clock Freq.	V_{CC} = 4.5V to 5.5V, R_L = 500Ω, C_L = 50 pF, T_A = Min to Max			35		40		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output		Clock	Ripple Carry	5	25	5	20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Clock	Ripple Carry	5	25	5	20	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		Clock	Any Q	4	18	4	15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Clock	Any Q	6	25	6	20	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		En T	Ripple Carry	3	16	3	13	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		En T	Ripple Carry	3	16	3	13	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagrams

ALS160B



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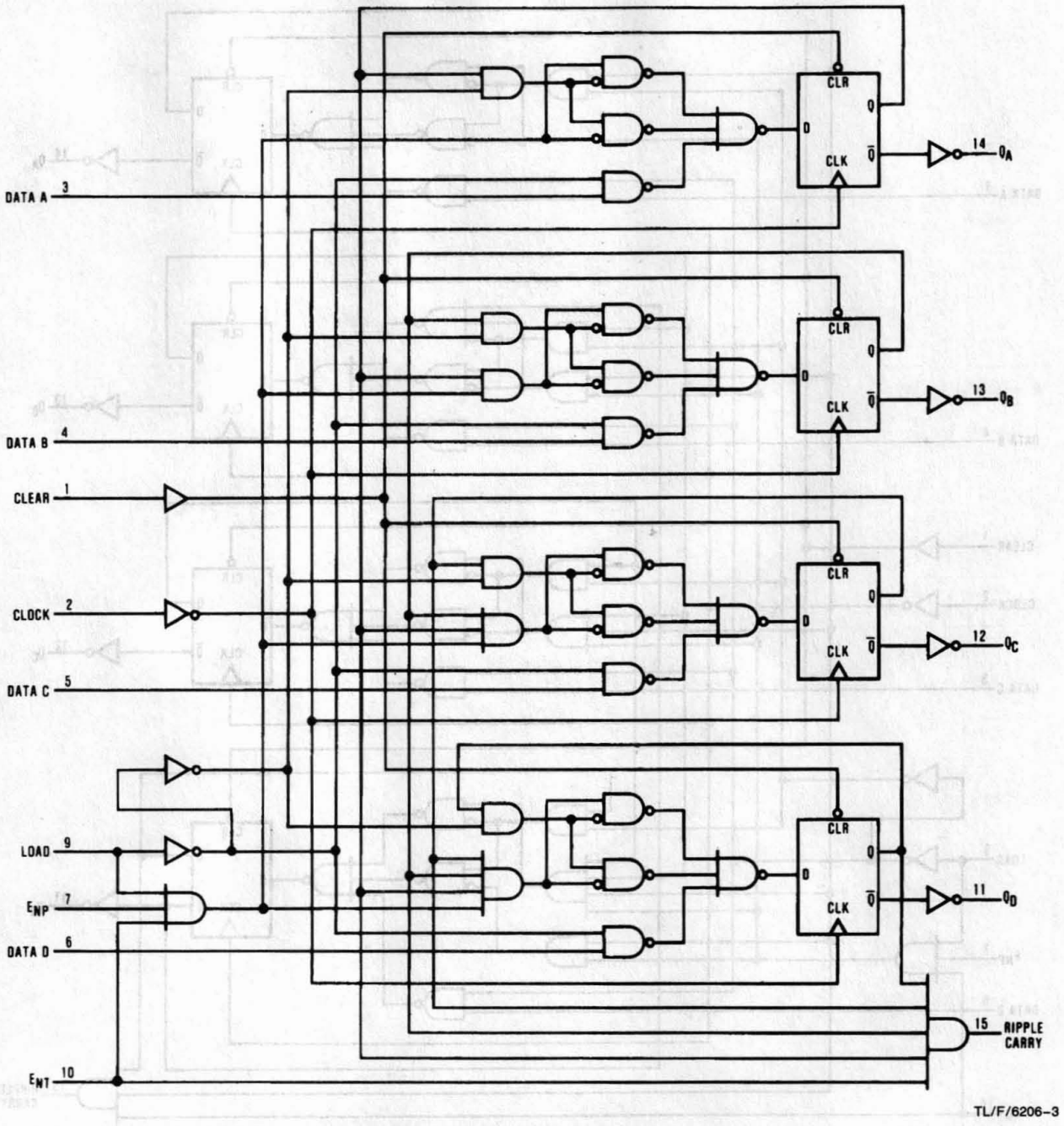
Logic Diagrams (Continued)

ALS161B



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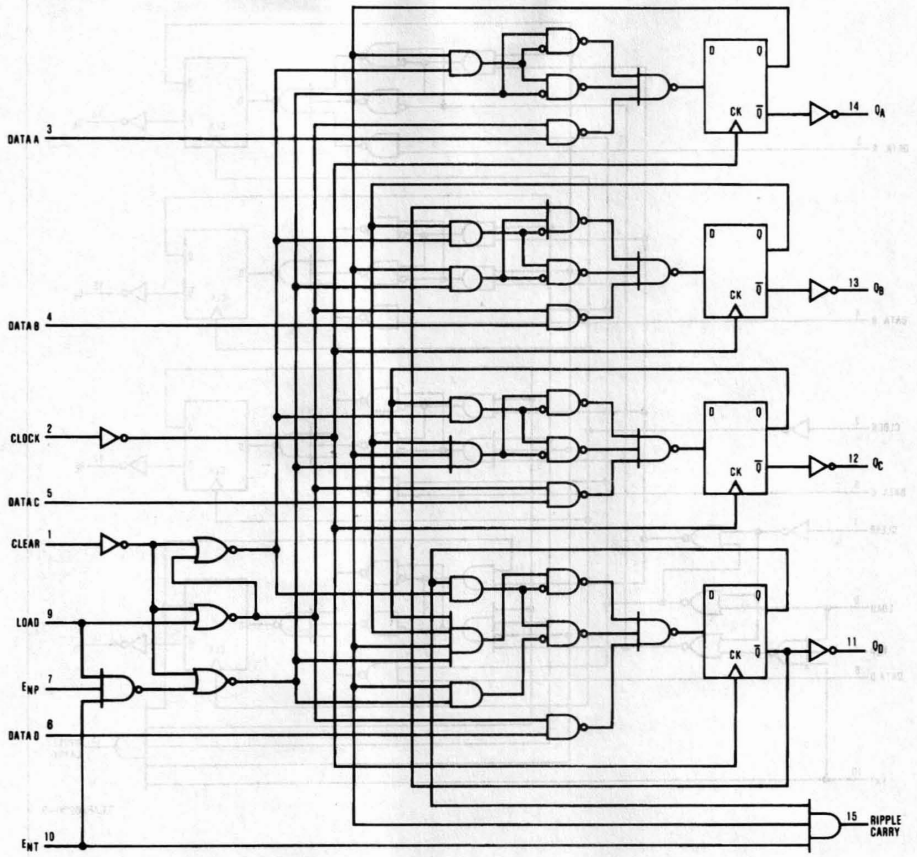
Logic Diagrams (Continued)

ALS162B



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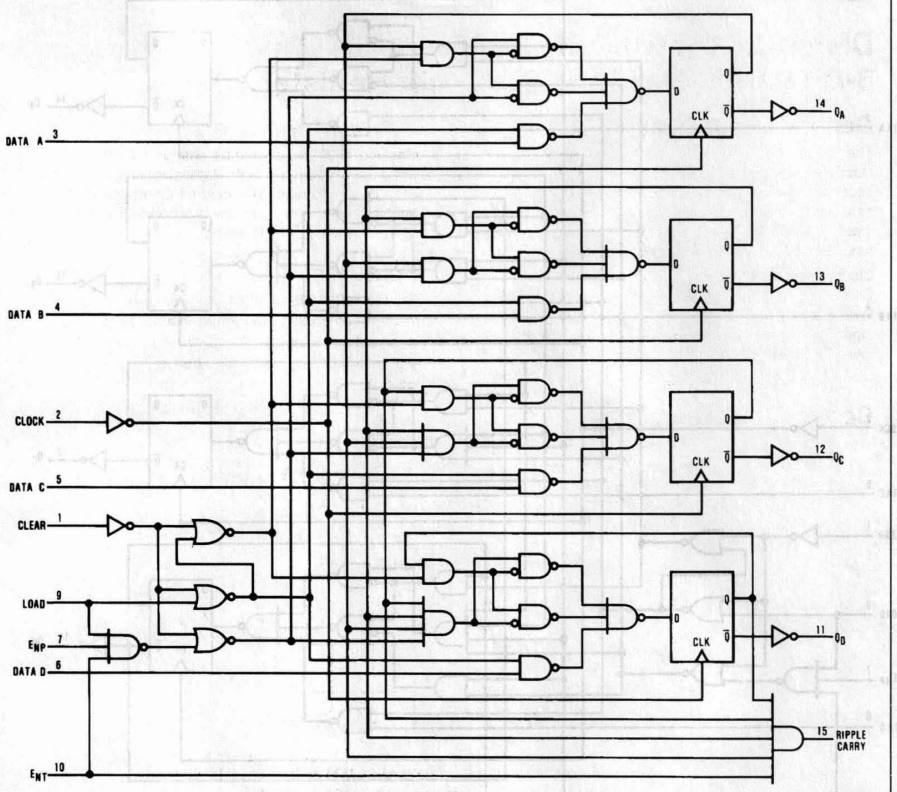
Logic Diagrams (Continued)

ALS163B



TL/F/6206–5

National Semiconductor Corporation

PRELIMINARY

DM54ALS165/DM74ALS165
8-Bit Parallel In/Serial Out Shift Register

General Description

The DM54/74ALS165 is an 8-bit serial register that, when clocked, shifts the data toward serial output, $\overline{Q}_H$. Parallel-in access to each stage is provided by eight individual direct data inputs that are enabled by a low level at the SH/$\overline{LD}$ input. The DM54/74ALS165 also features a clock inhibit function and a complemented serial output, $\overline{Q}_H$.

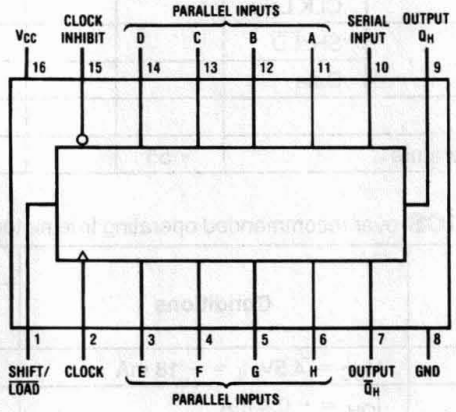
Clocking is accomplished by a low-to-high transition of the CLK input while SH/$\overline{LD}$ is held high and CLK INH is held low. The functions of the CLK and CLK INH (clock inhibit) inputs are interchangeable. Since a low CLK input and a low-to-high transition of CLK INH will also accomplish clocking, CLK INH should be changed to the high level only while the CLK input is high. Parallel loading is inhibited when SH/$\overline{LD}$ is held high. The parallel inputs to the register are enabled while SH/$\overline{LD}$ is low independently of the levels of CLK, CLK INH, or SER inputs.

Features

- Complementary outputs
- Direct overriding load (data) inputs
- Gated clock inputs
- Parallel-to-serial data conversion

Connection Diagram

Dual-In-Line Package



TL/F/6712–1

Order Number DM54ALS165J, DM74ALS165M or DM74ALS165N
See NS Package Number J16A, M16A or N16A

Function Table

Inputs					Internal Outputs		Output Q_H
Shift/ Load	Clock Inhibit	Clock	Serial	Parallel A...H	Q_A	Q_B	
L	X	X	X	a...h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	↑	L	H	X	H	Q_{An}	Q_{Gn}
H	↑	L	L	X	L	Q_{An}	Q_{Gn}
H	H	X	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = High Level (steady-state), L = Low Level (steady-state)

X = Don't Care (any input, including transitions)

↑ = Transition from low-to-high level

a...h = The level of steady-state input at inputs A through H, respectively

Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established

Q_{An}, Q_{Gn} = The level of Q_A or Q_G, respectively, before the most recent ↑ transition of the clock

This document contains information on a product under development. NSC reserves the right to change or discontinue this product without notice.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54ALS165			DM74ALS165			Units
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLOCK}	Clock Frequency								MHz
t_W	Pulse Duration	CLK High							ns
		CLK Low							
t_{SU}	Setup Time	SH/$\overline{LD}$							ns
		Data							
t_H	Hold Time								ns
T_A	Operating Free Air Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		DM54ALS165			Units
				Min	Typ (Note 1)	Max	
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA, V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_I = 0.4V				−0.1	mA
I_O (Note 2)	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V (Note 3)			16		mA

Switching Characteristics

over recommended free air temperature range (Note 4). All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Input	Output	Conditions	DM54ALS165			DM74ALS165			Units
					Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Frequency			V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R_L = 50Ω	25			25			MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Load	Q_H or $\overline{Q}_H$			21			21		ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Load	Q_H or $\overline{Q}_H$			26			26		
t_{PLH}	Propagation Delay Time Low to High Level Output	CLK	Q_H or $\overline{Q}_H$			14			14		ns
t_{PHL}	Propagation Delay Time High to Low Level Output	CLK	Q_H or $\overline{Q}_H$			16			16		
t_{PLH}	Propagation Delay Time Low to High Level Output	H	Q_H			13			13		ns
t_{PHL}	Propagation Delay Time High to Low Level Output	H	Q_H			24			24		
t_{PLH}	Propagation Delay Time Low to High Level Output	H	$\overline{Q}_H$			19			19		ns
t_{PHL}	Propagation Delay Time High to Low Level Output	H	$\overline{Q}_H$			17			17		

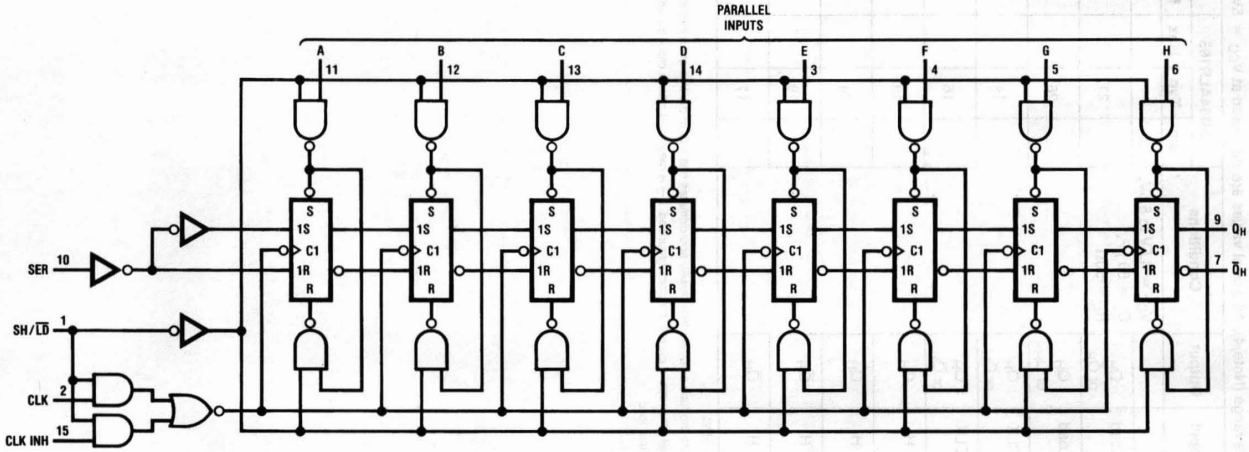
Note 1: All typical values are at V_{CC} = 5V, T_A = 25°C.

Note 2: The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

Note 3: With 4.5V applied to the serial input and all other inputs except the clock grounded, I_{CC} is measured after a clock transition from 0V to 4.5V.

Note 4: See Section 1 for test waveforms and output load.

Logic Diagram



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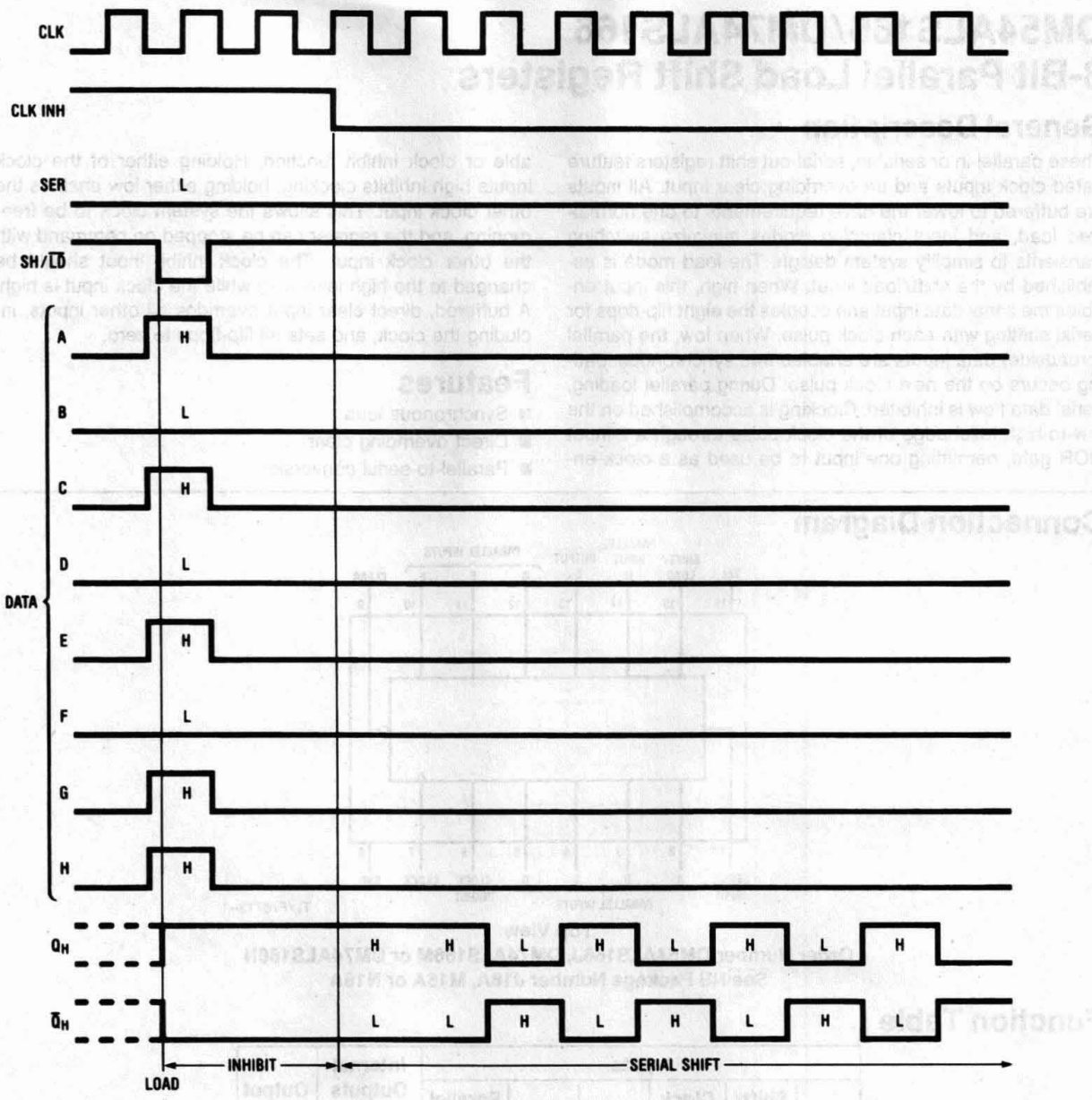
Timing Diagram

Typical Shift, Load, and Inhibit Sequences



TL/F/6712–3

National Semiconductor Corporation

PRELIMINARY

DM54ALS166/DM74ALS166 8-Bit Parallel Load Shift Registers

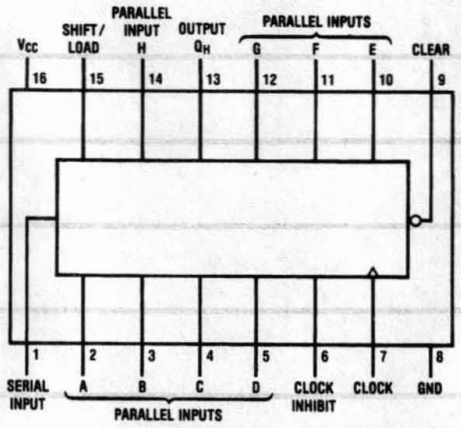
General Description

These parallel-in or serial-in, serial-out shift registers feature gated clock inputs and an overriding clear input. All inputs are buffered to lower the drive requirements to one normalized load, and input clamping diodes minimize switching transients to simplify system design. The load mode is established by the shift/load input. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel (broadside) data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high level edge of the clock pulse through a 2-input NOR gate, permitting one input to be used as a clock enable or clock inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This allows the system clock to be free-running, and the register can be stopped on command with the other clock input. The clock inhibit input should be changed to the high level only while the clock input is high. A buffered, direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero.

Features

- Synchronous load
- Direct overriding clear
- Parallel-to-serial conversion

Connection Diagram



TL/F/6713–1

Top View
Order Number DM54ALS166J, DM74ALS166M or DM74ALS166N
See NS Package Number J16A, M16A or N16A

Function Table

Inputs						Internal Outputs		Output Q_H
Clear	Shift/ Load	Clock Inhibit	Clock	Serial	Parallel A...H	Q_A	Q_B	
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	↑	X	a...h	a	b	h
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	X	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = high level (steady-state), L = low level (steady-state).

X = don't care (any input, including transitions).

↑ = transition from low-to-high level.

a...h = the level of steady-state input at inputs A through H, respectively.

Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Gn} = the level of Q_A or Q_G, respectively, before the most recent ↑ transition of the clock.

This document contains information on a product under development. NSC reserves the right to change or discontinue this product without notice.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Free Air Operating Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54ALS166			DM74ALS166			Units
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency								MHz
t_W	Pulse Duration	$\overline{CLR}$							ns
		CLK High							
		CLK Low							
t_{SU}	Setup Time before CLK ↑	SH/$\overline{LD}$							ns
		Data							
		$\overline{CLR}$ Inactive							
t_H	Hold Time, Data after CLK ↑								
T_A	Operating Free-Air Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free-air temperature range unless otherwise noted

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V, I_{OH} = −0.4 mA		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
		V_{CC} = 4.5V	74ALS I_{OL} = 8 mA		0.35	0.5	
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V			−0.1		mA
I_O (Note 2)	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V (Note 3)			16		mA

Switching Characteristics

over recommended free air temperature range (Note 4). All typicals are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions	Input	Output	DM54ALS166			DM74ALS166			Units
					Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
f_{MAX}	Maximum Clock Frequency	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R_L = 500Ω, T_A = Min to Max				60			60		MHz
t_{PHL}	Propagation Delay Time High to Low Level Output		$\overline{CLR}$	Q_H		10			10		ns
t_{PLH}	Propagation Delay Time Low to High Level Output		CLK	Q_H		12			12		ns
t_{PHL}	Propagation Delay Time High to Low Level Output		CLK	Q_H		13			13		ns

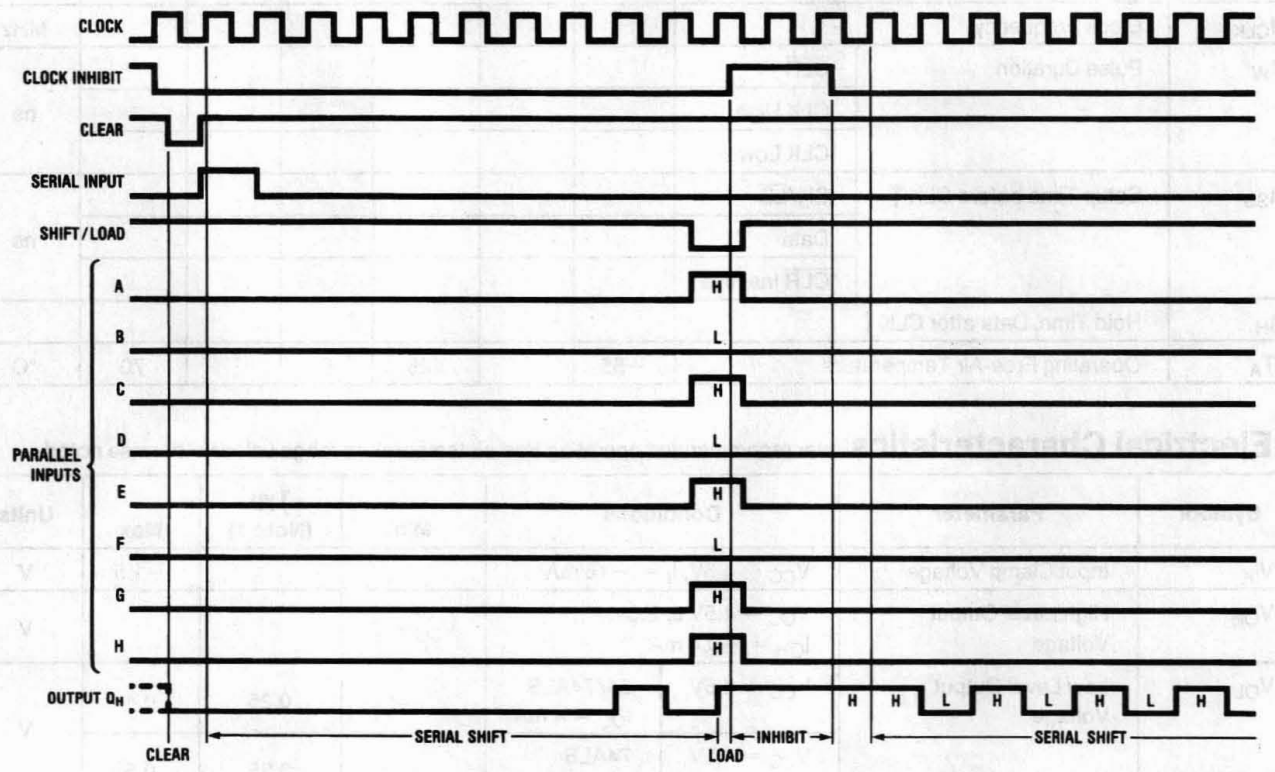
Note 1: All typical values are at V_{CC} = 5V, T_A = 25°C.

Note 2: The output conditions have been chosen to produce a current that closely approximates one half of the true short circuit output current, I_{OS}.

Note 3: With 4.5V applied to the serial input and all other inputs except the clock grounded, I_{CC} is measured after a clock transition from 0V to 4.5V.

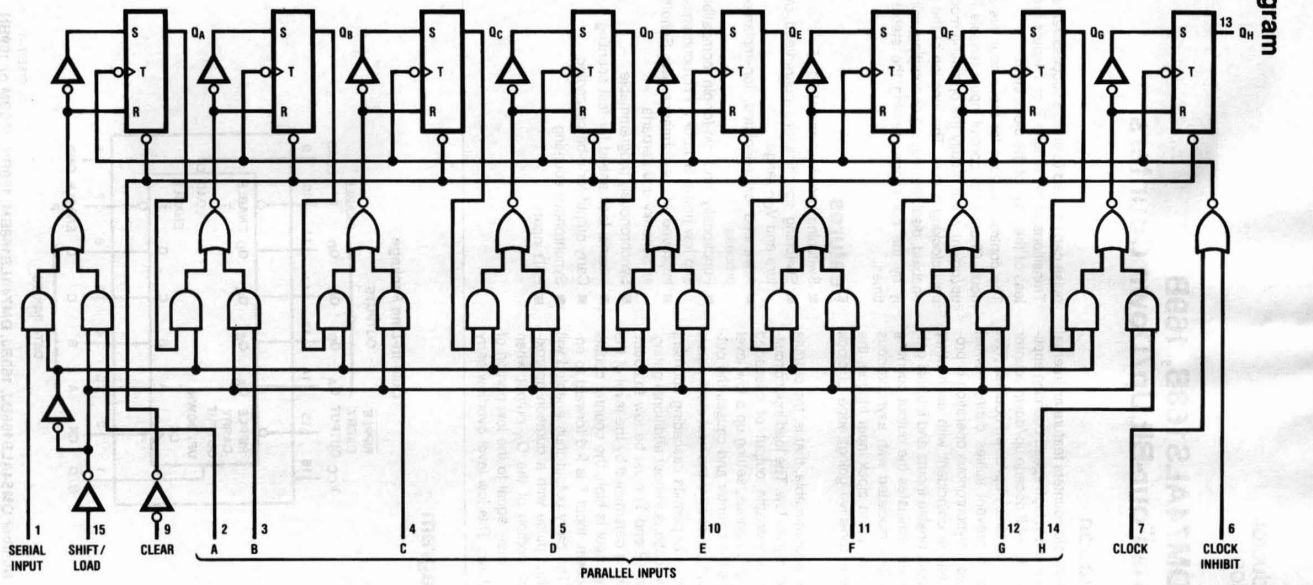
Note 4: See Section 1 for test waveforms and output load.

Timing Diagram



TL/F/6713–3

Logic Diagram



TL/F/6713–2

National Semiconductor Corporation

DM54ALS/DM74ALS168B, 169B Synchronous Four-Bit Up/Down Counters

General Description

These synchronous presettable counters feature an internal carry look ahead for cascading in high speed counting applications. The ALS168B is a four-bit decade up/down counter and the ALS169B is a four-bit binary up/down counter. The carry output is decoded to prevent spikes during normal mode of counting operation. Synchronous operation is provided so that outputs change coincident with each other when so instructed by count enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive going) edge of clock input waveform.

These counters are fully programmable; that is, the outputs may each be preset either high or low. The load input circuitry allows loading with carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry permits cascading counters for n-bit synchronous applications without additional gating. Both count enable inputs ($\overline{P}$ and $\overline{T}$) must be low to count. The direction of the count is determined by the level of the up/down input. When the input is high, the counter counts up; when low, it counts down. Input T is fed forward to enable the carry outputs. The carry output thus enabled will produce a low level output pulse with a duration approximately equal to the high portion of the Q_A output when counting up, and approximately equal to the low portion of the Q_A when counting down. This low level overflow carry pulse can be used to enable successively cascaded stages. Transitions at the enable $\overline{P}$ or $\overline{T}$ inputs are allowed regardless of the level of the clock input.

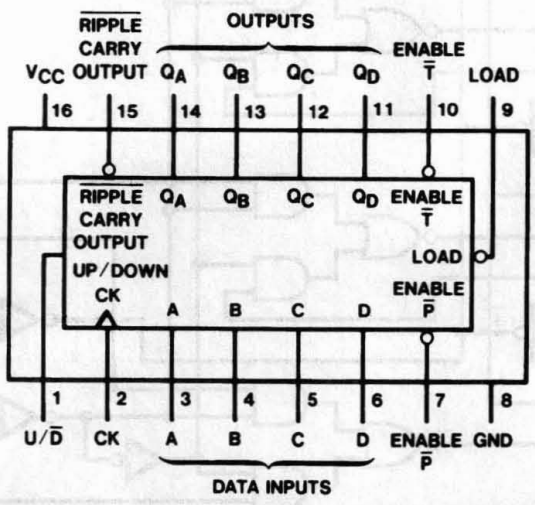
The control functions for these counters are fully synchronous. Changes at control inputs (enable $\overline{P}$, enable $\overline{T}$, load, up/down) which modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin-for-pin compatible with Schottky and low power Schottky TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts
- Synchronously programmable
- Internal look ahead for fast counting
- Carry output for n-bit cascading
- Synchronous counting
- ESD inputs

Connection Diagram

Dual-In-Line Package



TL/F/6207–1

Order Number DM54ALS168BJ, 169BJ, DM74ALS168BM, 168BN, 169BM or 169BN
See NS Package Number J16A, M16A or N16A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54ALS168B, 169B			DM74ALS168B, 169B			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency		0		22	0		40	MHz
t_{SU}	Setup Time	Data; A, B, C, D	20 ↑	6		15 ↑	6		ns
		En $\overline{P}$, En $\overline{T}$	25 ↑	8		15 ↑	8		ns
		$\overline{Load}$	20 ↑	8		15 ↑	8		ns
		U/$\overline{D}$	28 ↑	10		15 ↑	10		ns
t_H	Hold Time	Data; A, B, C, D	0 ↑	−3		0 ↑	−3		ns
		En $\overline{P}$, En $\overline{T}$	0 ↑	−3		0 ↑	−3		ns
		$\overline{Load}$	0 ↑	−4		0 ↑	−4		ns
		U/$\overline{D}$	0 ↑	−4		0 ↑	−4		ns
t_W	Width of Clock Pulse		15			13			ns

Note 1: The symbol (↑) indicates that the rising edge of the clock is used as reference.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V			15	25	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

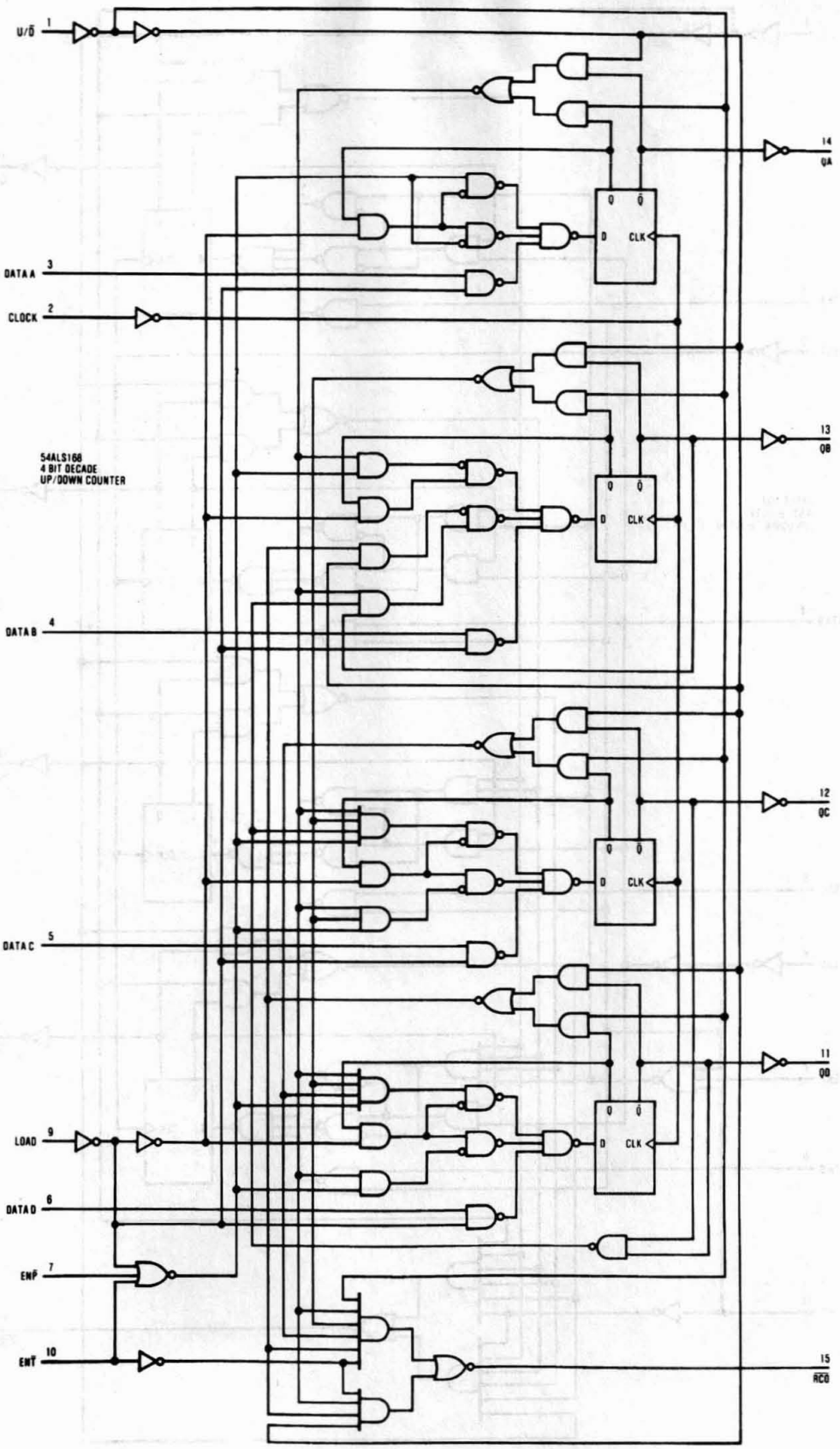
Symbol	Parameter	Conditions	From	To	DM54ALS168B, 169B		DM74ALS168B, 169B		Units
					Min	Max	Min	Max	
f_{MAX}	Max. Clock Freq.				22		40		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V, R_L = 500Ω, C_L = 50 pF	Clock	$\overline{\text{Ripple Carry}}$	3	25	3	20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Clock	$\overline{\text{Ripple Carry}}$	6	25	6	20	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		Clock	Any Q	2	20	2	15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Clock	Any Q	5	23	5	20	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		En T	$\overline{\text{Ripple Carry}}$	2	16	2	13	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		En T	$\overline{\text{Ripple Carry}}$	3	24	3	16	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		U/$\overline{\text{D}}$ (Note 2)	$\overline{\text{Ripple Carry}}$	5	22	5	19	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		U/$\overline{\text{D}}$ (Note 2)	$\overline{\text{Ripple Carry}}$	5	22	5	19	ns

Note 1: See Section 1 for test waveforms and output load.

Note 2: Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0), the ripple carry output transition will be in phase. If the count is maximum (9 for ALS168B or 15 for ALS169B), the ripple carry output will be out of phase.

Logic Diagrams

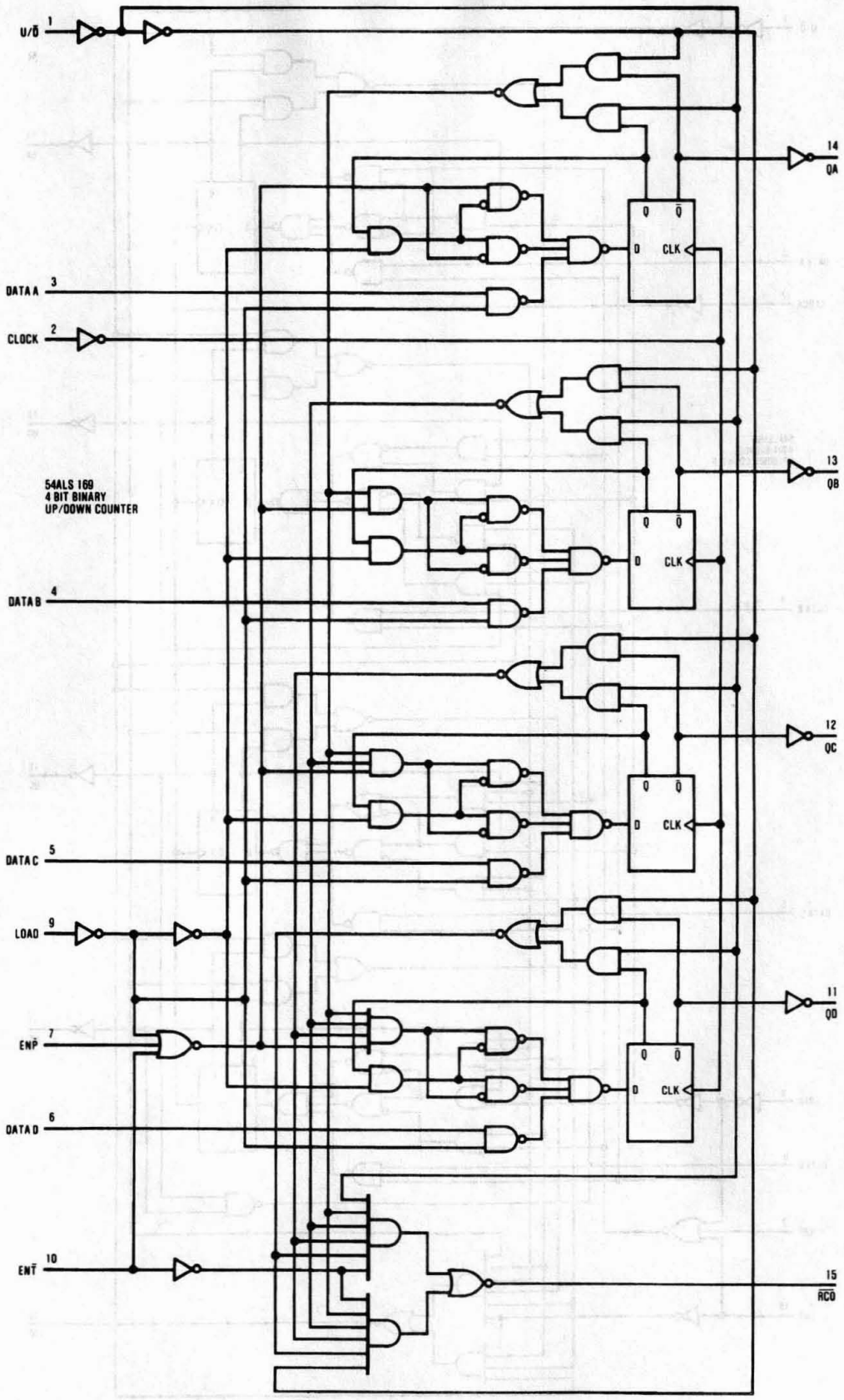
DM54ALS/DM74ALS168B



TL/F/6207–2

Logic Diagrams (Continued)

DM54ALS/DM74ALS169B



TL/F/6207–3

National Semiconductor Corporation

DM54ALS174/DM54ALS175/DM74ALS174/DM74ALS175 Hex/Quad D Flip-Flops with Clear

General Description

These positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. Both have an asynchronous clear input, and the quad (175) version features complementary outputs from each flip-flop.

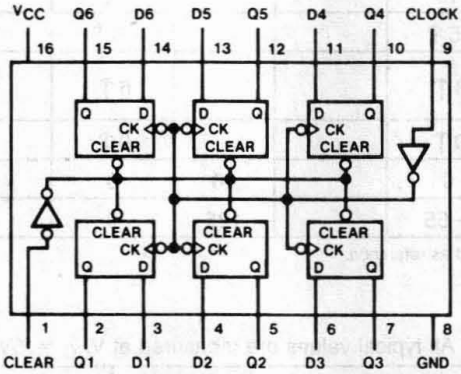
Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

Features

- Advanced oxide-isolated ion-implanted Schottky TTL process
- Pin and functional compatible with LS family counterpart
- Typical clock frequency maximum is 80 MHz
- Switching performance guaranteed over full temperature and V_{CC} supply range
- 54ALS174 contains six flip-flops with separate D inputs and Q outputs
- 54ALS175 contains four flip-flops with separate D inputs and both Q and $\overline{Q}$ outputs

Connection Diagrams

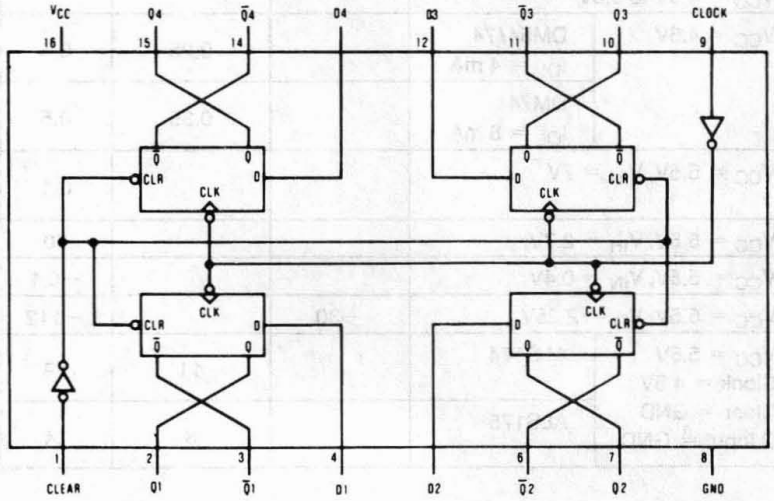
Dual-In-Line Package



TL/F/6112–1

Order Number DM54ALS174J or DM74ALS174M, N
See NS Package Number J16A, M16A or N16A

Dual-In-Line Package



TL/F/6112–2

Function Table

Inputs			Outputs	
Clear	Clock	D	Q	$\overline{Q}$*
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

H = High Level (steady state)
L = Low Level (steady state)
X = Don't Care
↑ = Transition from Low to High Level
Q_0 = the level of Q before the indicated steady-state input conditions were established
*applies to 54ALS175/74ALS175 only

Order Number DM54ALS175J
or DM74ALS175M, N
See NS Package Number J16A,
M16A or N16A

2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54ALS174,175			DM74ALS174,175			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
t_W	Pulse Width	Clock High or Low	12.5			10			ns
		$\overline{\text{Clear}}$ Low	15			10			
t_{SETUP}	Setup Time (Note 1)	Data Input	15 ↑			10 ↑			ns
		$\overline{\text{Clear}}$ Inactive State	8 ↑			6 ↑			
t_{HOLD}	Data Hold Time (Note 1)		0 ↑			0 ↑			ns
f_{CLOCK}	Clock Frequency		0		40	0		50	MHz
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol ↑ indicates that the rising edge of the clock is used as reference.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −400 μA V_{CC} = 4.5V to 5.5V		V_{CC} − 2	V_{CC} − 1.6		V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	DM54/74 I_{OL} = 4 mA		0.25	0.4	V
			DM74 I_{OL} = 8 mA		0.35	0.5	
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IN} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V Clock = 4.5V Clear = GND D Input = GND	ALS174		11	19	mA
			ALS175		8	14	

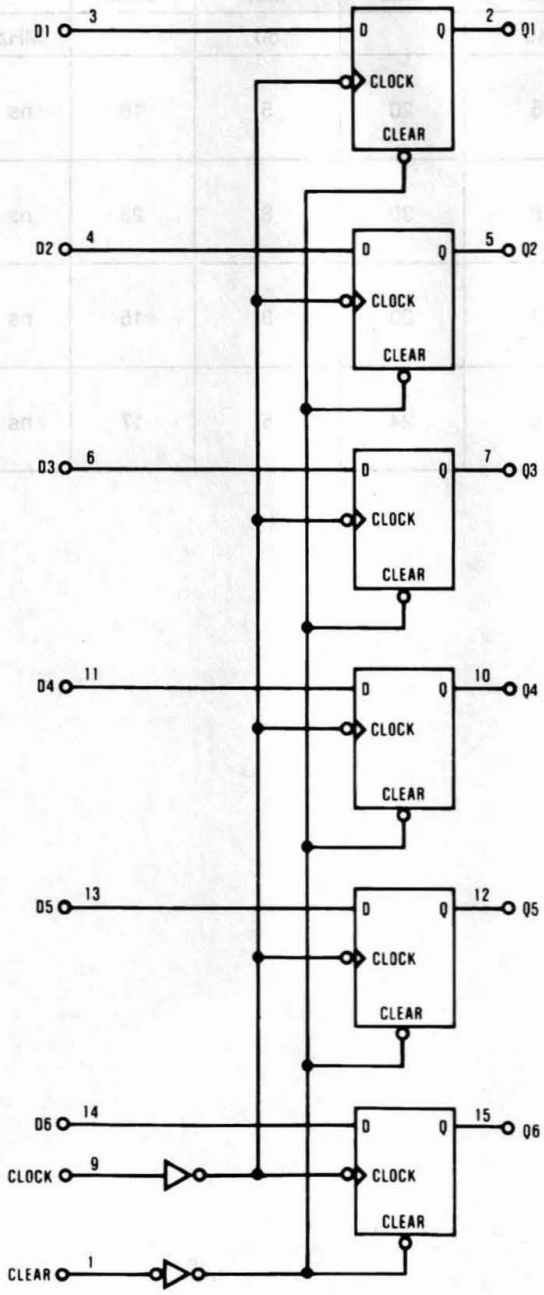
Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	DM54ALS174,175		DM74ALS174,175		Units
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	$R_L = 500\Omega$ $C_L = 50$ pF $V_{CC} = 4.5V$ to $5.5V$	40		50		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output From Clear (175 Only)		5	20	5	18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output From Clear		8	30	8	23	ns
t_{PLH}	Propagation Delay Time Low to High Level Output From Clock		3	20	3	15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output From Clock		5	24	5	17	ns

Note 1: See Section 1 for test waveforms and output load.

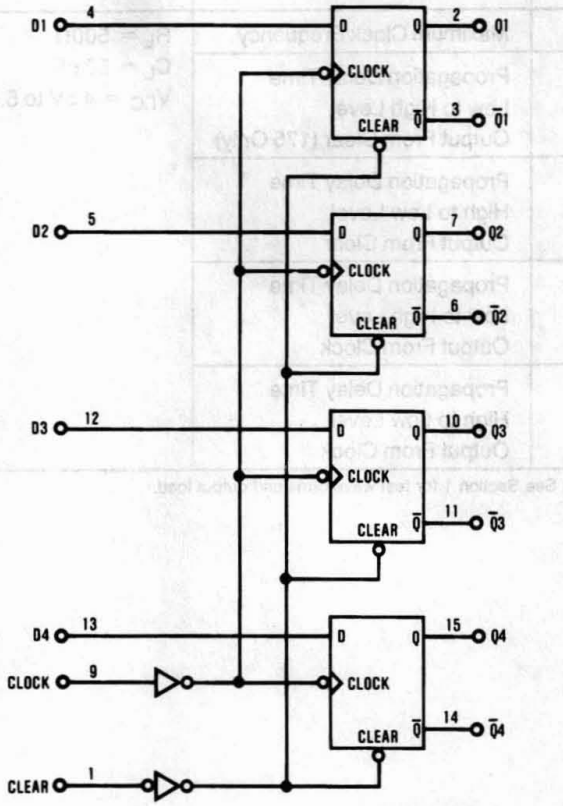
Logic Diagrams

54ALS174/74ALS174



TL/F/6112–3

54ALS175/74ALS175



TL/F/6112–4

National Semiconductor Corporation

PRELIMINARY

DM54ALS190/DM74ALS190/DM54ALS191/DM74ALS191 Synchronous 4-Bit Up/Down Decade and Binary Counter

General Description

The 'ALS190 and 'ALS191 are synchronous, reversible up/down counters. The 'ALS190 is a 4-bit decade counter and the 'ALS191 is a 4-bit binary counter. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered on a low-to-high level transition of the clock input if the enable input (G) is low. A high at G inhibits counting. The direction of the count is determined by the level of the down/up (D/$\overline{U}$) input. When D/$\overline{U}$ is low, the counter counts up and when D/$\overline{U}$ is high, it counts down.

These counters feature a fully independent clock circuit. Changes at the control inputs (G and D/$\overline{U}$) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter will be dictated solely by the condition meeting the stable set-up and hold times.

These counters are fully programmable; that is, the outputs may each be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

The CLK, D/$\overline{U}$, and LOAD inputs are buffered to lower the drive requirement, which significantly reduces the loading on, or current required by, clock drivers, etc., for long parallel words.

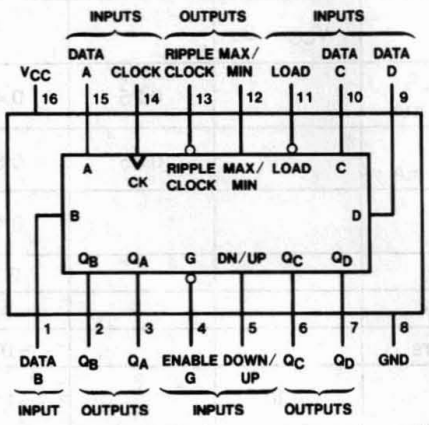
Two outputs have been made available to perform the cascading function; ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is zero (all outputs low) counting down or maximum (9 or 15) counting up. The ripple clock output produces a low-level output pulse under those same conditions but only while the clock input is low. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin-for-pin compatible with Schottky and low power Schottky TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts
- Single down/up count control line
- Look-ahead circuitry enhances speed of cascaded counters
- Fully synchronous in count modes
- Asynchronously presettable with load control

Connection Diagram

Dual-In-Line Package



TL/F/6208–1

Order Number DM54ALS190J, DM54ALS191J, DM74ALS190M, DM74ALS191M, DM74ALS190N or DM74ALS191N
See NS Package Number J16A, M16A or N16A

This document contains information on a device under development. National Semiconductor Corporation reserves the right to change or discontinue this product without notice.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter			DM54ALS190, 191			DM74ALS190, 191			Units
				Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage			2			2			V
V_{IL}	Low Level Input Voltage					0.7			0.8	V
I_{OH}	High Level Output Current					−0.4			−0.4	mA
I_{OL}	Low Level Output Current					4			8	mA
f_{CLOCK}	Clock Frequency	'ALS190		0		20	0		25	MHz
		'ALS191		0		25	0		30	MHz
t_W	Pulse Duration	CLK High or Low	'ALS190	25			20			ns
			'ALS191	20			16.5			ns
		$\overline{LOAD}$ Low		25			20			ns
t_{SU}	Setup Time	Data before $\overline{LOAD}$ ↑		25			20			ns
		G before CLK ↑		45			20			ns
		D/$\overline{U}$ before CLK ↑		45			20			ns
		$\overline{LOAD}$ Inactive before CLK ↑		20			20			ns
t_H	Hold Time	Data after $\overline{LOAD}$ ↑		5			5			ns
		G after CLK ↑		0			0			ns
		D/$\overline{U}$ after CLK ↑		0			0			ns
T_A	Operating Free Air Temperature			−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		DM74ALS190, 191			Units
				Min	Typ (Note 1)	Max	
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V, I_{OH} = −0.4 mA		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
		V_{CC} = 4.5V	74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_I = 0.4V	G or CLK			−0.2	mA
			All Others			−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V (Note 2)		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V, All Inputs at 0V			12	22	mA

Note 1: All typical values are at V_{CC} = 5V, T_A = 25°C.

Note 2: The output conditions have been chosen to produce a current that closely approximates one half of the true short circuit output current, I_{OS}.

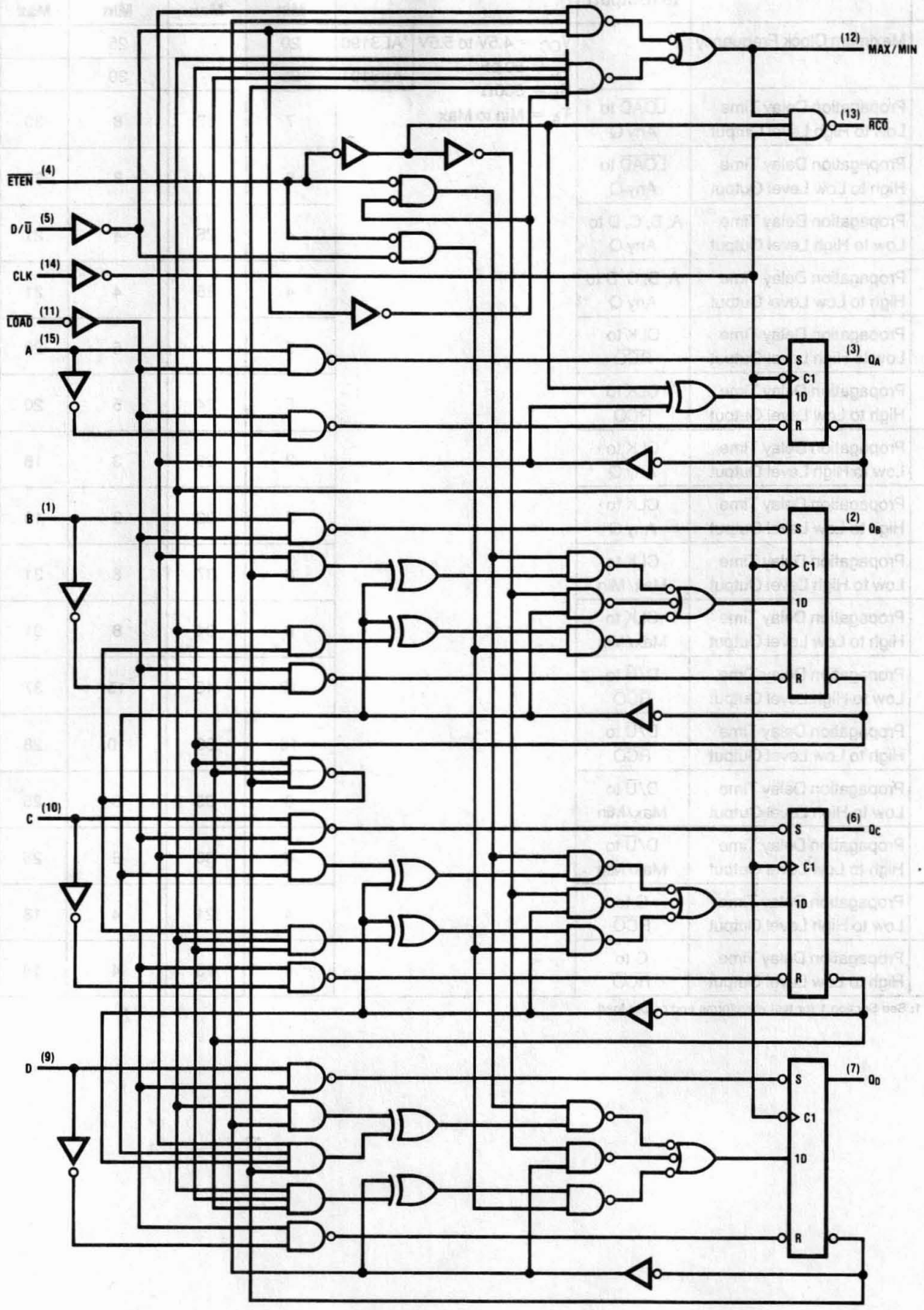
Switching Characteristics (Note 1)

Symbol	Parameter	From (Input) to (Output)	Conditions		DM54ALS190, 191		DM74ALS190, 191		Units
					Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R_L = 500Ω, T_A = Min to Max	'ALS190	20		25		MHz
				'ALS191	25		30		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	$\overline{LOAD}$ to Any Q			7	37	8	30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	$\overline{LOAD}$ to Any Q			8	34	8	30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A, B, C, D to Any Q			4	25	4	21	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A, B, C, D to Any Q			4	25	4	21	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	CLK to $\overline{RCO}$			5	24	5	20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	CLK to $\overline{RCO}$			5	24	5	20	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	CLK to Any Q			3	26	3	18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	CLK to Any Q			3	22	3	18	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	CLK to Max/Min			8	37	8	31	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	CLK to Max/Min			8	34	8	31	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	D/$\overline{U}$ to $\overline{RCO}$			12	45	15	37	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	D/$\overline{U}$ to $\overline{RCO}$			10	36	10	28	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	D/$\overline{U}$ to Max/Min			8	35	8	25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	D/$\overline{U}$ to Max/Min			8	30	8	25	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	G to $\overline{RCO}$			4	21	4	18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	G to $\overline{RCO}$			4	23	4	18	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagrams

ALS190

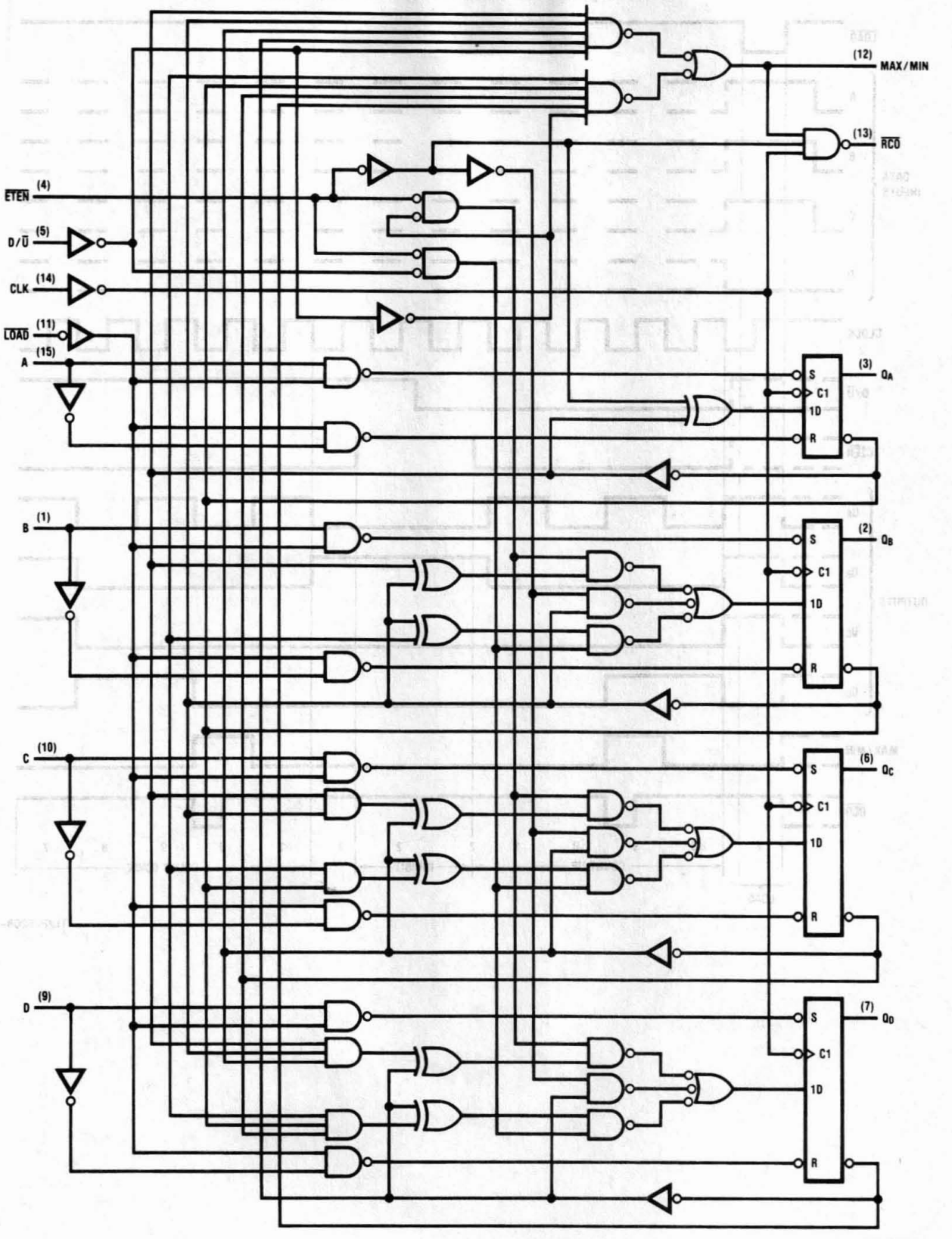


TL/F/6208–2

Pin numbers shown are for J and N packages.

Logic Diagrams (Continued)

ALS191

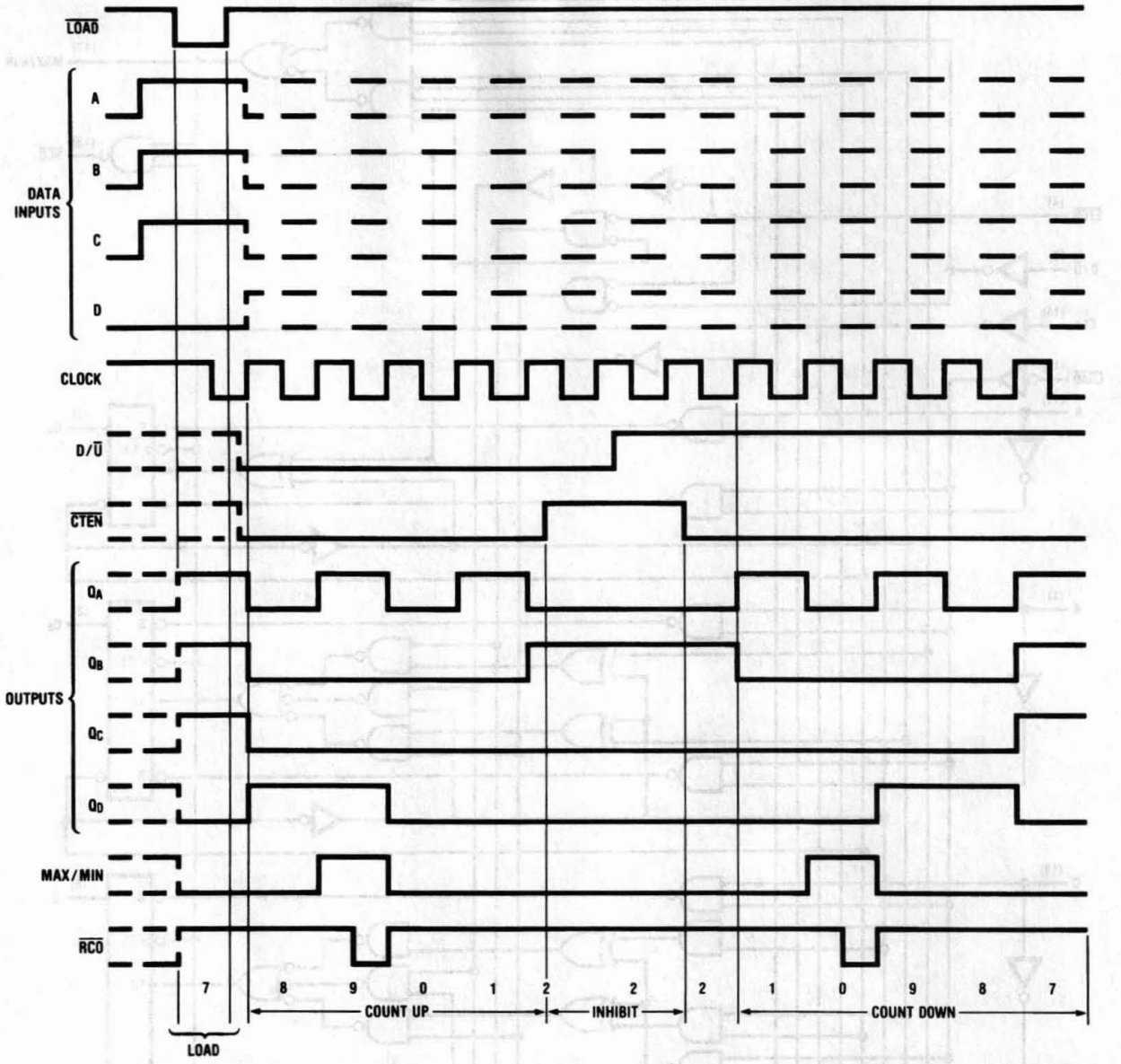


TL/F/6208–3

Pin numbers shown are for J and N packages.

Timing Diagrams

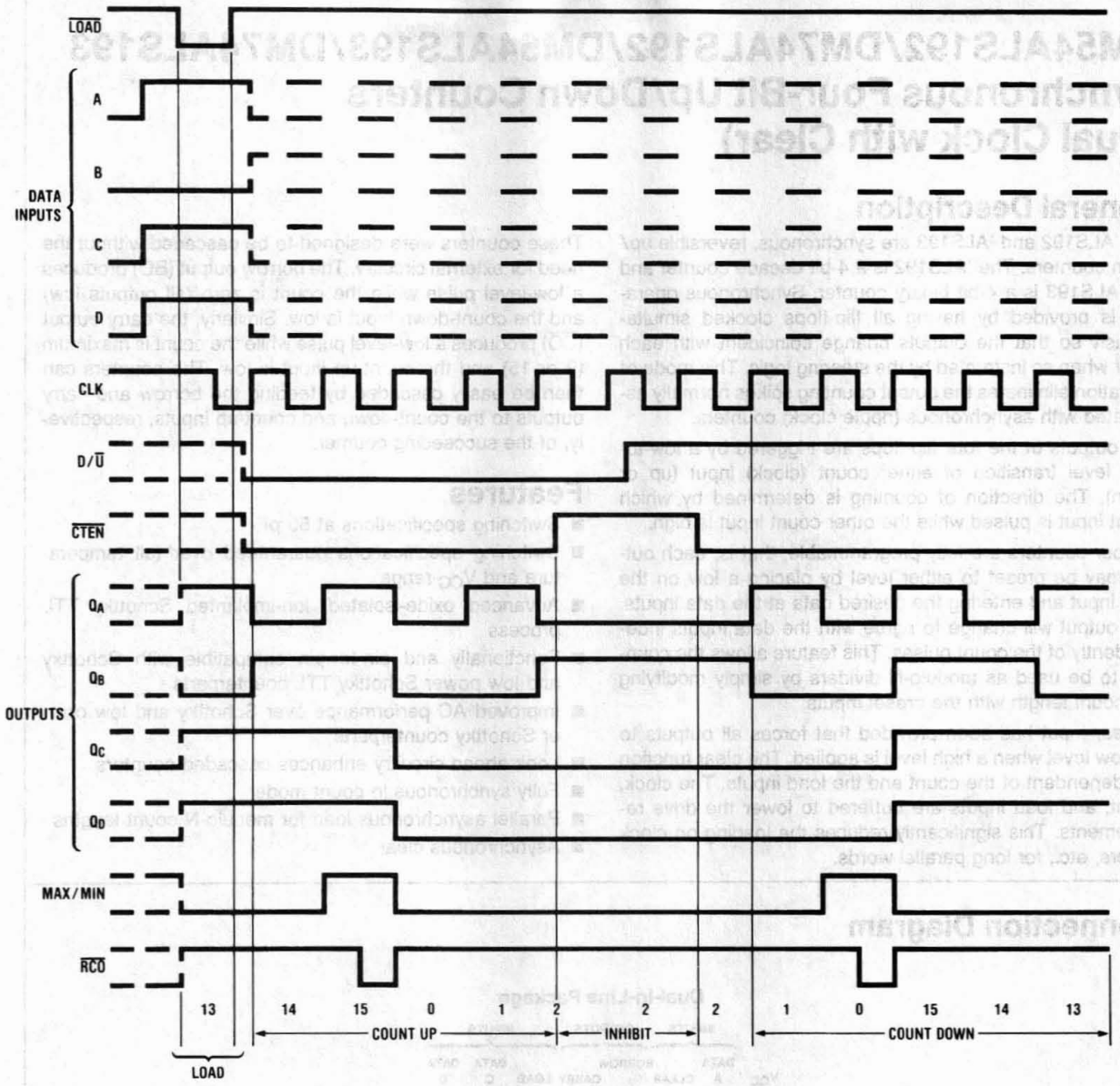
'ALS190 Typical Load, Count, and Inhibit Sequences



TL/F/6208–4

Timing Diagrams (Continued)

'ALS191 Typical Load, Count, and Inhibit Sequences



TL/F/6208–5

National Semiconductor Corporation

PRELIMINARY

DM54ALS192/DM74ALS192/DM54ALS193/DM74ALS193 Synchronous Four-Bit Up/Down Counters (Dual Clock with Clear)

General Description

The 'ALS192 and 'ALS193 are synchronous, reversible up/down counters. The 'ALS192 is a 4-bit decade counter and the 'ALS193 is a 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered by a low-to-high level transition of either count (clock) input (up or down). The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided that forces all outputs to the low level when a high level is applied. The clear function is independent of the count and the load inputs. The clock, count, and load inputs are buffered to lower the drive requirements. This significantly reduces the loading on clock drivers, etc., for long parallel words.

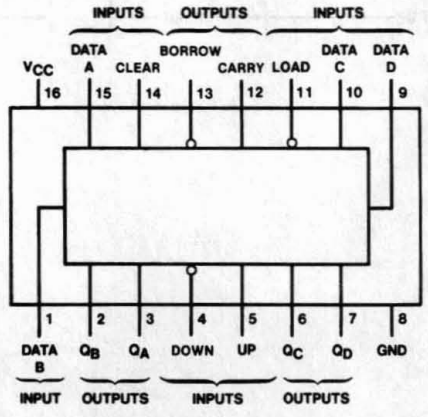
These counters were designed to be cascaded without the need for external circuitry. The borrow output (BO) produces a low-level pulse while the count is zero (all outputs low) and the count-down input is low. Similarly, the carry output ($\overline{CO}$) produces a low-level pulse while the count is maximum (9 or 15) and the count-up input is low. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs, respectively, of the succeeding counter.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin-for-pin compatible with Schottky and low power Schottky TTL counterparts
- Improved AC performance over Schottky and low power Schottky counterparts
- Look ahead circuitry enhances cascaded counters
- Fully synchronous in count mode
- Parallel asynchronous load for modulo-N count lengths
- Asynchronous clear

Connection Diagram

Dual-In-Line Package



TL/F/6209–1

Order Number DM54ALS192J, 193J, DM74ALS192M, 193M or DM74ALS192N, 193N
See NS Package Number J16A, M16A or N16A

This document contains information on a device under development. National Semiconductor Corporation reserves the right to change or discontinue this product without notice.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0 to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter			DM54ALS192, 193			DM74ALS192, 193			Units
				Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage			2			2			V
V_{IL}	Low Level Input Voltage					0.7			0.8	V
I_{OH}	High Level Output Current					−0.4			−0.4	mA
I_{OL}	Low Level Output Current					4			8	mA
f_{CLK}	Clock Frequency	'ALS192		0		20	0		25	MHz
		'ALS193		0		25	0		30	MHz
t_W	Pulse Duration	CLR High		10			10			ns
		$\overline{LOAD}$ Low		25			20			ns
		UP or DOWN High or Low	'ALS192	25			20			ns
			'ALS193	30			16.5			ns
t_{SU}	Setup Time	Data before $\overline{LOAD}$ ↑		25			20			ns
		CLR Inactive before UP ↑ or DOWN ↑		20			20			ns
		$\overline{LOAD}$ Inactive before UP ↑ or DOWN ↑		20			20			ns
		UP High before DOWN ↑		17			17			ns
		DOWN High before UP ↑		15			15			ns
t_H	Hold Time	Data after $\overline{LOAD}$ ↑		5			5			ns
		UP High after DOWN ↑		0			0			ns
		DOWN High after UP ↑		0			0			ns
T_A	Operating Free Air Temperature			−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range

Symbol	Parameter	Conditions			DM74ALS192, 193			Units
					Min	Typ (Note 1)	Max	
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA					−1.5	V
V_{OH}	High Level Output	V_{CC} = 4.5V to 5.5V, I_{OH} = −0.4 mA			V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 4 mA			0.25	0.4	V
		V_{CC} = 4.5V	74ALS I_{OL} = 8 mA			0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_I = 7V					0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_I = 2.7V					20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_I = 0.4V		UP, DOWN			−0.2	mA
				All Others			−0.1	mA

Electrical Characteristics over recommended operating free air temperature range (Continued)

Symbol	Parameter	Conditions	DM74ALS192, 193			Units
			Min	Typ (Note 1)	Max	
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V (Note 2)	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V (Note 3)		12	22	mA

Note 1: All typical values are at V_{CC} = 5V, T_A = 25°C.

Note 2: The output conditions have been chosen to produce a current that closely approximates one half of the true short circuit output current, I_{OS}.

Note 3: I_{CC} is measured with the clear and load inputs grounded, and all other inputs at 4.5V.

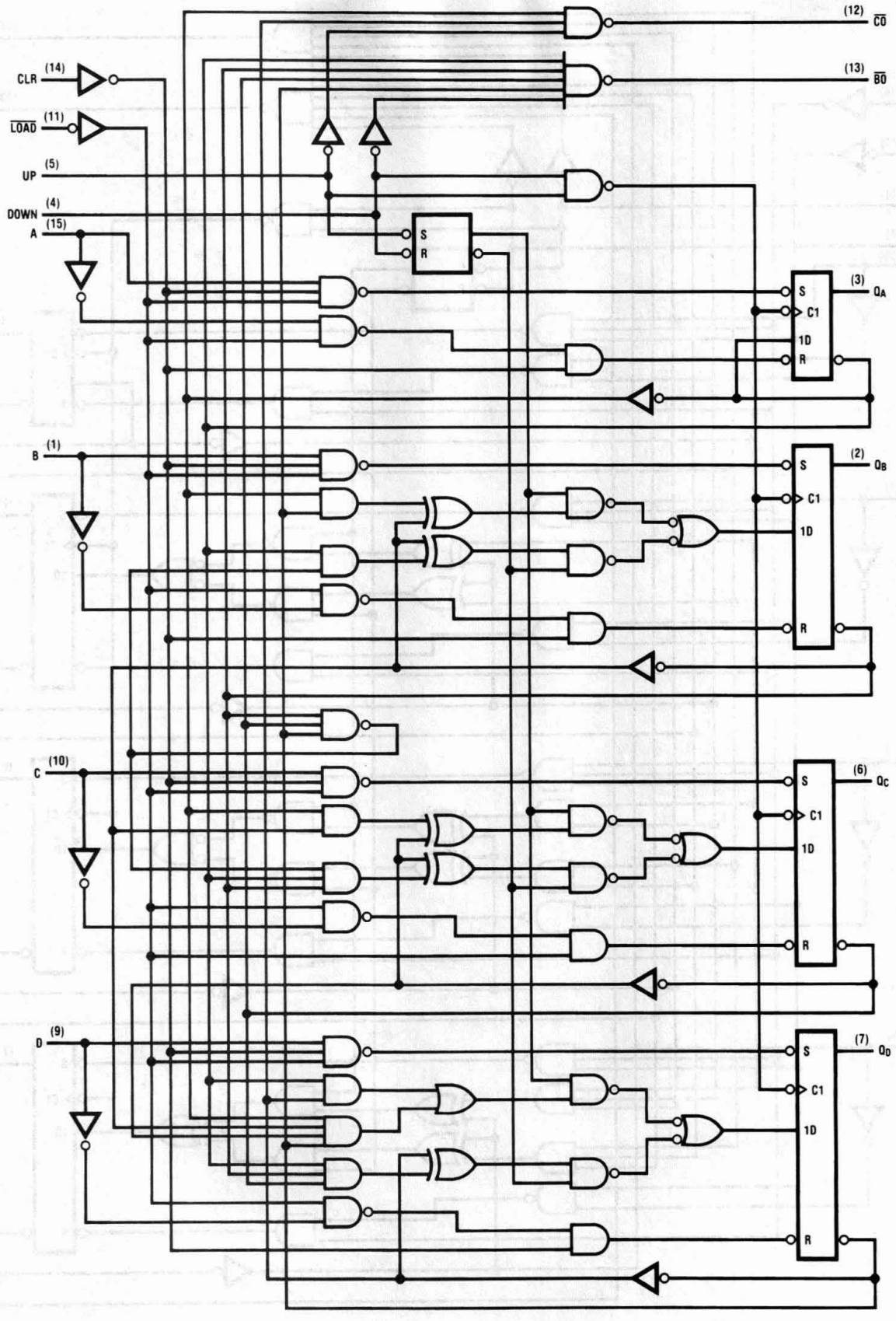
Switching Characteristics (Note 4)

Symbol	Parameter	Conditions	From (Input)	To (Output)	DM54ALS192, 193		DM74ALS192, 193		Units
					Min	Max	Min	Max	
f_{MAX}	'ALS192	V_{CC} = 4.5V to 5.5V			20		25		MHz
	'ALS193	C_L = 50 pF			25		30		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	R_L = 500Ω T_A = Min to Max	Up	C0	3	20	4	16	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Up	C0	3	21	5	18	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		Down	B0	4	20	4	16	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Down	B0	5	22	5	18	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		Up or Down	Any Q	4	27	4	19	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Up or Down	Any Q	4	23	4	17	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		$\overline{LOAD}$	Any Q	8	38	8	30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		$\overline{LOAD}$	Any Q	8	37	8	28	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		CLR	Any Q	5	20	5	17	ns

Note 4: See Section 1 for test waveforms and output load.

Logic Diagrams

'ALS192

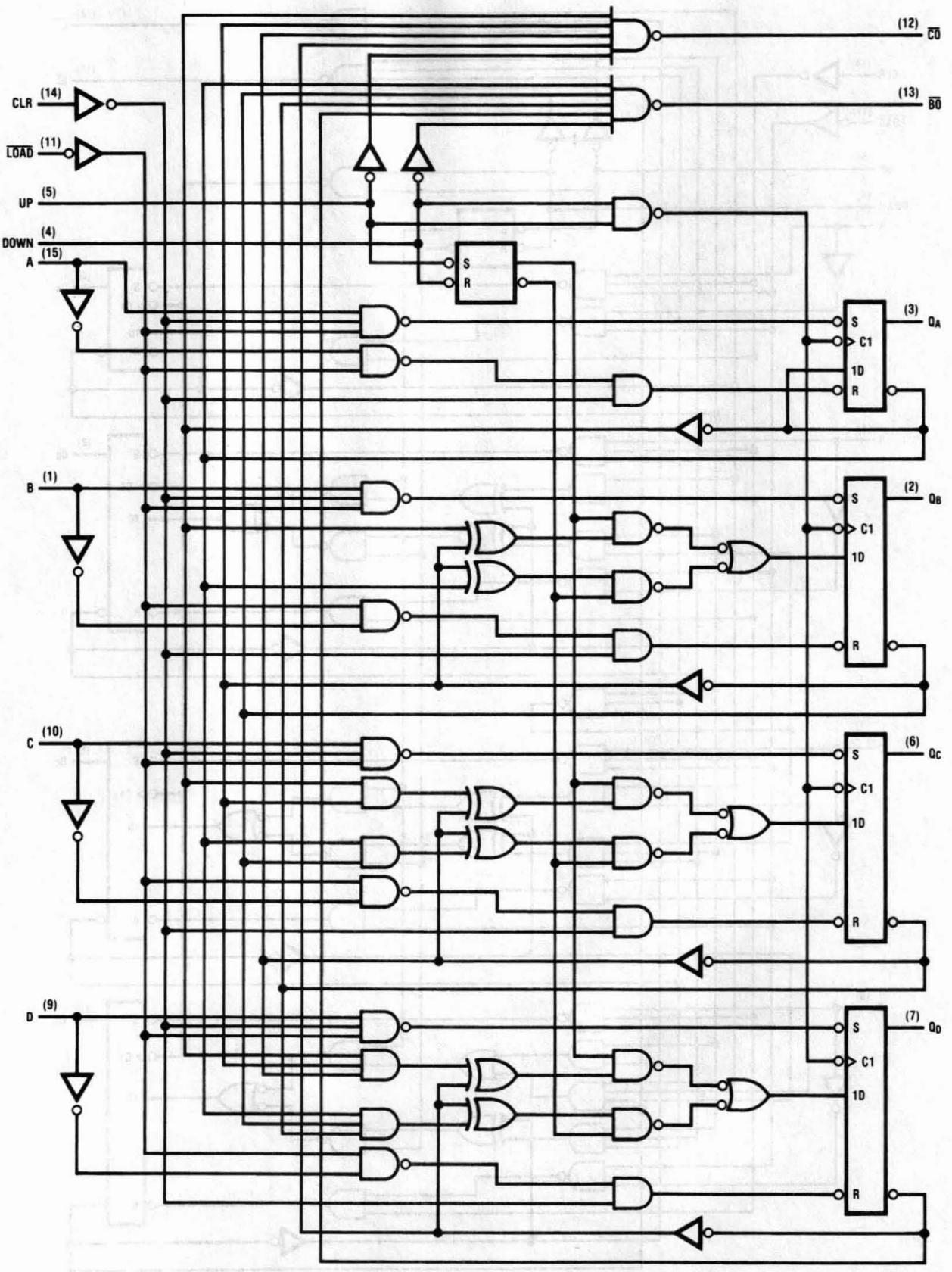


TL/F/6209–2

Pin numbers shown are for J and N packages.

Logic Diagrams (Continued)

'ALS193

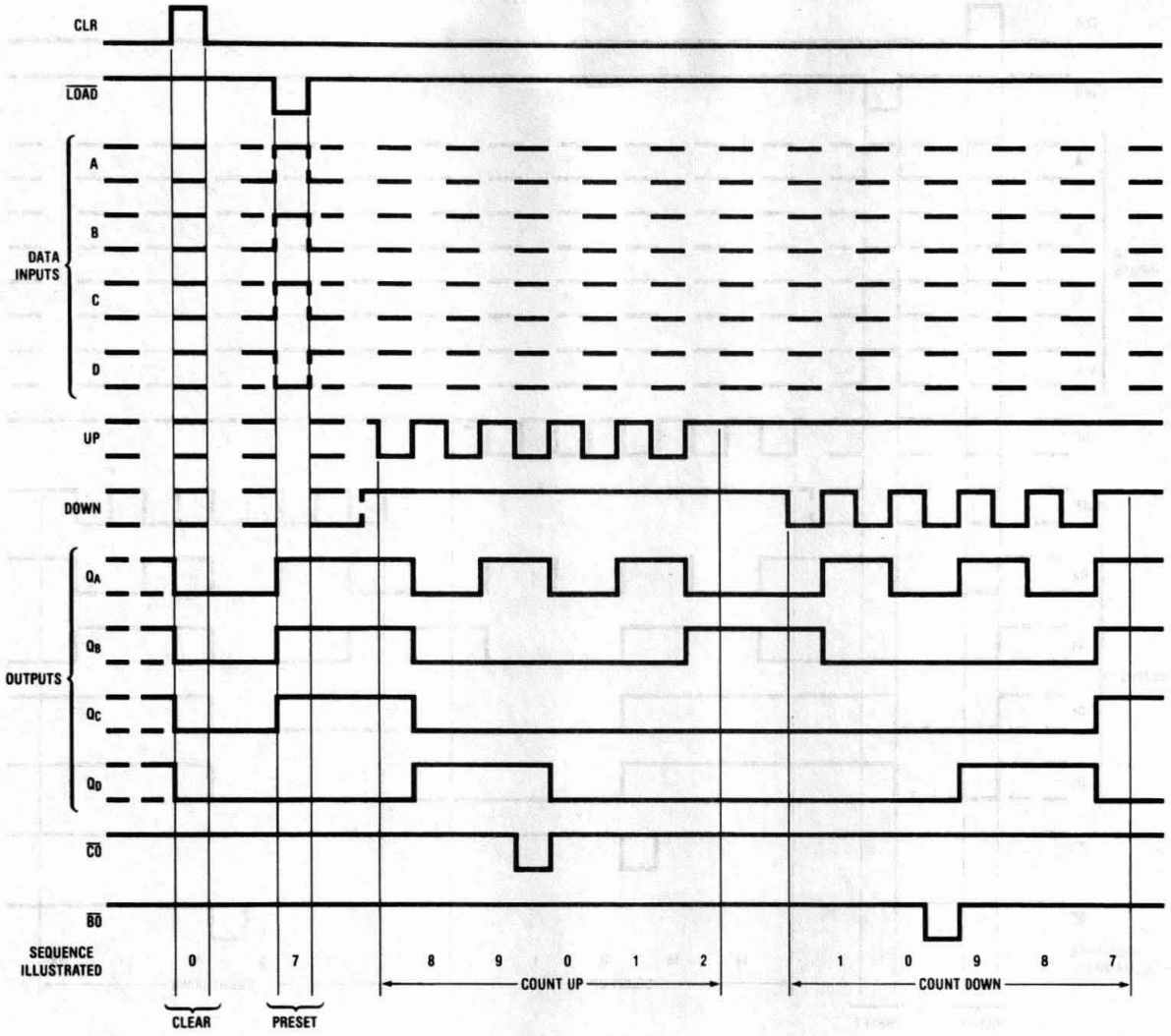


TL/F/6209–3

Pin numbers shown are for J and N packages.

Timing Diagrams

'ALS192 Typical Clear, Load and Count Sequences



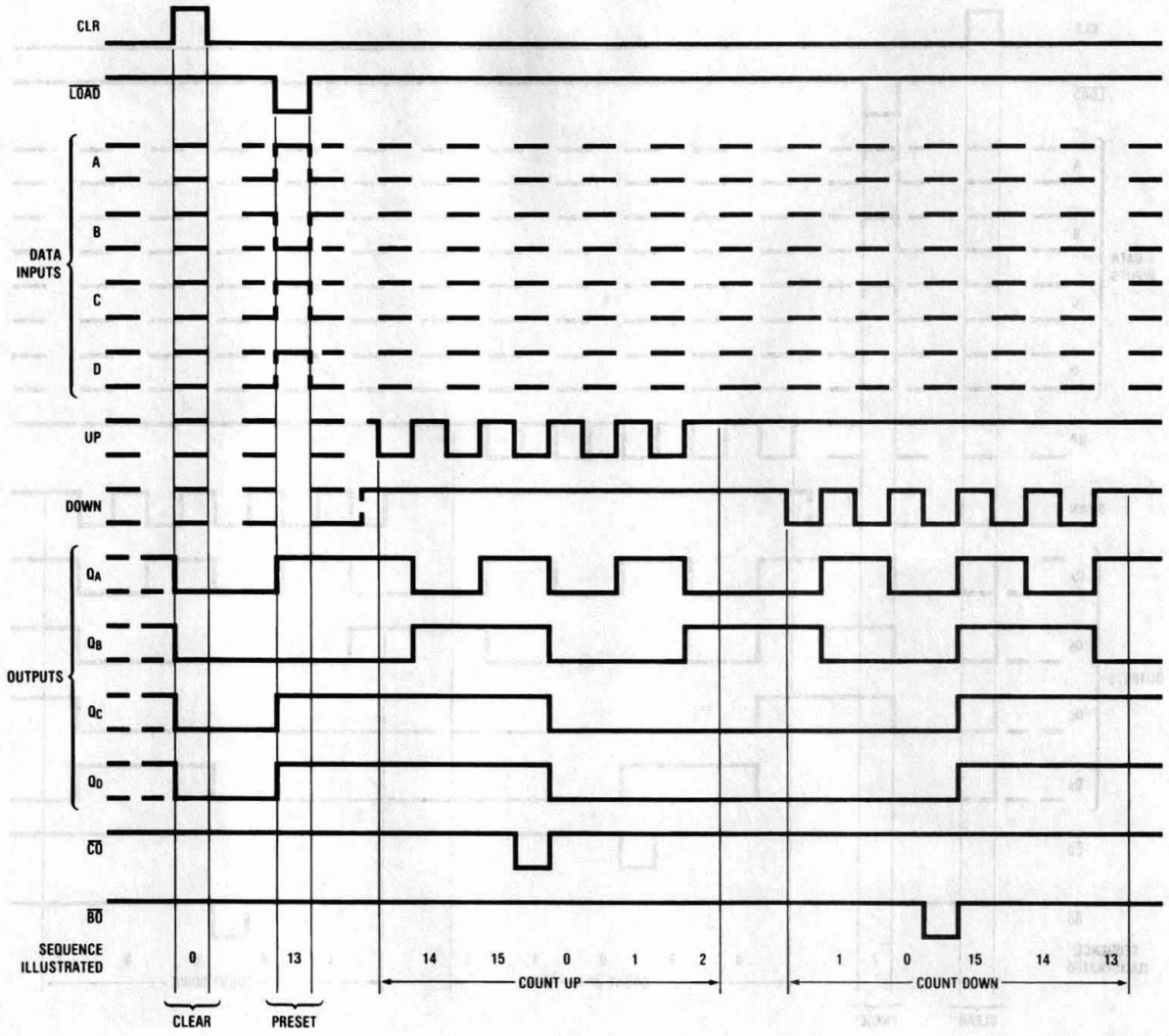
TL/F/6209–4

Note A: Clear overrides load, data, and count inputs.

Note B: When counting up, count-down input must be high; when counting down, count-up input must be high.

Timing Diagrams (Continued)

'ALS193 Typical Clear, Load and Count Sequences



TL/F/6209–5

Note A: Clear overrides load, data, and count inputs.

Note B: When counting up, count-down input must be high; when counting down, count-up input must be high.

National Semiconductor Corporation

DM54ALS240A/DM74ALS240A/DM54ALS241A/ DM74ALS241A Octal TRI-STATE® Bus Drivers

General Description

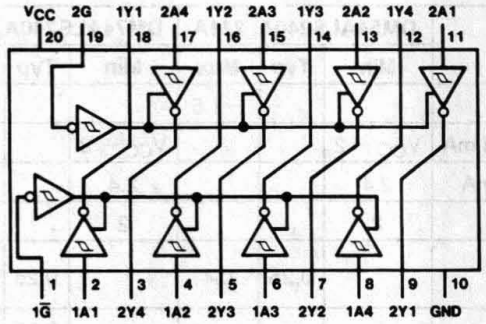
These octal TRI-STATE bus drivers are designed to provide the designer with flexibility in implementing a bus interface with memory, microprocessor, or communication systems. The output TRI-STATE gating control is organized into two separate groups of four buffers. The ALS240A control inputs symmetrically enable the respective outputs when set logic low, while the ALS241A has complementary enable gating. The TRI-STATE circuitry contains a feature that maintains the buffer outputs in TRI-STATE (high impedance state) during power supply ramp-up or ramp-down. This eliminates bus glitching problems that arise during power-up and power-down.

Features

- Advanced low power oxide-isolated ion-implanted Schottky TTL process
- Functional and pin compatible with the DM54/74LS counterpart
- Improved switching performance with less power dissipation compared with the DM54/74LS counterpart
- Switching response specified into 500Ω and 50 pF load
- Switching response specifications guaranteed over full temperature and V_{CC} supply range
- PNP input design reduces input loading
- Low level drive current: 54ALS = 12 mA, 74ALS = 24 mA

Connection Diagram

Dual-In-Line Package

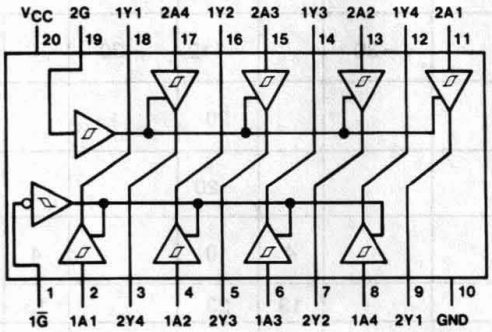


TL/F/6210–1

Top View

Order Number DM54ALS240AJ, DM74ALS240AWM or DM74ALS240AN
See NS Package Number J20A, M20B or N20A

Dual-In-Line Package



TL/F/6210–2

Top View

Order Number DM54ALS241AJ, DM74ALS241AWM or DM74ALS241AN
See NS Package Number J20A, M20B or N20A

Function Tables

'ALS240A

Input		Output
$\overline{G}$	A	Y
L	L	H
L	H	L
H	X	Z

'ALS241A

Input		Output
2G	2A	Y
H	L	L
H	H	H
L	X	Z

'ALS241A

Input		Output
1G	1A	Y
L	L	L
L	H	H
H	X	Z

H = High Level Logic State
L = Low Level Logic State
X = Don't Care (Either Low or High Level Logic State)
Z = High Impedance (Off) State

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V_{CC}	7V
Input Voltage	7V
Voltage Applied to Disabled Output	5.5V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS240A, 241A			DM74ALS240A, 241A			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Operating Free Air Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise specified)

Symbol	Parameter	Conditions		DM54ALS240A, 241A			DM74ALS240A, 241A			Units
				Min	Typ	Max	Min	Typ	Max	
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = 4.5V	I_{OH} = −3 mA	2.4			2.4			V
			I_{OH} = Max	2			2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 54ALS (Max)			0.25	0.4		0.25	0.4	V
		I_{OL} = 74ALS (Max)			—	—		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_I = 7V				0.1			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_I = 2.7V				20			20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1			−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	−30		−112	mA
I_{OZH}	High Level TRI-STATE Output Current	V_{CC} = 5.5V, V_O = 2.7V				20			20	μA
I_{OZL}	Low Level TRI-STATE Output Current	V_{CC} = 5.5V, V_O = 0.4V				−20			−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V, ALS240B Outputs High			4	10		4	10	mA
		Outputs Low			13	23		13	23	mA
		Outputs TRI-STATE			14	25		14	25	mA
		V_{CC} = 5.5V, ALS241B Outputs High			9	17		9	15	mA
		Outputs Low			15	28		15	26	mA
		Outputs TRI-STATE			17	32		17	30	mA

'ALS240A Switching Characteristics over recommended operating free air temperature range

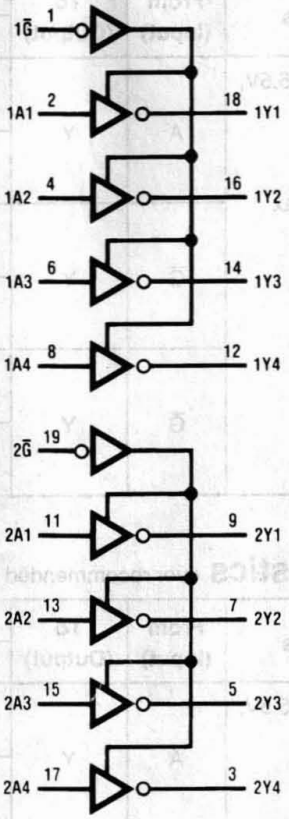
Symbol	Parameter	Conditions	From (Input)	To (Output)	DM54ALS240A		DM74ALS240A		Units
					Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R1 = 500Ω, R2 = 500Ω, T_A = Min to Max	A	Y	2	22	2	9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output				2	11	2	9	ns
t_{PZH}	Output Enable Time to High Level Output		$\overline{G}$	Y	4	34	5	13	ns
t_{PZL}	Output Enable Time to Low Level Output				5	26	5	18	ns
t_{PHZ}	Output Disable Time from High Level Output		$\overline{G}$	Y	1	15	2	10	ns
t_{PLZ}	Output Disable Time from Low Level Output				3	24	3	12	ns

'ALS241A Switching Characteristics over recommended operating free air temperature range

Symbol	Parameter	Conditions	From (Input)	To (Output)	DM54ALS241A		DM74ALS241A		Units
					Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R1 = 500Ω, R2 = 500Ω, T_A = Min to Max	A	Y	3	31	3	11	ns
t_{PHL}	Propagation Delay Time High to Low Level Output				1	14	3	10	ns
t_{PZH}	Output Enable Time to High Level Output		$1\overline{G}$	Y	5	33	7	21	ns
t_{PZL}	Output Enable Time to High Level Output				7	27	7	21	ns
t_{PHZ}	Output Disable Time to High Level Output		$1\overline{G}$	Y	2	13	2	10	ns
t_{PLZ}	Output Disable Time to Low Level Output				2	32	3	15	ns
t_{PZH}	Output Enable Time to High Level Output		2G	Y	7	38	7	21	ns
t_{PZL}	Output Enable Time to Low Level Output				7	30	7	21	ns
t_{PHZ}	Output Disable Time from High Level Output		2G	Y	2	17	2	10	ns
t_{PLZ}	Output Disable Time from Low Level Output				3	35	3	15	ns

Logic Diagrams

DM54/74ALS240A



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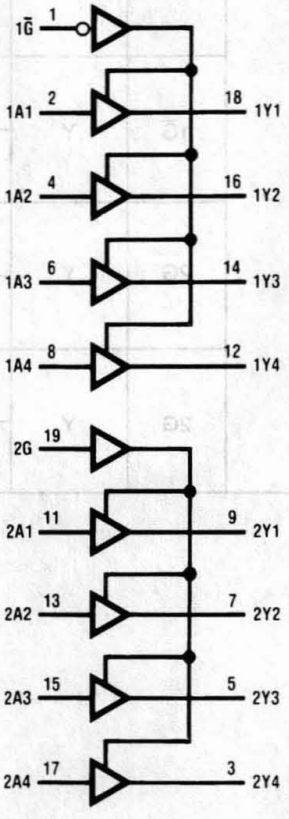
DM54/74ALS241A



TL/F/6210–4

National Semiconductor Corporation

DM54ALS242B/DM74ALS242B/ DM54ALS243A/DM74ALS243A Quad TRI-STATE® Bidirectional Bus Drivers

General Description

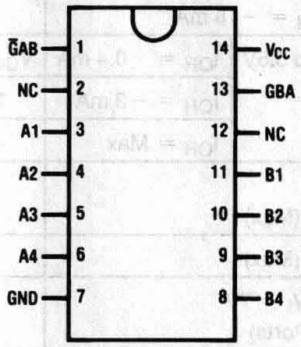
These octal TRI-STATE® bus drivers are designed to provide the designer with flexibility in implementing a bus interface with memory, microprocessor, or communication systems. The ALS242B has inverting buffers, while the ALS243A has non-inverting buffers. The direction enable gating is configured with separate control over either buffer direction and the two control buffers are complementary. Connecting these control inputs to one common line implements single line direction control, while individual control can put both buffer directions into TRI-STATE simultaneously (disabled state) or put both buffer directions into the active state (data latch state). The TRI-STATE circuitry contains a feature that maintains the buffer outputs in TRI-STATE (high impedance state) during power supply ramp-up or ramp-down. This eliminates bus glitching problems that arise during power-up and power-down.

Features

- Advanced low power oxide-isolated ion-implanted Schottky TTL process
- Functional and pin compatible with the DM54/74LS counterpart
- Improved switching performance with less power dissipation compared with the DM54/74LS counterpart
- Switching response specified into 500Ω and 50 pF load
- Switching response specifications guaranteed over full temperature and V_{CC} supply range
- PNP input design reduces input loading
- Low level drive current:
  54ALS = 12 mA, 74ALS = 24 mA

Connection Diagram

Dual-In-Line Package



TL/F/6211–1

Top View

Order Number DM54ALS242BJ, DM54ALS243AJ, DM74ALS242BM, DM74ALS242BN, DM74ALS243AM, DM74ALS243AN
See NS Package Number J14A, M14A or N14A

Function Table

Inputs		'ALS242B	'ALS243A
$\overline{G}AB$	GBA		
L	L	$\overline{A}$ to B	A to B
H	H	$\overline{B}$ to A	B to A
H	L	Isolation	Isolation
L	H	Latch A and B ($A = \overline{B}$)	Latch A and B ($A = B$)

2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V_{CC}	7V
Input Voltage	
Dedicated Inputs	7V
I/O Ports	5.5V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0 to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS242B, 243A			DM74ALS242B, 243A			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Operating Free-Air Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free-air temperature (unless otherwise specified)

Symbol	Parameter	Conditions		DM54ALS242B, 243A			DM74ALS242B, 243A			Units
				Min	Typ	Max	Min	Typ	Max	
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2			−1.2	V
V_{OH}	High Level Output	V_{CC} = 4.5V to 5.5V	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = 4.5V	I_{OH} = −3 mA	2.4			2.4			V
			I_{OH} = Max	2			2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 54ALS (Max)			0.25	0.4		0.25	0.4	V
		I_{OL} = 74ALS (Max)			—	—		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_I = 7V (5.5V for I/O Ports)				0.1			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_I = 2.7V (Note 1)				20			20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V (Note 1)				−0.1			−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V, ALS242B Active Outputs High			10	20		10	16	mA
		Active Outputs Low			14	26		14	21	mA
		Outputs TRI-STATE			12	24		12	19	mA
		V_{CC} = 5.5V, ALS243A Active Outputs High			15	30		15	25	mA
		Active Outputs Low			20	35		20	30	mA
		Outputs TRI-STATE			21	37		21	32	mA

Note 1: For the I/O ports, the parameters I_{IH} and I_{IL} include the TRI-STATE output currents (I_{OZH} and I_{OZL}).

'ALS242B Switching Characteristics over recommended operating free-air temperature range (Note 1)

Symbol	Parameter	Conditions	From (Input)	To (Output)	54ALS242B		74ALS242B		Units
					Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R1 = 500Ω, R2 = 500Ω, T_A = Min to Max	A or B	B or A	2	15	2	11	ns
t_{PHL}	Propagation Delay Time High to Low Level Output				2	14	2	10	ns
t_{PZH}	Output Enable Time to High Level Output		$\overline{G}$AB	B	4	22	4	18	ns
t_{PZL}	Output Enable Time to Low Level Output				7	25	7	21	ns
t_{PHZ}	Output Disable Time to High Level Output		$\overline{G}$AB	B	2	16	2	14	ns
t_{PLZ}	Output Disable Time to Low Level Output				2	18	2	12	ns
t_{PZH}	Output Enable Time to High Level Output		GBA	A	4	22	4	18	ns
t_{PZL}	Output Enable Time to Low Level Output				7	25	7	21	ns
t_{PHZ}	Output Disable Time from High Level Output		GBA	A	2	16	2	14	ns
t_{PLZ}	Output Disable Time from Low Level Output				2	18	2	12	ns

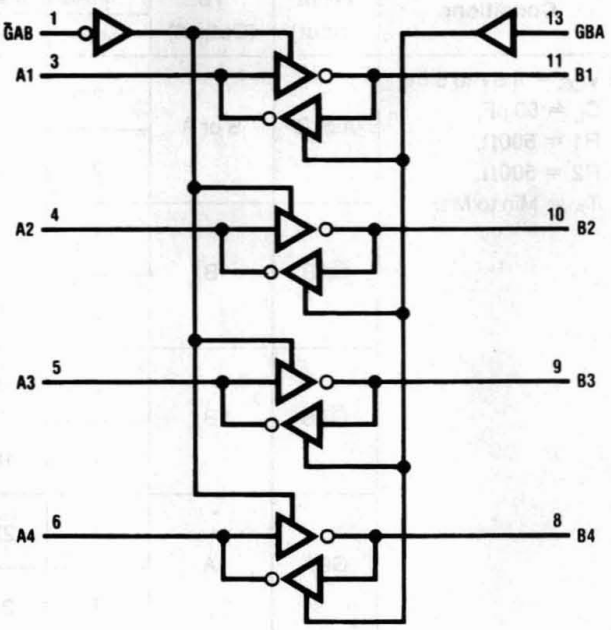
'ALS243A Switching Characteristics over recommended operating free-air temperature range (Note 1)

Symbol	Parameter	Conditions	From (Input)	To (Output)	54ALS243A		74ALS243A		Units
					Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R1 = 500Ω, R2 = 500Ω, T_A = Min to Max	A or B	B or A	4	15	4	11	ns
t_{PHL}	Propagation Delay Time High to Low Level Output				4	15	4	11	ns
t_{PZH}	Output Enable Time to High Level Output		$\overline{G}$AB	B	7	25	7	20	ns
t_{PZL}	Output Enable Time to Low Level Output				7	25	7	20	ns
t_{PHZ}	Output Disable Time to High Level Output		$\overline{G}$AB	B	2	16	2	14	ns
t_{PLZ}	Output Disable Time to Low Level Output				3	27	3	22	ns
t_{PZH}	Output Enable Time to High Level Output		GBA	A	7	25	7	20	ns
t_{PZL}	Output Enable Time to Low Level Output				7	25	7	20	ns
t_{PHZ}	Output Disable Time from High Level Output		GBA	A	2	16	2	14	ns
t_{PLZ}	Output Disable Time from Low Level Output				3	27	3	22	ns

Note 1: See Section 1 for test waveforms and output loads.

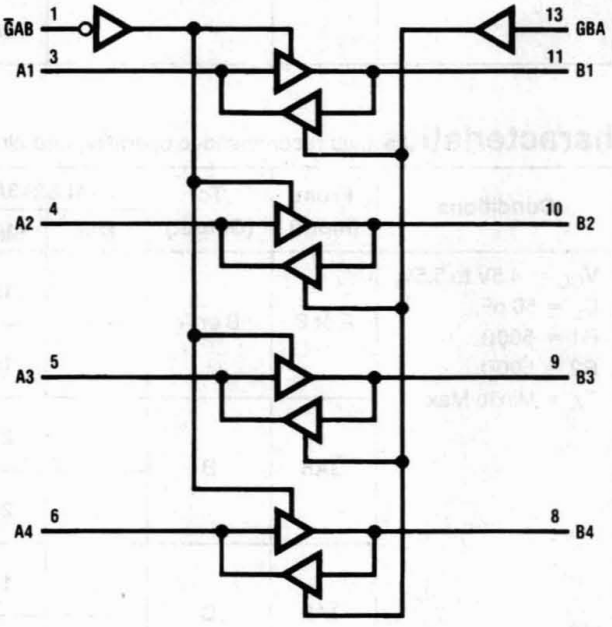
Logic Diagrams

DM54/74ALS242B



TL/F/6211–2

DM54/74ALS243A



TL/F/6211–3

National Semiconductor Corporation

DM54ALS244A/DM74ALS244A Octal TRI-STATE® Bus Driver

General Description

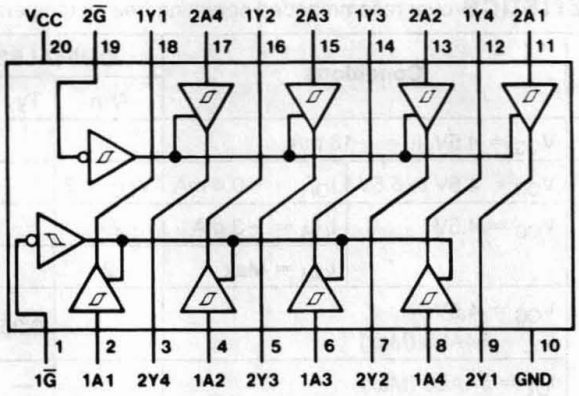
This octal TRI-STATE bus driver is designed to provide the designer with flexibility in implementing a bus interface with memory, microprocessor, or communication systems. The output TRI-STATE gating control is organized into two separate groups of four buffers, and both control inputs enable the respective outputs when set logic low. The TRI-STATE circuitry contains a feature that maintains the buffer outputs in TRI-STATE (high impedance state) during power supply ramp-up or ramp-down. This eliminates bus glitching problems that arise during power-up and power-down.

Features

- Advanced low power oxide-isolated ion-implanted Schottky TTL process
- Functional and pin compatible with the DM54/74LS counterpart
- Improved switching performance with less power dissipation compared with the DM54/74LS counterpart
- Switching response specified into 500Ω and 50 pF load
- Switching response specifications guaranteed over full temperature and V_{CC} supply range
- PNP input design reduces input loading
- Low level drive current:
  54ALS = 12 mA, 74ALS = 24 mA

Connection Diagram

Dual-In-Line Package



TL/F/6212–1

Top View
Order Number DM54ALS244AJ, DM74ALS244AWM or DM74ALS244AN
See NS Package Number J20A, M20B or N20A

Function Table

Input		Output
$\overline{G}$	A	Y
L	L	L
L	H	H
H	X	Z

H = High Level Logic State
L = Low Level Logic State
X = Don't Care (Either Low or High Level Logic State)
Z = High Impedance (Off) State

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V_{CC}	7V
Input Voltage	7V
Voltage Applied to Disabled Output	5.5V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0 to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS244A			DM74ALS244A			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Operating Free-Air Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise specified)

Symbol	Parameter	Conditions		DM54ALS244A			DM74ALS244A			Units
				Min	Typ	Max	Min	Typ	Max	
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = 4.5V	I_{OH} = −3 mA	2.4			2.4			V
			I_{OH} = Max	2			2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 54ALS (Max)			0.25	0.4		0.25	0.4	V
		I_{OL} = 74ALS (Max)			—	—		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_I = 7V				0.1			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_I = 2.7V				20			20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1			−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	−30		−112	mA
I_{OZH}	High Level TRI-STATE Output Current	V_{CC} = 5.5V, V_O = 2.7V				20			20	μA
I_{OZL}	Low Level TRI-STATE Output Current	V_{CC} = 5.5V, V_O = 0.4V				−20			−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V, Outputs High			9	15		9	15	mA
		Outputs Low			15	24		15	24	mA
		Outputs TRI-STATE			17	27		17	27	mA

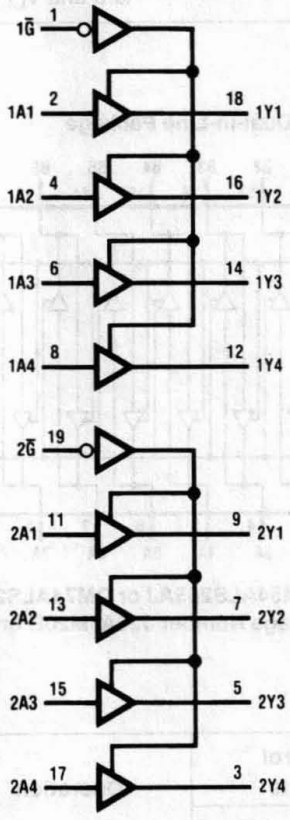
Switching Characteristics over recommended operating free-air temperature range (Note 1)

Symbol	Parameter	From (Input)	To (Output)	Conditions	54ALS244A		74ALS244A		Units
					Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	A	Y	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R1 = 500Ω, R2 = 500Ω, T_A = Min to Max	1	18	3	10	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A	Y		3	13	3	10	ns
t_{PZH}	Output Enable Time to High Level Output	$\overline{G}$	Y		1	29	7	20	ns
t_{PZL}	Output Enable Time to Low Level Output	$\overline{G}$	Y		1	27	7	20	ns
t_{PHZ}	Output Disable Time from High Level Output	$\overline{G}$	Y		2	12	2	10	ns
t_{PLZ}	Output Disable Time from Low Level Output	$\overline{G}$	Y		1	21	3	13	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram

DM54/74ALS244B



TL/F/6212–2

National Semiconductor Corporation

DM54ALS245A/DM74ALS245A Octal TRI-STATE® Bus Transceivers

General Description

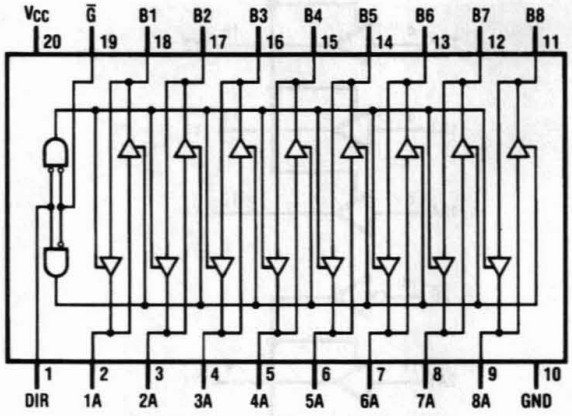
This advanced low power Schottky device contains 8 pairs of TRI-STATE logic elements configured as octal bus transceivers. These circuits are designed for use in memory, microprocessor systems and in asynchronous bidirectional data buses. Two way communication between buses is controlled by the (DIR) input. Data transmits either from the A bus to the B bus or from the B bus to the A bus. Both the driver and receiver outputs can be disabled via the ($\overline{G}$) enable input which causes outputs to enter the high impedance mode so that the buses are effectively isolated.

Features

- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Non-inverting logic output
- Glitch free bus during power up and down
- TRI-STATE outputs independently controlled on A and B buses
- Low output impedance to drive terminated transmission lines to 133Ω
- Switching response specified into 500Ω/50 pF
- Specified to interface with CMOS at $V_{OH} = V_{CC} - 2V$
- PNP inputs to reduce input loading
- Switching specifications guaranteed over full temperature and V_{CC} range

Connection Diagram

Dual-In-Line Package



TL/F/6213–1

Order Number DM54ALS245AJ or DM74ALS245AWM, N
See NS Package Number J20A, M20B or N20A

Function Table

Control Inputs		Operation
$\overline{G}$	DIR	
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	Hi-Z

H = High Logic Level
L = Low Logic Level
X = Either High or Low Logic Level

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	
Control Inputs	7V
I/O Ports	5.5V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

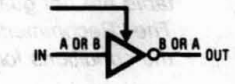
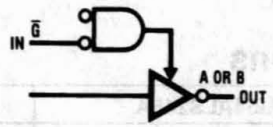
Symbol	Parameter	DM54ALS245A			DM74ALS245A			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Operating Free Air Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions			Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18 mA					−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, I_{OH} = −3 mA			2.4	3.2		V
		V_{CC} = 4.5V, I_{OH} = Max			2	2.3		V
		I_{OH} = −0.4 mA, V_{CC} = 4.5V to 5.5V			V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 12 mA			0.25	0.4	V
			74ALS I_{OL} = 24 mA			0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V	V_{IN} = 7V	Control Inputs			0.1	mA
			V_{IN} = 5.5V	A or B Ports			0.1	
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IN} = 2.7V					20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V					−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_{OUT} = 2.25V			−30		−112	mA
I_{CC}	54ALS254A Supply Current	V_{CC} = 5.5V	Outputs High			30	48	mA
			Outputs Low			38	60	mA
			TRI-STATE			38	63	mA
I_{CC}	74ALS254A Supply Current	V_{CC} = 5.5V	Outputs High			30	45	mA
			Outputs Low			36	55	mA
			TRI-STATE			38	58	mA

Switching Characteristics over recommended operating free air temperature range (Notes 1 and 2)

Symbol	Parameter	Circuit Configuration	DM54ALS245A		DM74ALS245A		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time High-to-Low Level Output		1	19	3	10	ns
t_{PHL}	Propagation Delay Time High-to-Low Level Output		1	14	3	10	ns
t_{PZL}	Output Enable Time to Low Level		2	29	5	20	ns
t_{PZH}	Output Enable Time to High Level		2	30	5	20	ns
t_{PLZ}	Output Disable Time from Low Level		2	30	4	15	ns
t_{PHZ}	Output Disable Time from High Level		2	14	2	10	ns

Note 1: See Section 1 for test waveforms and output load.

Note 2: Switching characteristic conditions are V_{CC} = 4.5V to 5.5V, R_L = 500Ω, C_L = 50 pF.

National Semiconductor Corporation

DM54ALS251/DM74ALS251 TRI-STATE® 1 of 8 Line Data Selector/Multiplexer

General Description

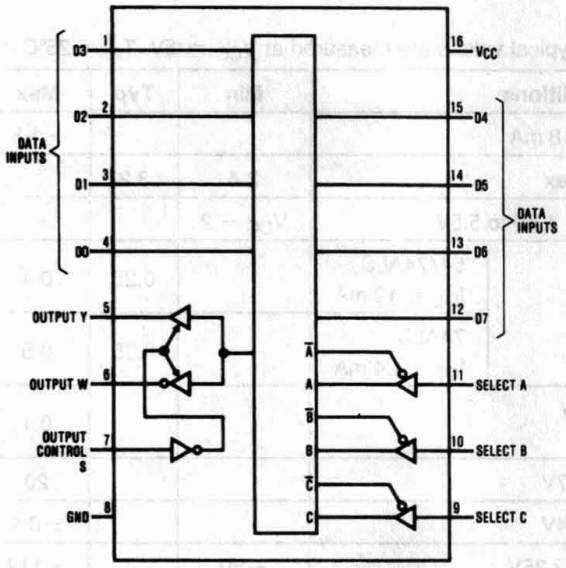
This Data Selector/Multiplexer contains full on-chip decoding to select one-of-eight data sources as a result of a unique three-bit binary code at the Select inputs. Two complementary outputs provide both inverting and non-inverting buffer operation. An Output Control input is provided which, when at the high level, places both outputs in the high impedance Off state. In order to prevent bus access conflicts, output disable times are shorter than output enable times. The Select input buffers incorporate internal overlap features to ensure that select input changes do not cause invalid output transients.

Features

- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Switching performance is guaranteed over full temperature and V_{CC} supply range
- Pin and functional compatible with LS family counterpart
- Improved output transient handling capability
- Output control circuitry incorporates power-up TRI-STATE feature

Connection Diagram

Dual-In-Line Package



TL/F/6214–1

Order Number DM54ALS251J or DM74ALS251M, N
See NS Package Number J16A, M16A or N16A

Function Table

Inputs				Outputs	
Select			Strobe		
C	B	A	S	Y	W
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = High Level, L = Low Level, X = Don't Care

Z = High Impedance (Off)

D0 thru D7 = The Level of the Respective D Input

2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V_{CC}	7V
Input Voltage	7V
Voltage Applied to Disabled Output	5.5V
Operating Free Air Temperature Range	
DM54ALS251	−55°C to +125°C
DM74ALS251	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS251			DM74ALS251			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

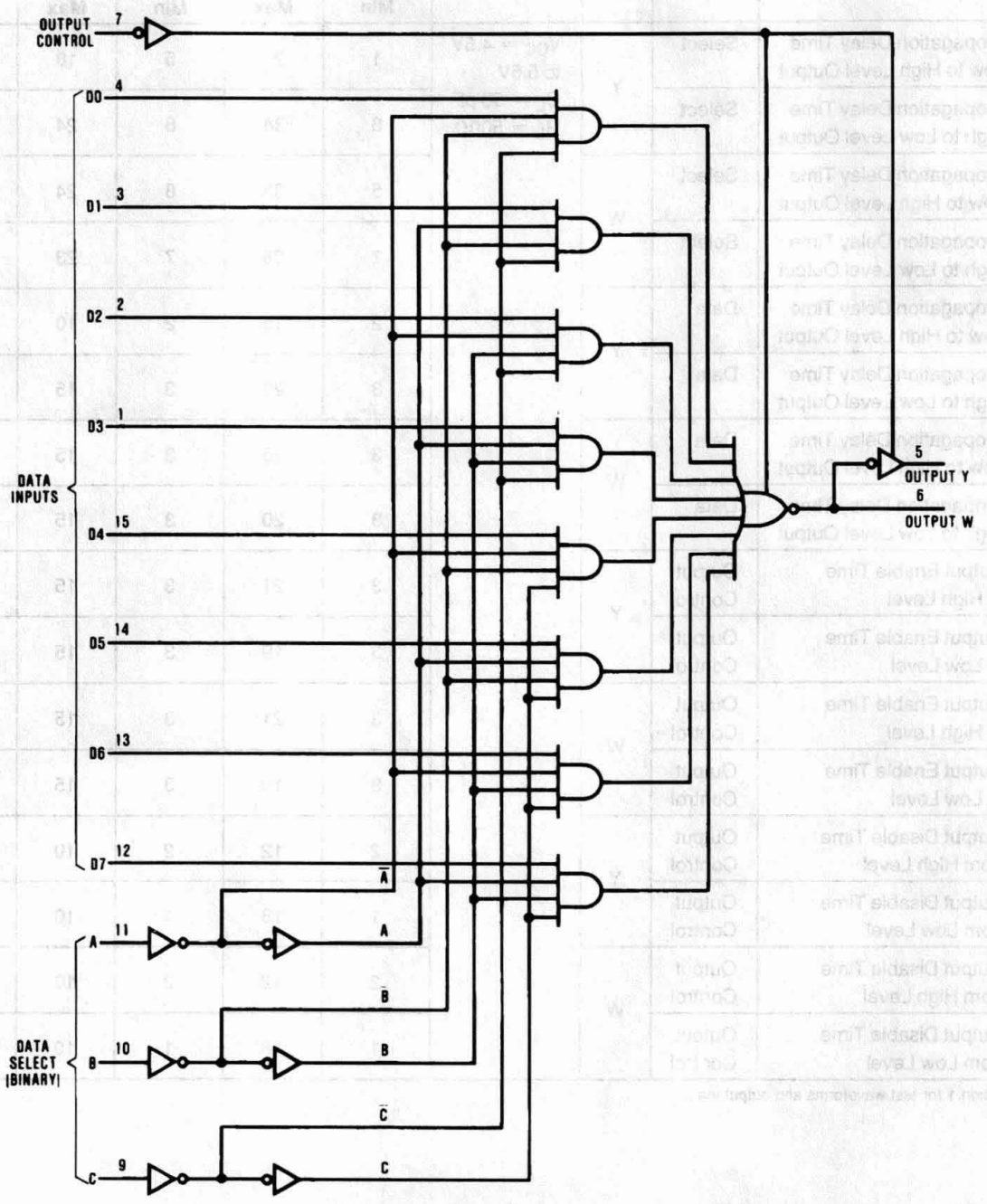
Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, I_{OH} = Max		2.4	3.2		V
		I_{OH} = 400 μA, V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 12 mA		0.25	0.4	V
			74ALS I_{OL} = 24 mA		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_{OUT} = 2.25V		−30		−112	mA
I_{OZH}	Off-State Output Current, High Bias	V_{CC} = 5.5V, V_{OUT} = 2.7V				20	μA
I_{OZL}	Off-State Output Current, Low Bias	V_{CC} = 5.5V, V_{OUT} = 0.4V				−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V, Inputs = GND	Enabled		7	10	mA
		Inputs = 4.5V, V_{CC} = 5.5V	Disabled		9.4	14	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	From	To	Conditions	DM54ALS251		DM74ALS251		Units
					Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Select	Y	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R_L = 500Ω	1	21	5	18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select	Y		8	34	8	24	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select	W		5	38	8	24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select	W		7	26	7	23	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Data	Y		2	15	2	10	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data	Y		3	23	3	15	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Data	W		3	25	3	15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data	W		3	20	3	15	ns
t_{PZH}	Output Enable Time to High Level	Output Control	Y		3	21	3	15	ns
t_{PZL}	Output Enable Time to Low Level	Output Control	Y		3	19	3	15	ns
t_{PZH}	Output Enable Time to High Level	Output Control	W		3	21	3	15	ns
t_{PZL}	Output Enable Time to Low Level	Output Control	W		3	19	3	15	ns
t_{PHZ}	Output Disable Time from High Level	Output Control	Y		2	12	2	10	ns
t_{PLZ}	Output Disable Time from Low Level	Output Control	Y		1	18	1	10	ns
t_{PHZ}	Output Disable Time from High Level	Output Control	W		2	12	2	10	ns
t_{PLZ}	Output Disable Time from Low Level	Output Control	W		1	18	1	10	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6214–2

National Semiconductor Corporation

PRELIMINARY

DM54ALS253/DM74ALS253 TRI-STATE® Dual 1 of 4 Line Data Selector/Multiplexer

General Description

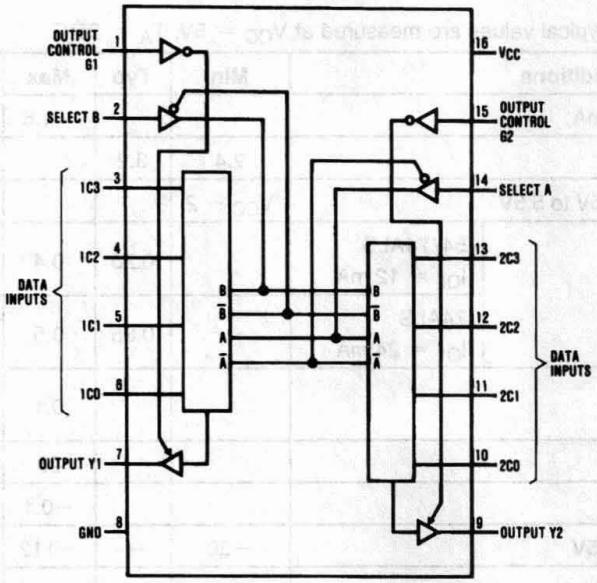
This Data Selector/Multiplexer contains full on-chip decoding to select one-of-four data sources as a result of a unique two-bit binary code at the Select Inputs. Each of the two Data Selector/Multiplexer circuits have their own separate Data and Output Control inputs and a non-inverting TRI-STATE output buffer. The Output Control inputs, when at the high level, place the corresponding output in the high impedance Off state. In order to prevent bus access conflicts, output disable times are shorter than output enable times. The Select input buffers incorporate internal overlap features to ensure that select input changes do not cause invalid output transients.

Features

- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Switching performance is guaranteed over full temperature and V_{CC} supply range
- Pin and functional compatible with LS family counterpart
- Improved output transient handling capability
- Output control circuitry incorporates power-up TRI-STATE feature

Connection Diagram

Dual-In-Line Package



TL/F/6215–1

Order Number DM54ALS253J, DM74ALS253M or DM74ALS253N
See NS Package Number J16A, M16A or N16A

Function Table

Select Inputs		Data Inputs				Output Control	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs A and B are common to both sections

H = High Level, L = Low Level, X = Don't Care, Z = High Impedance

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V_{CC}	7V
Input Voltage	7V
Voltage Applied to Disabled Output	5.5V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS253			DM74ALS253			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, I_{OH} = Max		2.4	3.2		V
		I_{OH} = 400 μA, V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 12 mA		0.25	0.4	V
			74ALS I_{OL} = 24 mA		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IN} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IN} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_{OUT} = 2.25V		−30		−112	mA
I_{OZH}	Off-State Output Current, High Bias	V_{CC} = 5.5V, V_{OUT} = 2.7V				20	μA
I_{OZL}	Off-State Output Current, Low Bias	V_{CC} = 5.5V, V_{OUT} = 0.4V				−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V	Output High		6.5	12	mA
			Output Low		6.5	12	
			Output Disabled		7.5	14	

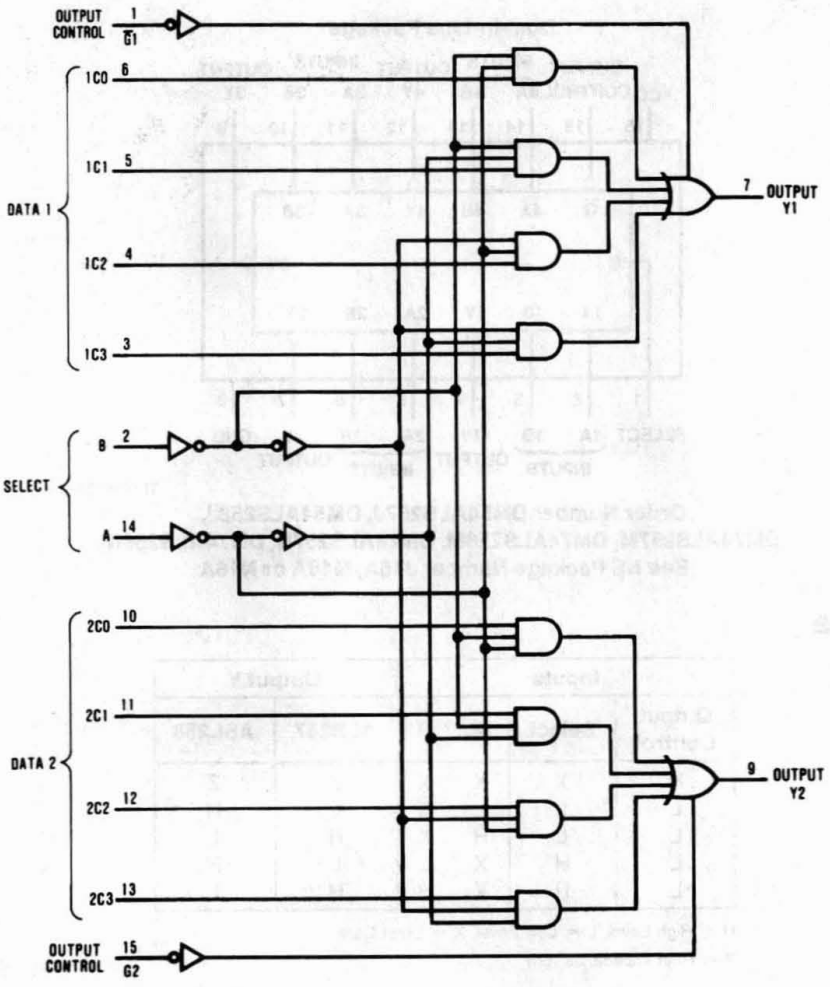
Switching Characteristics

over recommended operating free air temperature range (Note 1). All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	From (Input) To (Output)	Conditions	DM54ALS253		DM74ALS253		Units
				Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Y	V_{CC} = 4.5V to 5.5V C_L = 50 pF R_L = 500Ω	5	30	5	21	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Y		5	27	5	21	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Y		2	15	2	10	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Y		3	18	3	14	ns
t_{PZH}	Output Enable Time to High Level Output	Output Control to Y		3	20	3	14	ns
t_{PZL}	Output Enable Time to Low Level Output	Output Control to Y		2	19	4	16	ns
t_{PHZ}	Output Disable Time from High Level Output	Output Control to Y		2	12	2	10	ns
t_{PLZ}	Output Disable Time from Low Level Output	Output Control to Y		2	18	2	14	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6215–2

National Semiconductor Corporation

DM54ALS/DM74ALS257, 258 TRI-STATE® Quad 1-of-2-Line Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four TRI-STATE outputs that can interface directly with data lines of bus-organized systems. A 4-bit word selected from one of two sources is routed to the four outputs. The ALS257 presents true data whereas the ALS258 presents inverted data to minimize propagation delay time.

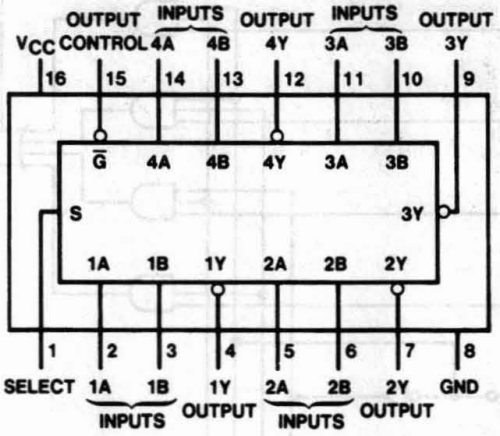
This TRI-STATE output feature means that n-bit (paralleled) data selectors with up to 258 sources can be implemented for data buses. It also permits the use of standard TTL registers for data retention throughout the system.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky and low power Schottky TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts
- TRI-STATE buffer-type outputs drive bus lines directly
- Expand any data input point
- Multiplex dual data buses
- General four functions of two variables (one variable is common)
- Source programmable counters

Connection Diagram

Dual-In-Line Package



TL/F/6227–1

Order Number DM54ALS257J, DM54ALS258J, DM74ALS257M, DM74ALS258M, DM74ALS257N, DM74ALS258N
See NS Package Number J16A, M16A or N16A

Function Table

Inputs				Output Y	
Output Control	Select	A	B	ALS257	ASL258
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = High Level, L = Low Level, X = Don't Care
Z = High Impedance (off)

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Voltage Applied to Disabled Output	5.5V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS257, 258			DM74ALS257, 258			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter		Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage		V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage		V_{CC} = 4.5V, V_{IL} = Max	54ALS I_{OH} = −1 mA	2.4	3.2		V
				74ALS I_{OH} = −2.6 mA	2.4	3.3		V
			I_{OH} = −0.4 mA	54/74ALS	V_{CC} − 2			V
V_{OL}	Low Level Output Voltage		V_{CC} = 4.5V, V_{IH} = 2V	54/74ALS I_{OL} = 12 mA		0.25	0.4	V
				74ALS I_{OL} = 24 mA		0.35	0.5	V
I_I	Input Current at Max Input Voltage		V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current		V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current		V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current		V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied		V_{CC} = 5.5V, V_{IH} = 2V, V_O = 2.7V				20	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied		V_{CC} = 5.5V, V_{IH} = 2V, V_O = 0.4V				−20	μA
I_{CCH}	Supply Current	ALS257	V_{CC} = 5.5V, Outputs Open	Outputs High		3	6	mA
		ALS258				2.5	4	mA
I_{CCL}	Supply Current	ALS257		Outputs Low		8	12	mA
		ALS258				7	11	mA
I_{CCZ}	Supply Current	ALS257		Outputs Disabled		9	14	mA
		ALS258				8	13	mA

2

'ALS257 Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From	To	DM54ALS257		DM74ALS257		Units
					Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V C_L = 50 pF R_L = 500Ω	Data	Any Y	2	12	2	10	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Data	Any Y	2	14	2	12	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		Select	Any Y	4	21	4	18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Select	Any Y	5	25	5	22	ns
t_{ZH}	Output Enable Time to High Level		Output Control	Any Y	4	20	4	16	ns
t_{ZL}	Output Enable Time to Low Level		Output Control	Any Y	5	22	5	18	ns
t_{HZ}	Output Disable Time from High Level		Output Control	Any Y	2	12	2	10	ns
t_{LZ}	Output Disable Time from Low Level		Output Control	Any Y	3	35	3	15	ns

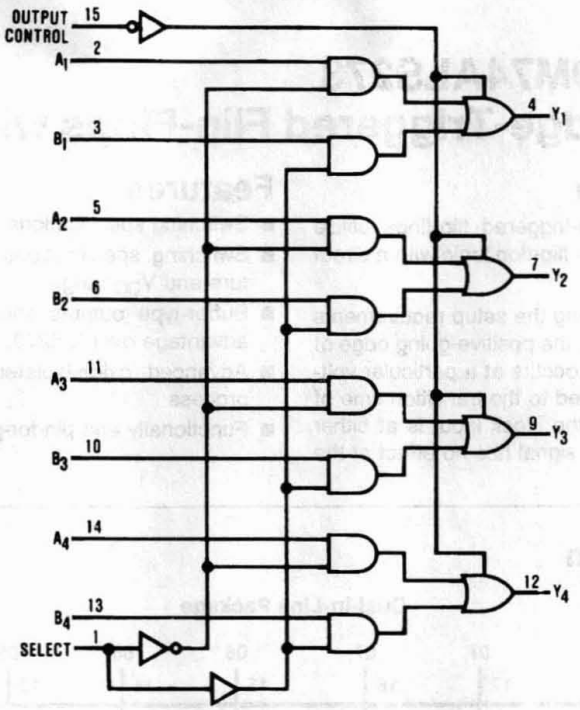
'ALS258 Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From	To	DM54ALS258		DM74ALS258		Units
					Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V C_L = 50 pF R_L = 500Ω	Data	Any Y	1	12	2	8	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Data	Any Y	2	9	2	7	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		Select	Any Y	3	28	3	20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Select	Any Y	8	25	5	25	ns
t_{ZH}	Output Enable Time to High Level		Output Control	Any Y	5	20	5	18	ns
t_{ZL}	Output Enable Time to Low Level		Output Control	Any Y	5	21	5	18	ns
t_{HZ}	Output Disable Time from High Level		Output Control	Any Y	2	12	2	10	ns
t_{LZ}	Output Disable Time from Low Level		Output Control	Any Y	3	37	3	18	ns

Note 1: See Section 1 for test waveforms and output load.

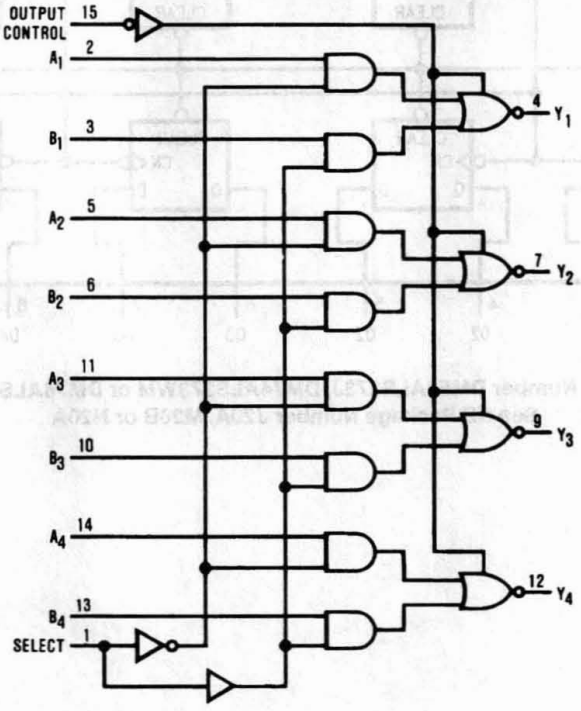
Logic Diagrams

54/74ALS257



TL/F/6227–2

54/74ALS258



TL/F/6227–3

National Semiconductor Corporation

DM54ALS273/DM74ALS273
Octal D-Type Edge-Triggered Flip-Flops with Clear

General Description

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic with a direct clear input.

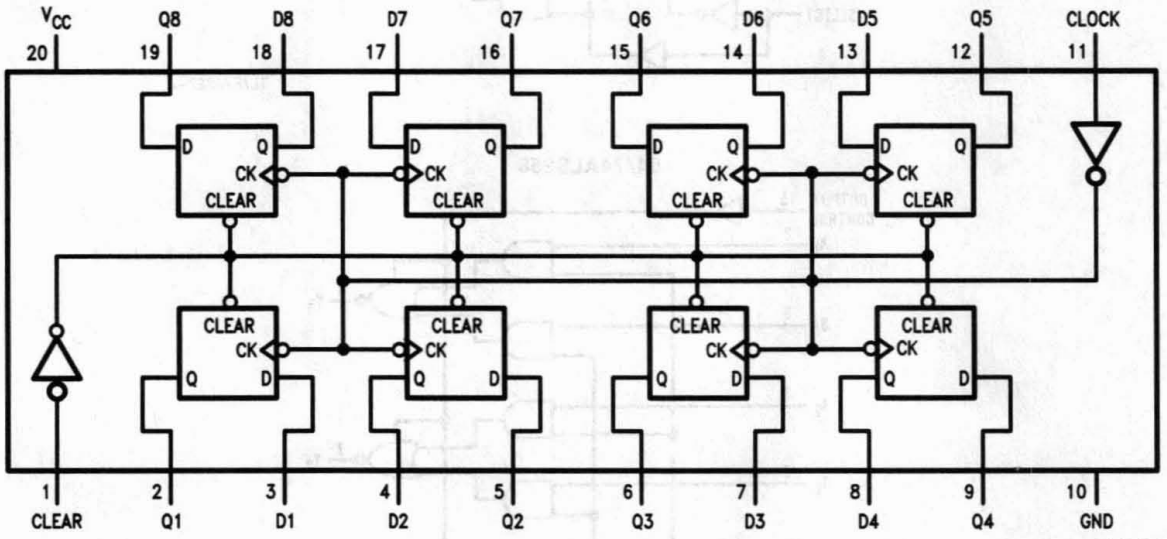
Information at the D inputs meeting the setup requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Buffer-type outputs and improved AC offer significant advantage over 'LS273.
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin-for-pin compatible with 'LS273.

Connection Diagram

Dual-In-Line Package



TL/F/6216–1

Order Number DM54ALS273J, DM74ALS273WM or DM74ALS273N
See NS Package Number J20A, M20B or N20A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54ALS273			DM74ALS273			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−1			−2.6	mA
I_{OL}	Low Level Output Current				12			24	mA
f_{CLK}	Clock Frequency		0		30	0		35	MHz
$t_{W(CLK)}$	Width of Clock Pulse	High	16.5			14			ns
		Low	16.5			14			ns
t_W	Width of Clear Pulse	Low	10			10			ns
t_{SU}	Data Setup Time		10 ↑			10 ↑			ns
		Clear Inactive	15 ↑			15 ↑			
t_H	Data Hold Time		0 ↑			0 ↑			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, V_{IL} = V_{IL} Max	54ALS I_{OH} = −1 mA	2.4	3.2		V
			74ALS I_{OH} = −2.6 mA	2.4	3.3		V
		I_{OH} = −400 μA	54/74ALS	V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, V_{IH} = 2V	54/74ALS I_{OL} = 12 mA		0.25	0.4	V
			74ALS I_{OL} = 24 mA		0.35	0.5	V
I_I	Input Current @ Max. Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V, Outputs Open	Outputs High		11	20	mA
			Outputs Low		19	29	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

Symbol	Parameter	Conditions	From	To	DM54ALS273		DM74ALS273		Units
					Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF			30		35		MHz
t_{PHL}	Propagation Delay Time High to Low Level Output		Clear	Any Q	4	24	4	18	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		Clock	Any Q	2	20	2	12	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Clock	Any Q	3	17	3	15	ns

Note 1: See Section 1 for test waveforms and output load.

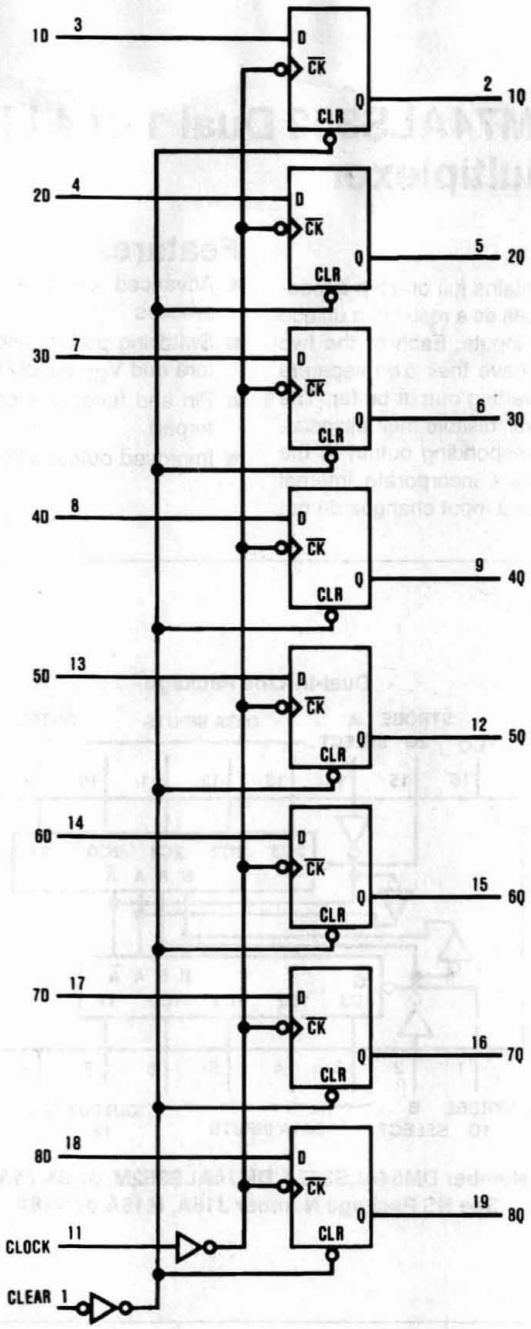
Function Table (Each Flip-Flop)

Inputs			Output
Clear	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

L = Low State, H = High State, X = Don't Care

↑ = Positive Edge Transition, Q_0 = Previous Condition of Q

Logic Diagram



TL/F/6216-2

National Semiconductor Corporation

PRELIMINARY

DM54ALS352/DM74ALS352 Dual 1 of 4 Line Data Selector/Multiplexer

General Description

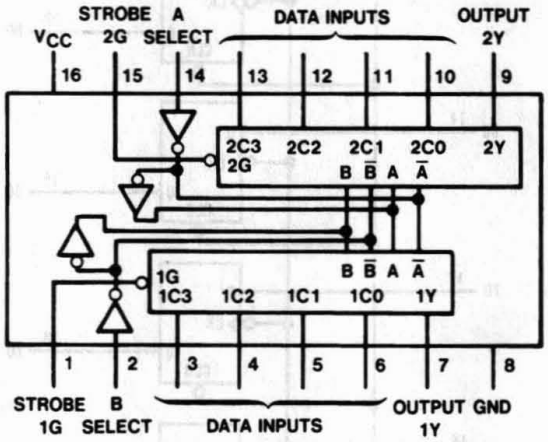
This Data Selector/Multiplexer contains full on-chip decoding to select one-of-four data sources as a result of a unique two-bit binary code at the Select inputs. Each of the two Data Selector/Multiplexer circuits have their own separate Data and Strobe inputs and an inverting output buffer. The Strobe inputs, when at the high level, disable their associated data inputs and force the corresponding output to the high state. The Select input buffers incorporate internal overlap features to ensure that select input changes do not cause invalid output transients.

Features

- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Switching performance is guaranteed over full temperature and V_{CC} supply range
- Pin and functional compatible with the LS family counterpart
- Improved output transient handling capability

Connection Diagram

Dual-In-Line Package



TL/F/6218–1

Order Number DM54ALS352J, DM74ALS352M, or DM74ALS352N
See NS Package Number J16A, M16A or N16A

Function Table

Select Inputs		Data Inputs				Strobe	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	H
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	L	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Select inputs A and B are common to both sections

H = High Level, L = Low Level, X = Don't Care

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS352			DM74ALS352			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, I_{OH} = Max		2.4	3.2		V
		I_{OH} = −400 μA, V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 12 mA		0.25	0.4	V
			74ALS I_{OL} = 24 mA		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IN} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IN} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_{OUT} = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V (Note 1)			6.5	10	mA

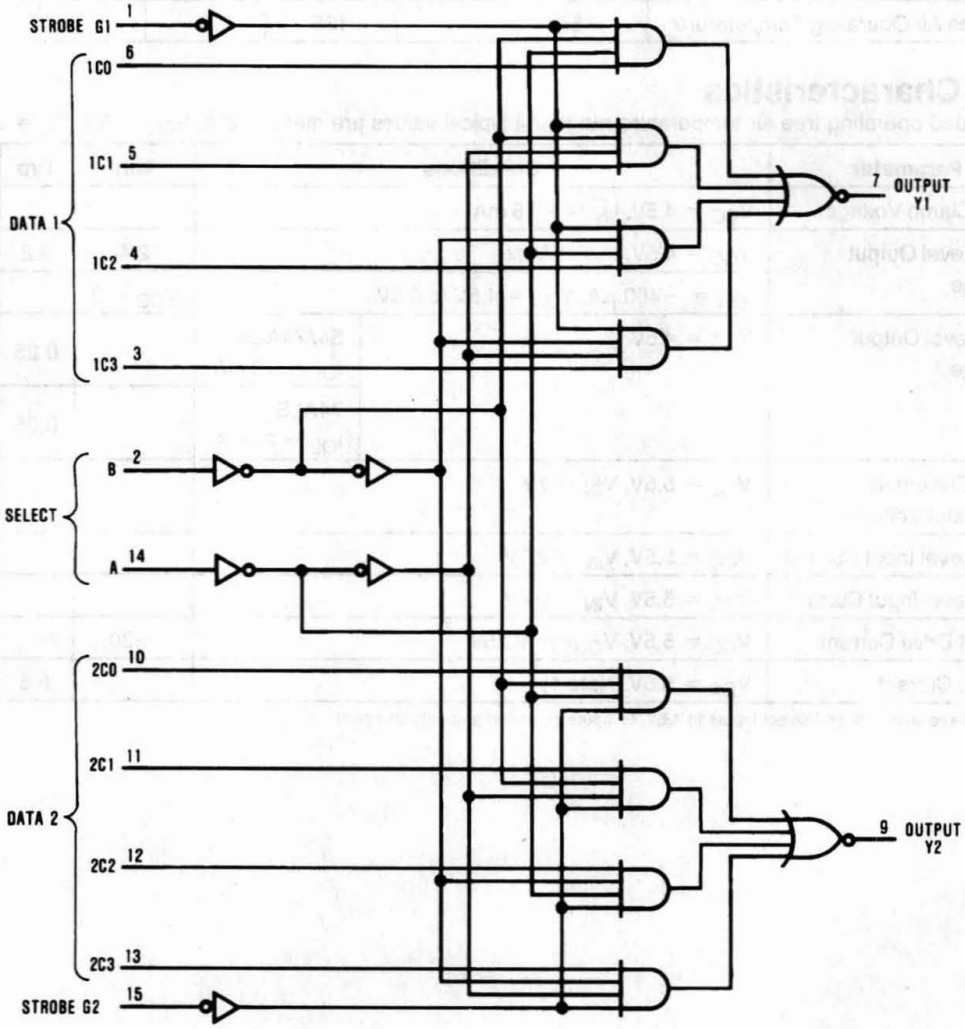
Note 1: I_{CC} is measured with data and select inputs at 4.5V, G inputs grounded and outputs open.

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	From (Input) To (Output)	Conditions	DM54ALS352		DM74ALS352		Units
				Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Y	V_{CC} = 4.5V to 5.5V C_L = 50 pF R_L = 500Ω	5	32	5	24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Y		5	24	5	21	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Y		3	24	3	18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Y		2	15	2	13	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to Y		4	26	4	18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Y		4	24	4	20	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6218–2

National Semiconductor Corporation

DM54ALS353/DM74ALS353 TRI-STATE® Dual 1 of 4 Line Data Selector/Multiplexer

General Description

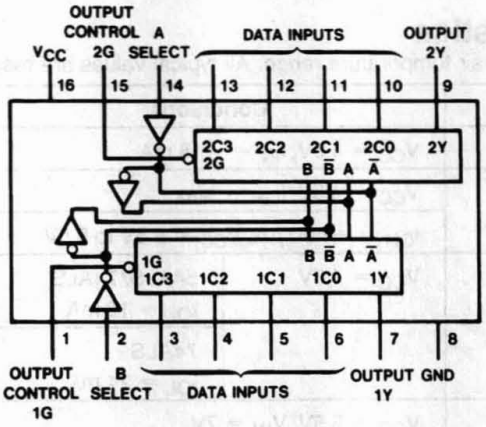
This Data Selector/Multiplexer contains full on-chip decoding to select one-of-four data sources as a result of a unique two-bit binary code at the Select inputs. Each of the two Data Selector/Multiplexer circuits have their own separate Data and Output Control inputs and an inverting TRI-STATE output buffer. The Output Control inputs, when at the high level, place the corresponding output in the high impedance Off state. In order to prevent bus access conflicts, output disable times are shorter than output enable times. The Select input buffers incorporate internal overlap features to ensure that select input changes do not cause invalid output transients.

Features

- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Switching performance is guaranteed over full temperature and V_{CC} supply range
- Pin and functional compatible with LS family counterpart
- Improved output transient handling capability
- Output control circuitry incorporates power-up TRI-STATE feature

Connection Diagram

Dual-In-Line Package



TL/F/6219–1

Order Number DM54ALS353J or DM74ALS353M, N
See NS Package Number J16A, M16A or N16A

Function Table

Select Inputs		Data Inputs				Output Control	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	L	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Address inputs A and B are common to both sections

H = High Level, L = Low Level, X = Don't Care

Z = High Impedance State

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Voltage Applied to Disabled Output	5.5V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS353			DM74ALS353			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

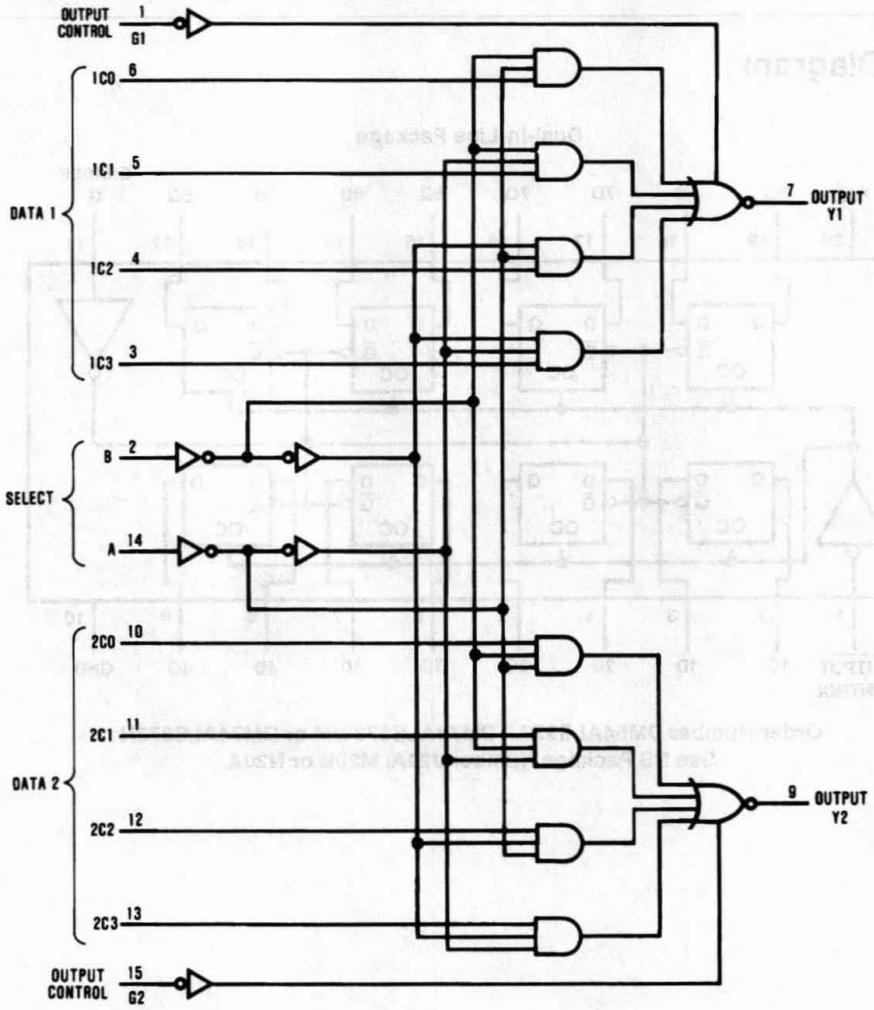
Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, I_{OH} = Max		2.4	3.2		V
		I_{OH} = −400 μA, V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54ALS/74ALS I_{OL} = 12 mA		0.25	0.4	V
			74ALS I_{OL} = 24 mA		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IN} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IN} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_{OUT} = 2.25V		−30		−112	mA
I_{OZH}	Off-State Output Current, High Bias	V_{CC} = 5.5V, V_{OUT} = 2.7V				20	μA
I_{OZH}	Off-State Output Current, Low Bias	V_{CC} = 5.5V, V_{OUT} = 0.4V				−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V	All Inputs at 4.5V		8	13	mA
			All Inputs at GND		7	12	

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	From	To	Conditions	DM54ALS353		DM74ALS353		Units
					Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Select	Y	V_{CC} = 4.5V to 5.5V C_L = 50 pF R_L = 500Ω	5	32	5	24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output				5	24	5	21	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Data			4	24	4	18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output				3	15	3	13	ns
t_{ZH}	Output Enable Time to High Level Output	Output Control			3	18	3	13	ns
t_{ZL}	Output Enable Time to Low Level Output				3	20	2	16	ns
t_{HZ}	Output Disable Time from High Level Output				2	12	2	10	ns
t_{LZ}	Output Disable Time from Low Level Output				2	22	2	14	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6219–2

National Semiconductor Corporation

DM54ALS373/DM74ALS373 Octal D-Type TRI-STATE® Transparent Latches

General Description

These 8-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the ALS373 are transparent D-type latches. While the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was set up.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

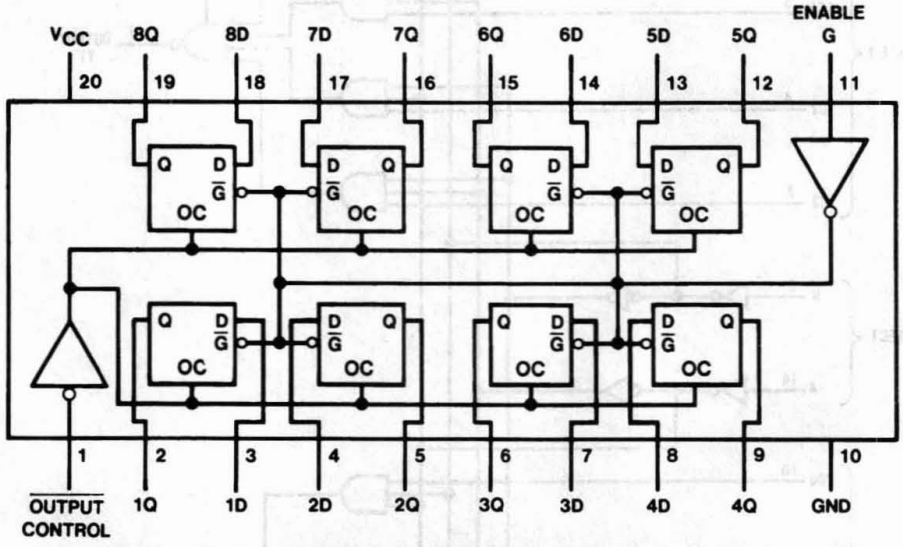
The output control does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with LS TTL counterpart
- Improved AC performance over LS373 at approximately half the power
- TRI-STATE buffer-type outputs drive bus lines directly

Connection Diagram

Dual-In-Line Package



TL/F/6220–1

Order Number DM54ALS373J, DM74ALS373WM or DM74ALS373N
See NS Package Number J20A, M20B or N20A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Voltage Applied to Disabled Output	5.5V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS373			DM74ALS373			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
t_W	Width of Enable Pulse, High or Low	10			10			ns
t_{SU}	Data Setup Time	10↓			10↓			ns
t_H	Data Hold Time	7↓			7↓			ns
T_A	Free Air Operating Temperature	−55		125	0		70	°C

The (↓) arrow indicates the negative edge of the enable is used for reference.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, V_{IL} = V_{IL}Max	54ALS, I_{OH} = −1 mA	2.4	3.2		V
			74ALS, I_{OH} = −2.6 mA	2.4	3.3		V
		V_{CC} = 4.5V to 5.5V, I_{OH} = −400 μA	54/74ALS	V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, V_{IH} = 2V	54/74ALS, I_{OL} = 12 mA		0.25	0.4	V
			74ALS, I_{OL} = 24 mA		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V	54/74ALS, V_O = 2.25V	−30		−112	mA
I_{OZH}	Off-State Output Current High Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V, V_O = 2.7V				20	μA
I_{OZL}	Off-State Output Current Low Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V, V_O = 0.4V				−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V, Outputs Open	Outputs High		9	16	mA
			Outputs Low		16	25	mA
			Outputs Disabled		17	27	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From	To	DM54ALS373		DM74ALS373		Units
					Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	Data	Any Q	2	17	2	12	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Data	Any Q	1	19	4	16	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		Enable	Any Q	6	29	6	22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Enable	Any Q	1	27	7	23	ns
t_{PZH}	Output Enable Time to High Level Output		Output Control	Any Q	3	33	6	18	ns
t_{PZL}	Output Enable Time to Low Level Output		Output Control	Any Q	3	24	5	20	ns
t_{PHZ}	Output Disable Time from High Level Output		Output Control	Any Q	2	24	2	10	ns
t_{PLZ}	Output Disable Time from Low Level Output		Output Control	Any Q	2	16	2	12	ns

Note 1: See Section 1 for test waveforms and output load.

Function Table

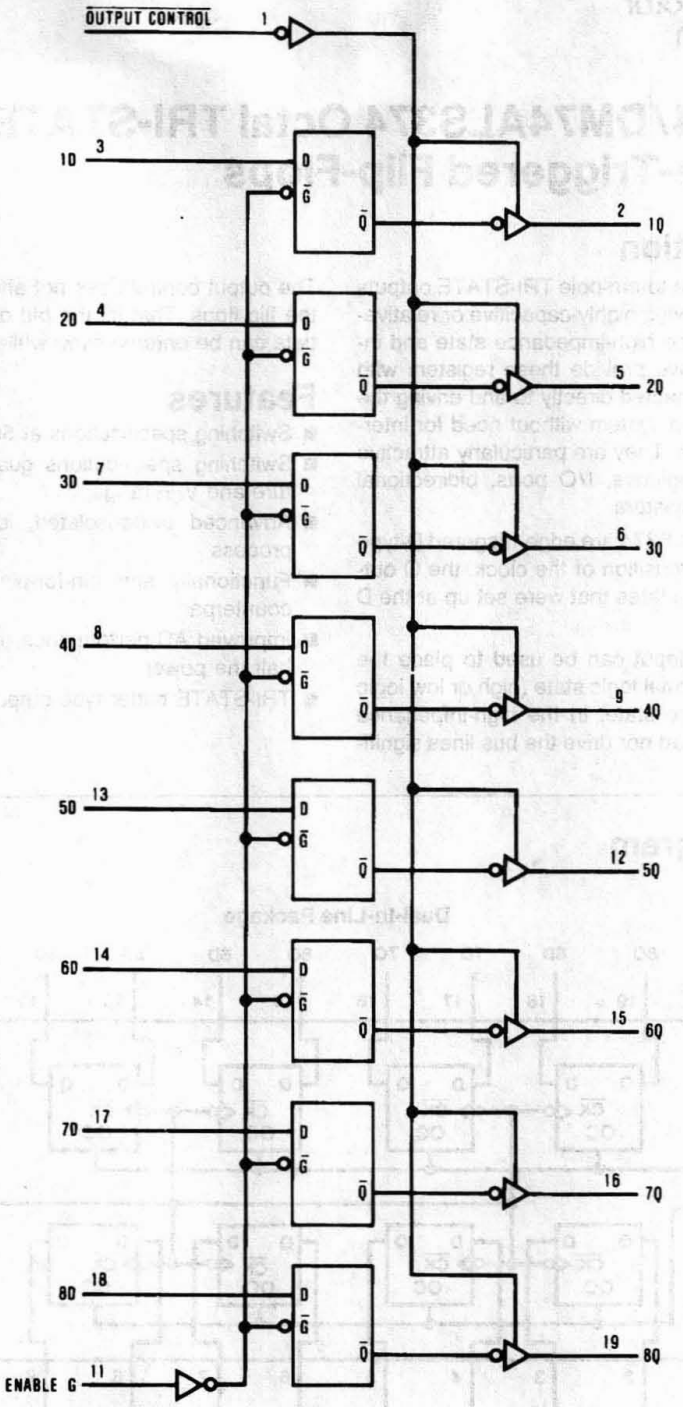
$\overline{\text{Output Control}}$	Enable G	D	Output Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

L = Low State, H = High State, X = Don't Care

Z = High Impedance State

Q_0 = Previous Condition of Q

Logic Diagram



TL/F/6220–2

National Semiconductor Corporation

DM54ALS374/DM74ALS374 Octal TRI-STATE® D-Type-Edge-Triggered Flip-Flops

General Description

These 8-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the ALS374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

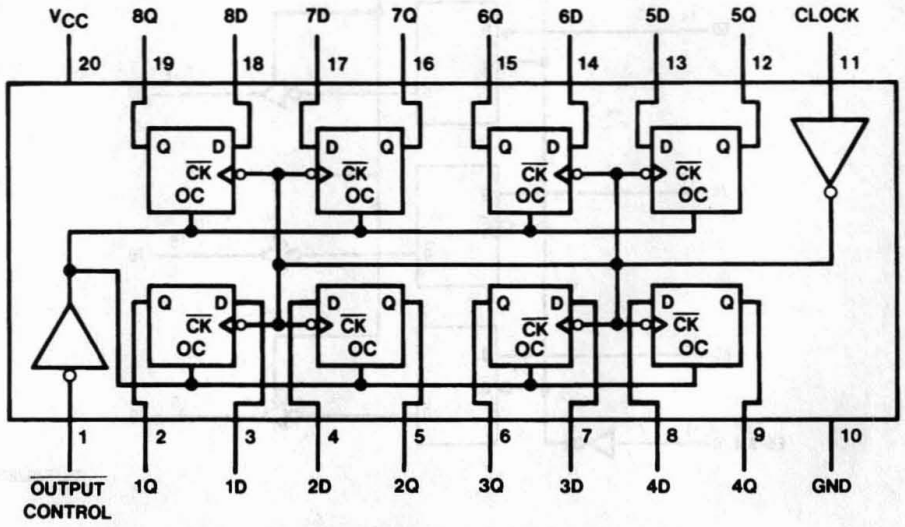
The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin-for-pin compatible with LS TTL counterpart
- Improved AC performance over LS374 at approximately half the power
- TRI-STATE buffer-type outputs drive bus lines directly

Connection Diagram

Dual-In-Line Package



TL/F/6113–1

Order Number DM54ALS374J, DM74ALS374WM or DM74ALS374N
See NS Package Number J20A, M20B or N20A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Voltage Applied to Disabled Output	5.5V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54ALS374			DM74ALS374			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−1			−2.6	mA
I_{OL}	Low Level Output Current				12			24	mA
f_{CLOCK}	Clock Frequency		0		30	0		35	MHz
t_W	Width of Clock Pulse	High	16.5			14			ns
		Low	16.5			14			ns
t_{SU}	Data Setup Time		10 ↑			10 ↑			ns
t_H	Data Hold Time		4 ↑			0 ↑			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V	I_{OH} = Max	2.4	3.2		V
		I_{OH} = −400 μA, V_{CC} = 4.5V to 5.5V	54/74ALS	V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, V_{IH} = 2V	54/74ALS I_{OL} = 12 mA		0.25	0.4	V
			74ALS I_{OL} = 24 mA		0.35	0.5	V
I_I	Input Current @ Max. Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V	54/74ALS V_O = 2.25V	−30		−112	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V, V_O = 2.7V				20	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V, V_O = 0.4V				−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V, Outputs Open	Outputs High		11	19	mA
			Outputs Low		19	28	mA
			Outputs Disabled		20	31	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From	To	DM54ALS374		DM74ALS374		Units
					Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF			30		35		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output		Clock	Any Q	3	21	3	12	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Clock	Any Q	5	19	5	16	ns
t_{PZH}	Output Enable Time to High Level Output		Output Control	Any Q	5	27	5	17	ns
t_{PZL}	Output Enable Time to Low Level Output		Output Control	Any Q	6	23	7	18	ns
t_{PHZ}	Output Disable Time from High Level Output		Output Control	Any Q	2	12	2	10	ns
t_{PLZ}	Output Disable Time from Low Level Output		Output Control	Any Q	3	33	3	18	ns

Note 1: See Section 1 for test waveforms and output load.

Function Table

$\overline{\text{Output Control}}$	Clock	D	Output $\overline{Q}$
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

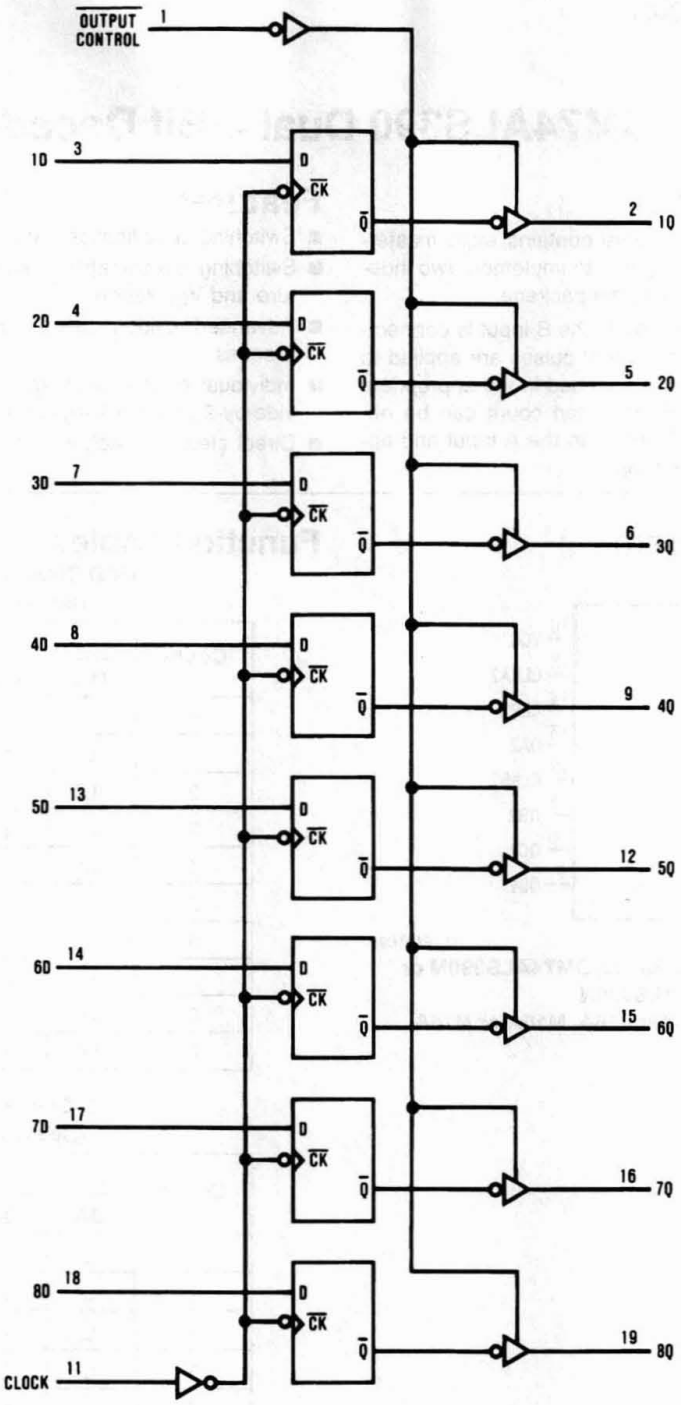
L = Low State, H = High State, X = Don't Care

↑ = Positive Edge Transition

Z = High Impedance State

Q_0 = Previous Condition of Q

Logic Diagram



TL/F/6113–2

2

National Semiconductor Corporation

PRELIMINARY

DM54ALS390/DM74ALS390 Dual 4-Bit Decade Counters

General Description

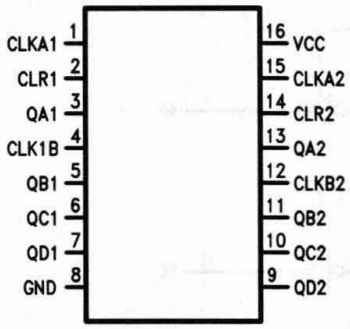
Each of these monolithic counters contains eight master-slave flip-flops and additional gating to implement two independent four bit counters in a single package.

To use their maximum count length, the B input is connected to the QA output. The input count pulses are applied to input A and the outputs are as described in the appropriate truth table. A symmetrical divide-by-ten count can be obtained by connecting the QD output to the A input and applying the input count to the B input.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Individual clocks for A and B flip-flops provide dual divide-by-2 and divide-by-5 counters
- Direct clear for each 4-bit counter

Connection Diagram



TL/F/9169–1

Order Number DM54ALS390J, DM74ALS390M or DM74ALS390N
See NS Package Number J16A, M16A or N16A

Function Tables

BCD Count Sequence (See Note 2)

Count	Output			
	QD	QC	QB	QA
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

Bi-Quinary (5-2) (See Note 3)

Count	Output			
	QA	QD	QC	QB
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

Note 2: Output QA is connected to input B for BCD count

Note 3: Output QD is connected to input A for bi-quinary count

H = High Logic Level, L = Low Logic Level

This document contains information on a product under development. NSC reserves the right to change or discontinue this product without notice.

Absolute Maximum Rating

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54ALS390			DM74ALS390			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{COUNT}	Count Frequency	A Input	0			0			MHz
		B Input	0			0			
t_W	Pulse Width	A Input High							ns
		A Input Low							
		B Input High							
		Clear High							
t_{SU}	Clear Inactive-State Setup Time								ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended free air temperature range

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V, I_{OH} = −0.4 mA		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	
I_I	Input Current at Max, V_I = 7V Input Voltage	V_{CC} = Max, V_I = 7V	Clear			100	µA
			Input A			200	
			Input B			300	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Clear			20	µA
			Input A			40	
			Input B			60	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Clear			−100	µA
			Input A			−200	
			Input B			−300	
I_O	Output Drive Current (B Bus Ports Only)	V_{CC} = Max, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 1)					mA

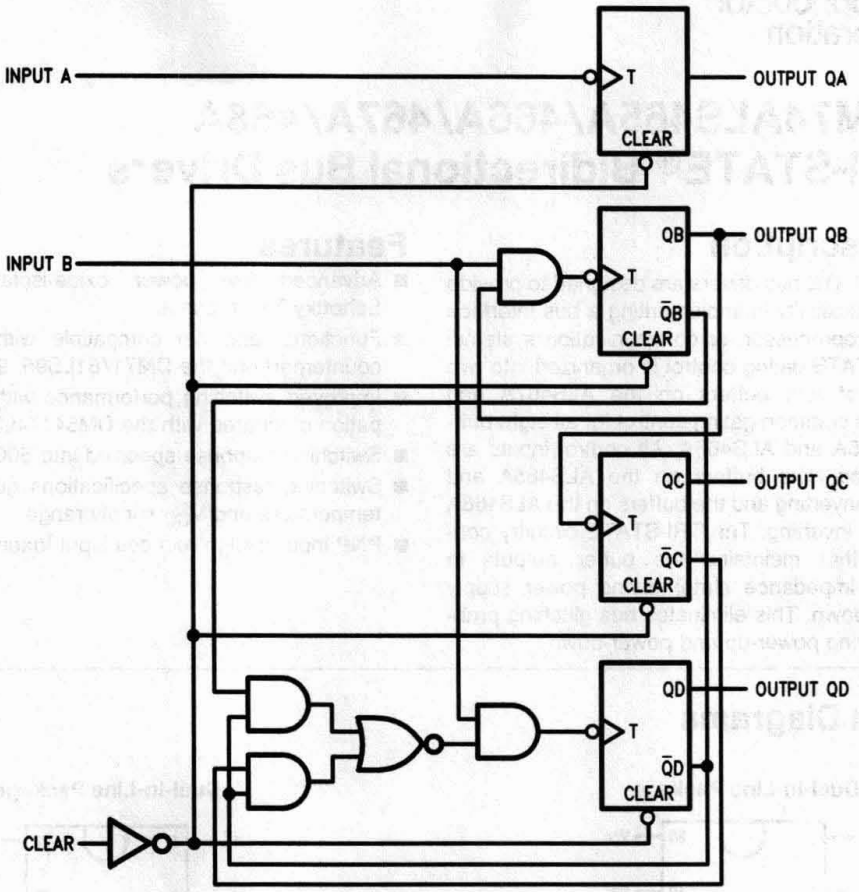
Switching Characteristics over recommended operating free air temperature range

Symbol	Parameter	Conditions	From (Input) To (Output)	DM54ALS390		DM74ALS390		Units
				Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency	V_{CC} = 4.5 to 5.5V, R_L = 500,Ω C_L = 50 pF T_A = Min to Max (Note 2)	A to QA					MHz
			B to QB					
t_{PLH}	Propagation Delay Time Low to High Level Output		A to QA					ns
t_{PHL}	Propagation Delay Time High to Low Level Output		A to QA					ns
t_{PLH}	Propagation Delay Time Low to High Level Output		A to QC					ns
t_{PHL}	Propagation Delay Time High to Low Level Output		A to QC					ns
t_{PLH}	Propagation Delay Time Low to High Level Output		B to QB					ns
t_{PHL}	Propagation Delay Time High to Low Level Output		B to QB					ns
t_{PLH}	Propagation Delay Time Low to High Level Output		B to QC					ns
t_{PHL}	Propagation Delay Time High to Low Level Output		B to QC					ns
t_{PLH}	Propagation Delay Time Low to High Level Output		B to QD					ns
t_{PHL}	Propagation Delay Time High to Low Level Output		B to QD					ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Clear to Any Q					ns

Note 1: I_{CC} is measured with all outputs open, both clear inputs grounded following momentary connection to 4.5V and all other inputs grounded.

Note 2: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/9169–2

National Semiconductor Corporation

DM54/DM74ALS465A/466A/467A/468A Octal TRI-STATE® Bidirectional Bus Drivers

General Description

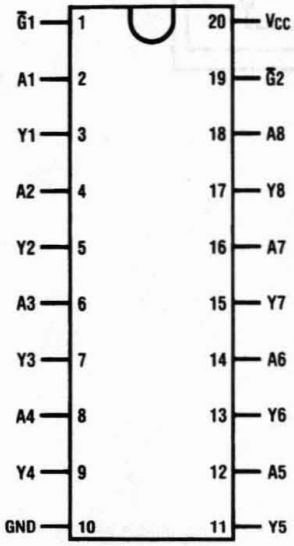
These octal TRI-STATE bus drivers are designed to provide the designer with flexibility in implementing a bus interface with memory, microprocessor, or communication systems. The output TRI-STATE gating control is organized into two separate groups of four buffers on the ALS467A and ALS468A, and one common gating control for all eight buffers on the ALS465A and ALS466A. All control inputs are active low enabling. The buffers on the ALS465A and ALS467A are non-inverting and the buffers on the ALS466A and ALS468A are inverting. The TRI-STATE circuitry contains a feature that maintains the buffer outputs in TRI-STATE (high impedance state) during power supply ramp-up or ramp-down. This eliminates bus glitching problems that arise during power-up and power-down.

Features

- Advanced low power oxide-isolated ion-implanted Schottky TTL process
- Functional and pin compatible with the DM54/74LS counterpart and the DM71/81LS95, 96, 97, 98
- Improved switching performance with less power dissipation compared with the DM54/74LS counterpart
- Switching response specified into 500Ω and 50 pF load
- Switching response specifications guaranteed over full temperature and V_{CC} supply range
- PNP input design reduces input loading

Connection Diagrams

Dual-In-Line Package



TL/F/6221–1

Top View

Order Number DM54ALS465AJ, DM54ALS466AJ, DM74ALS465AWM, DM74ALS466AWM, DM74ALS465AN or DM74ALS466AN
See NS Package Number J20A, M20B or N20A

Dual-In-Line Package

TL/F/6221–2

Top View

Order Number DM54ALS467AJ, DM54ALS468AJ, DM74ALS467AWM, DM74ALS468AWM, DM74ALS467AN or DM74ALS468AN
See NS Package Number J20A, M20B or N20A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V_{CC}	7V
Input Voltage	7V
Output Voltage (Disabled)	5.5V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS465A DM54ALS466A DM54ALS467A DM54ALS468A			DM74ALS465A DM74ALS466A DM74ALS467A DM74ALS468A			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Operating Free Air Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise specified)

Symbol	Parameter	Conditions		DM54ALS465A DM54ALS466A DM54ALS467A DM54ALS468A			DM74ALS465A DM74ALS466A DM74ALS467A DM74ALS468A			Units
				Min	Typ	Max	Min	Typ	Max	
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = 4.5V	I_{OH} = −3 mA	2.4			2.4			V
			I_{OH} = Max	2			2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 54ALS (Max)			0.25	0.4		0.25	0.4	V
		I_{OL} = 74ALS (Max)			—	—		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_I = 7V				0.1			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_I = 2.7V				20			20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1			−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	−30		−112	mA
I_{OZH}	High Level TRI-STATE Output Current	V_{CC} = 5.5V, V_O = 2.7V				20			20	μA
I_{OZL}	Low Level TRI-STATE Output Current	V_{CC} = 5.5V, V_O = 0.4V				−20			−20	μA

Electrical Characteristics (Continued)

over recommended operating free air temperature range (unless otherwise specified)

Symbol	Parameter	Conditions	DM54ALS465A DM54ALS466A DM54ALS467A DM54ALS468A			DM74ALS465A DM74ALS466A DM74ALS467A DM74ALS468A			Units
			Min	Typ	Max	Min	Typ	Max	
I_{CC}	Supply Current	V_{CC} = 5.5V, ALS465A							
		Outputs High		11	21		11	16	mA
		Outputs Low		19	33		19	28	
		Outputs TRI-STATE		23	38		23	33	
		V_{CC} = 5.5V, ALS466A							
		Outputs High		7	15		7	10	mA
		Outputs Low		16	29		16	24	
		Outputs TRI-STATE		19	32		19	27	
		V_{CC} = 5.5V, ALS467A							
		Outputs High		11	21		11	16	mA
		Outputs Low		19	33		19	28	
		Outputs TRI-STATE		23	38		23	33	
		V_{CC} = 5.5V, ALS468A							
		Outputs High		7	15		7	10	mA
		Outputs Low		16	29		16	24	
		Outputs TRI-STATE		19	32		19	27	

'ALS465A and 'ALS467A Switching Characteristics

over recommended operating free air temperature range (Note 1)

Parameter	Conditions	From (Input)	To (Output)	DM54ALS465A DM54ALS467A		DM74ALS465A DM74ALS467A		Units
				Min	Max	Min	Max	
t_{PLH}	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R1 = 500Ω, R2 = 500Ω, T_A = Min to Max	A	Y	2	16	2	13	ns
t_{PHL}				4	15	4	12	ns
t_{PZH}		$\overline{G}$	Any Y	4	27	4	23	ns
t_{PZL}				5	30	5	25	ns
t_{PHZ}		$\overline{G}$	Any Y	2	12	2	10	ns
t_{PLZ}				3	21	3	18	ns

'ALS466A and 'ALS468A Switching Characteristics

over recommended operating free air temperature range (Note 1)

Parameter	Conditions	From (Input)	To (Output)	DM54ALS466A DM54ALS468A		DM74ALS466A DM74ALS468A		Units
				Min	Max	Min	Max	
t_{PLH}	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R1 = 500Ω, R2 = 500Ω, T_A = Min to Max	A	Y	3	14	3	12	ns
t_{PHL}				2	11	2	9	ns
t_{PZH}		$\overline{G}$	Any Y	4	21	4	16	ns
t_{PZL}				7	25	7	23	ns
t_{PHZ}		$\overline{G}$	Any Y	2	12	2	10	ns
t_{PLZ}				2	20	2	17	ns

Note 1: See Section 1 for test waveforms and output loads.

National Semiconductor Corporation

DM54/74ALS518/519/520/521/522 8-Bit Comparators

General Description

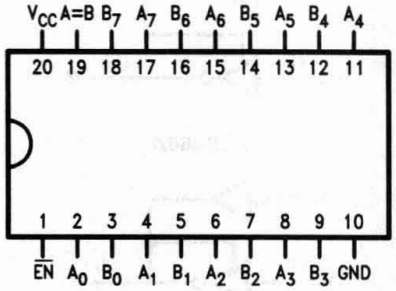
These comparators perform an "equal to" comparison of two eight-bit words with provision for expansion or external enabling. The matching of the two 8-bit input plus a logic LOW on the $\overline{EN}$ input produces the output A = B on the ALS518 and 519 and the output $\overline{A = B}$ on the ALS520, 521 and 522. The ALS520 and 521 have totem pole outputs, while the ALS518, 519 and 522 have open collector outputs for wire AND cascading. Additionally, the ALS518, 520 and 522 are provided with B input pull up termination resistors for analog or switch data.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with LS family counterpart
- Improved output transient handling capability

Connection Diagrams

Dual-In-Line Package



TL/F/6114–1

Order Number DM54ALS518J, DM54ALS519J, DM74ALS518WM, DM74ALS519WM, DM74ALS518N or DM74ALS519N
See NS Package Number J20A, M20B or N20A

Dual-In-Line Package

TL/F/6114–2

Order Number DM54ALS520J, DM54ALS521J, DM54ALS522J, DM74ALS520WM, DM74ALS521WM, DM74ALS522WM, DM74ALS520N, DM74ALS521N or DM74ALS522N
See NS Package Number J20A, M20B or N20A

Function Tables

ALS518, 519

Inputs		Output
$\overline{EN}$	Data	A = B
L	A = B	H
L	A ≠ B	L
H	X	L

H = High Logic Level; L = Low Logic Level; X = Don't Care

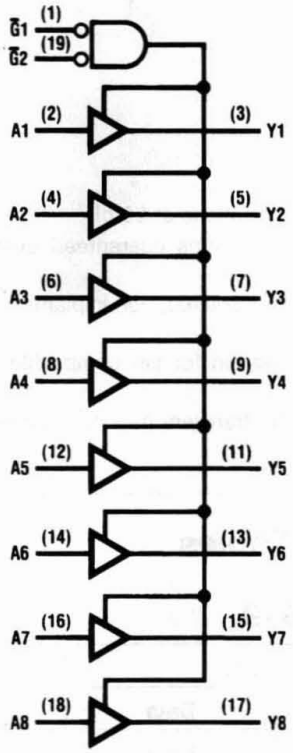
ALS520, 521, 522

Inputs		Output
$\overline{EN}$	Data	$\overline{A = B}$
L	A = B	L
L	A ≠ B	H
H	X	H

H = High Logic Level; L = Low Logic Level; X = Don't Care

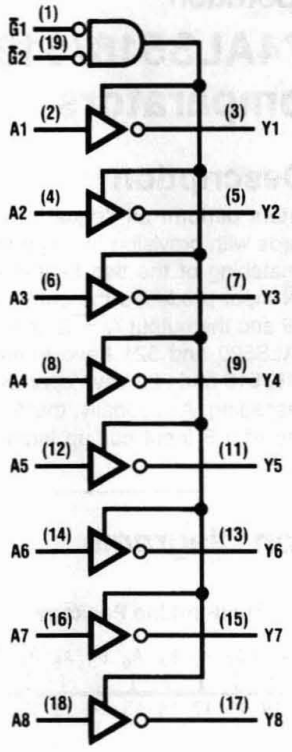
Logic Diagrams

ALS465A



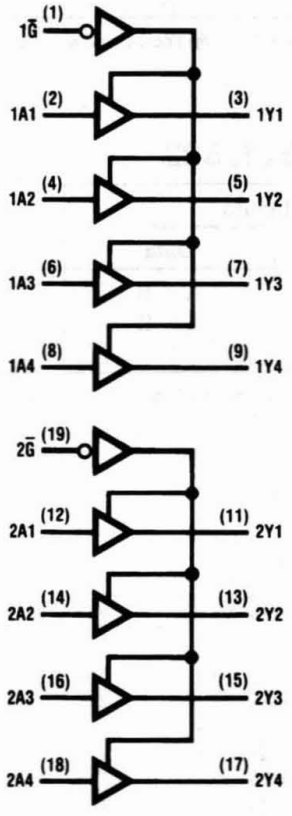
TL/F/6221–3

ALS466A



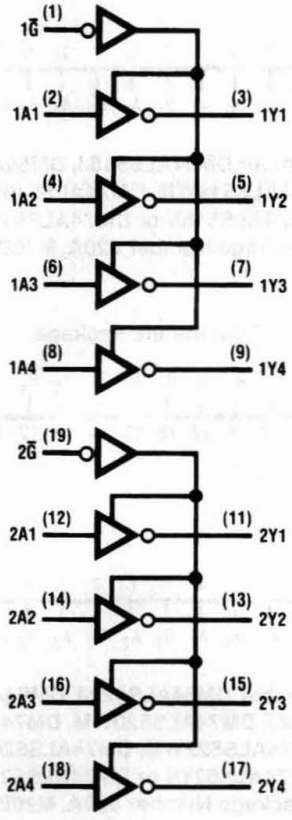
TL/F/6221–4

ALS467A



TL/F/6221–5

ALS468A



TL/F/6221–6

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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS 518, 519, 520, 521, 522			DM74ALS 518, 519, 520, 521, 522			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage (ALS518, 519, 522)			5.5			5.5	V
I_{OH}	High Level Output Current (ALS520, 521)			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V, I_{OH} = −400 μA	ALS520, 521	V_{CC} − 2			V
		V_{CC} = 4.5V, I_{OH} = Max		2.4	3.2		V
I_{OH}	High Level Output Current	V_{CC} = 5.5V, V_{OH} = 5.5V	ALS518, 519, 522			0.1	mA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 12 mA		0.25	0.4	V
			74ALS I_{OL} = 24 mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V	V_{IH} = 5.5V B Input ALS518, 520, 522			0.1	mA
			V_{IH} = 7V, All Others				
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V	All Others			20	μA
			B Input ALS518, 520, 522			−200	
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V	B Input ALS518, 520, 522			−0.6	mA
			All Others			−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V ALS520, 521	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V (Note 1)	ALS518, 519, 522		11	17	mA
			ALS520, 521		12	19	mA

Note 1: I_{CC} is measured with $\overline{G}$ grounded, A and B inputs at 4.5V and outputs open.

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From Input	To Output	DM74ALS 518, 519		DM54ALS 518, 519		Units
					Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V C_L = 50 pF R_L = 667Ω	A or B Data	A = B	15	37	15	33	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		A or B Data	A = B	3	18	3	15	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		$\overline{EN}$	A = B	15	37	15	33	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		$\overline{EN}$	A = B	3	18	3	15	ns

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From Input	To Output	DM54ALS 520, 521		DM74ALS 520, 521		Units
					Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V C_L = 50 pF R_L = 500Ω	A or B Data	$\overline{A = B}$	3	19	30	12	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		A or B Data	$\overline{A = B}$	3	25	50	20	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		$\overline{EN}$	$\overline{A = B}$	2	18	2	12	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		$\overline{EN}$	$\overline{A = B}$	5	23	5	22	ns

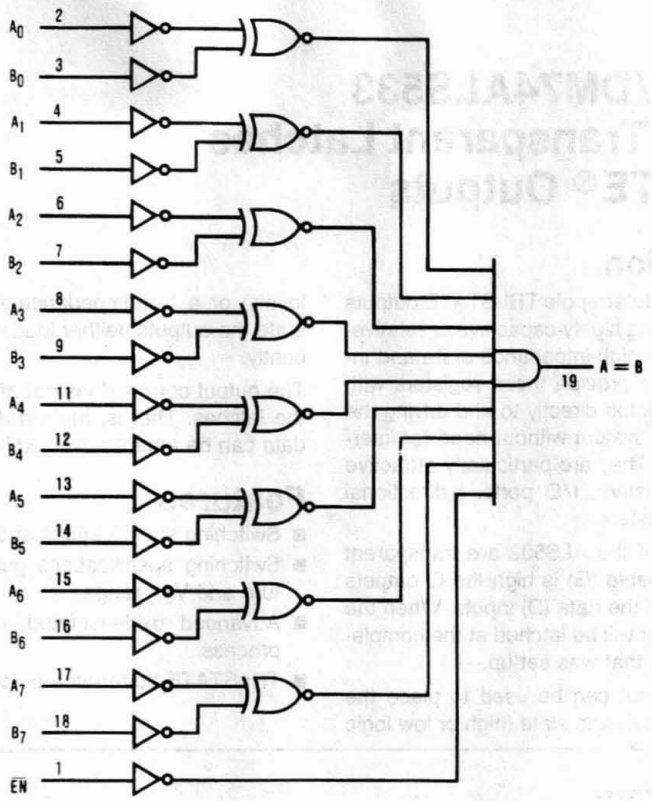
Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From Input	To Output	DM74ALS 522		DM54ALS 522		Units
					Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V C_L = 50 pF R_L = 667Ω	A or B Data	$\overline{A = B}$	10	30	10	25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		A or B Data	$\overline{A = B}$	5	25	5	23	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		$\overline{EN}$	$\overline{A = B}$	8	30	8	25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		$\overline{EN}$	$\overline{A = B}$	8	30	8	23	ns

Note 1: See Section 1 for test waveforms and output load.

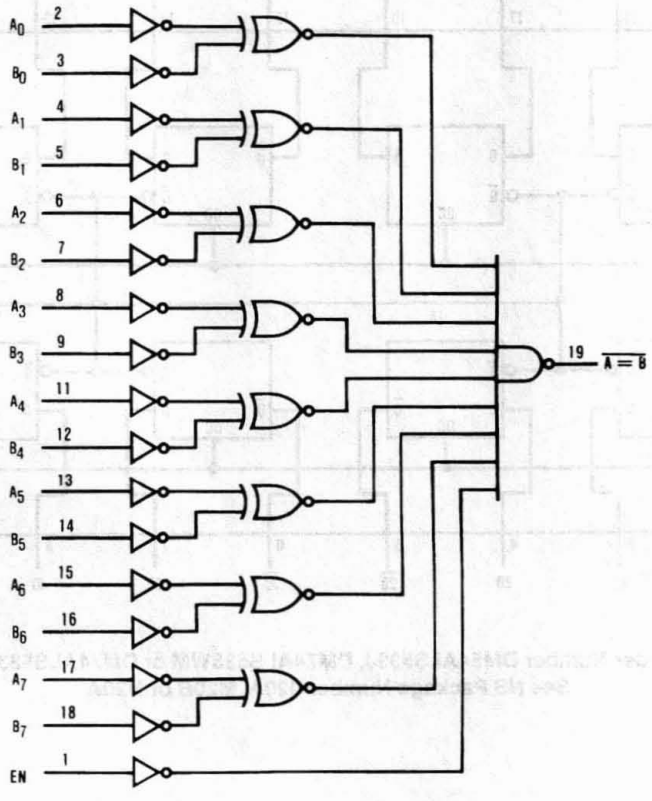
Logic Diagrams

ALS518/519



TL/F/6114–3

ALS520/521/522



TL/F/6114–4

National Semiconductor Corporation

DM54ALS533/DM74ALS533 Octal D-Type Transparent Latches with TRI-STATE® Outputs

General Description

These 8-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight inverting latches of the ALS533 are transparent D-type latches. While the enable (G) is high the Q outputs will follow the complement of the data (D) inputs. When the enable is taken low the output will be latched at the complement of the level of the data that was set up.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

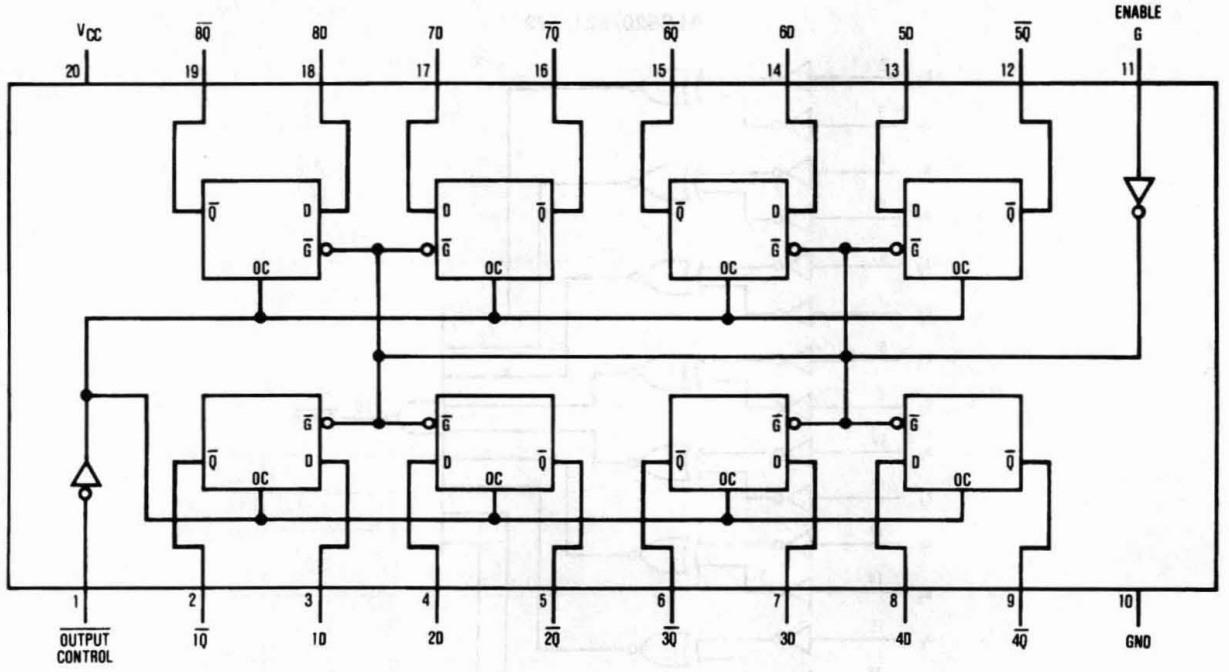
The output control does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- TRI-STATE buffer-type outputs drive bus lines directly

Connection Diagram

Dual-In-Line Package



TL/F/6222–1

Order Number DM54ALS533J, DM74ALS533WM or DM74ALS533N
See NS Package Number J20A, M20B or N20A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Voltage Applied to Disabled Output	5.5V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS533			DM74ALS533			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
t_W	Width of Enable Pulse, High or Low	15			15			ns
t_{SU}	Data Setup Time	15↓			15↓			ns
t_H	Data Hold Time	7↓			7↓			ns
T_A	Free Air Operating Temperature	−55		125	0		70	°C

The (↓) arrow indicates the negative edge of the enable is used for reference.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, V_{IL} = V_{IL} Max	54ALS I_{OH} = −1 mA	2.4	3.2		V
			74ALS I_{OH} = −2.6 mA	2.4	3.3		V
		V_{CC} = 4.5V to 5.5V	54/74ALS I_{OH} = −400 μA	V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, V_{IH} = 2V	54/74ALS I_{OL} = 12 mA		0.25	0.4	V
			74ALS I_{OL} = 24 mA		0.35	0.5	V
I_I	Input Current @ Max. Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V	54/74ALS V_O = 2.25V	−30		−112	mA
I_{OZH}	Off-State Output Current High Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V, V_O = 2.7V				20	μA
I_{OZL}	Off-State Output Current Low Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V, V_O = 0.4V				−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V, Outputs Open	Outputs High		10	17	mA
			Outputs Low		17	26	mA
			Outputs Disabled		18.5	28	mA

2

Switching Characteristics over recommended operating free air temperature range (Note 1).

Symbol	Parameter	Conditions	From	To	DM54ALS534		DM74ALS534		Units
					Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	Data	Any $\overline{Q}$	4	24	4	19	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Data	Any $\overline{Q}$	4	14	4	13	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		Enable	Any $\overline{Q}$	5	28	5	23	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Enable	Any $\overline{Q}$	4	21	4	18	ns
t_{PZH}	Output Enable Time to High Level Output		Output Control	Any $\overline{Q}$	4	19	4	17	ns
t_{PZL}	Output Enable Time to Low Level Output		Output Control	Any $\overline{Q}$	4	20	4	18	ns
t_{PHZ}	Output Disable Time from High Level Output		Output Control	Any $\overline{Q}$	2	12	2	10	ns
t_{PLZ}	Output Disable Time from Low Level Output		Output Control	Any $\overline{Q}$	3	22	3	16	ns

Note 1: See Section 1 for test waveforms and output load.

Function Table

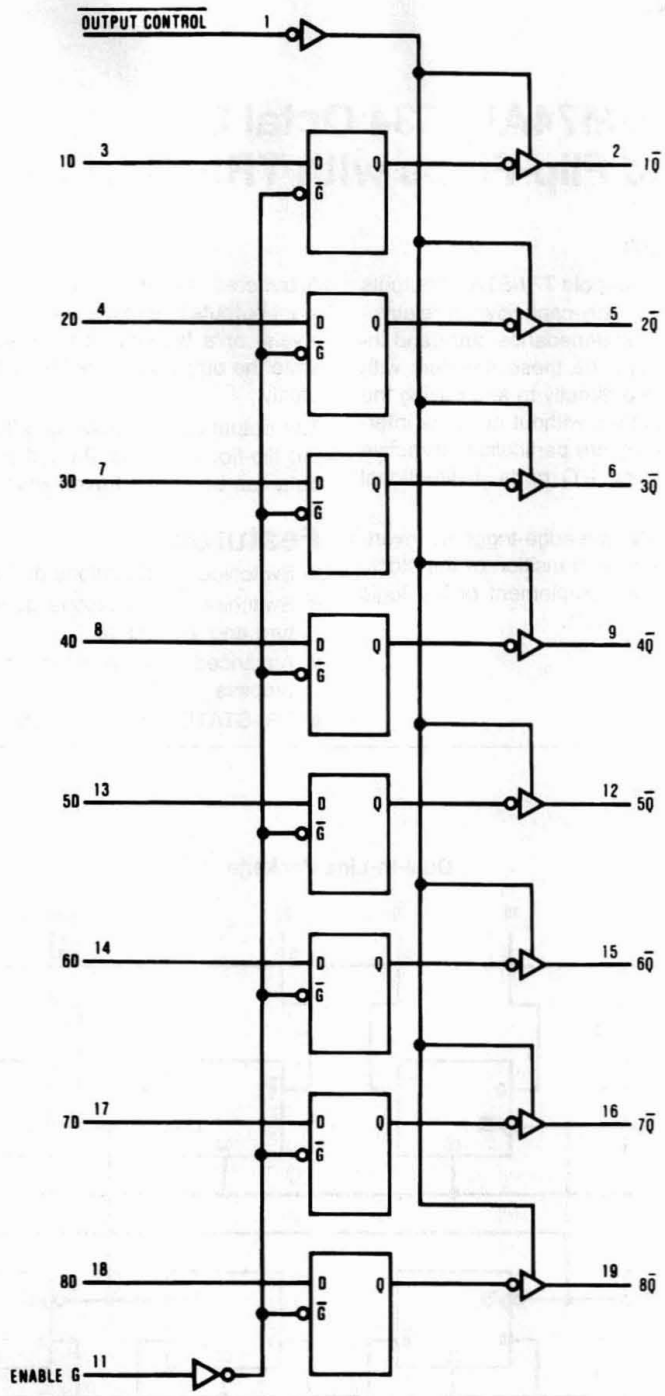
$\overline{\text{Output Control}}$	Enable G	D	Output $\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

L = Low State, H = High State, X = Don't Care

Z = High Impedance State

$\overline{Q}_0$ = Previous Condition of $\overline{Q}$

Logic Diagram



TL/F/6222–2

National Semiconductor Corporation

DM54ALS534/DM74ALS534 Octal D-Type Edge-Triggered Flip-Flops with TRI-STATE® Outputs

General Description

These 8-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the ALS534 are edge-triggered inverting D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the complement of the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

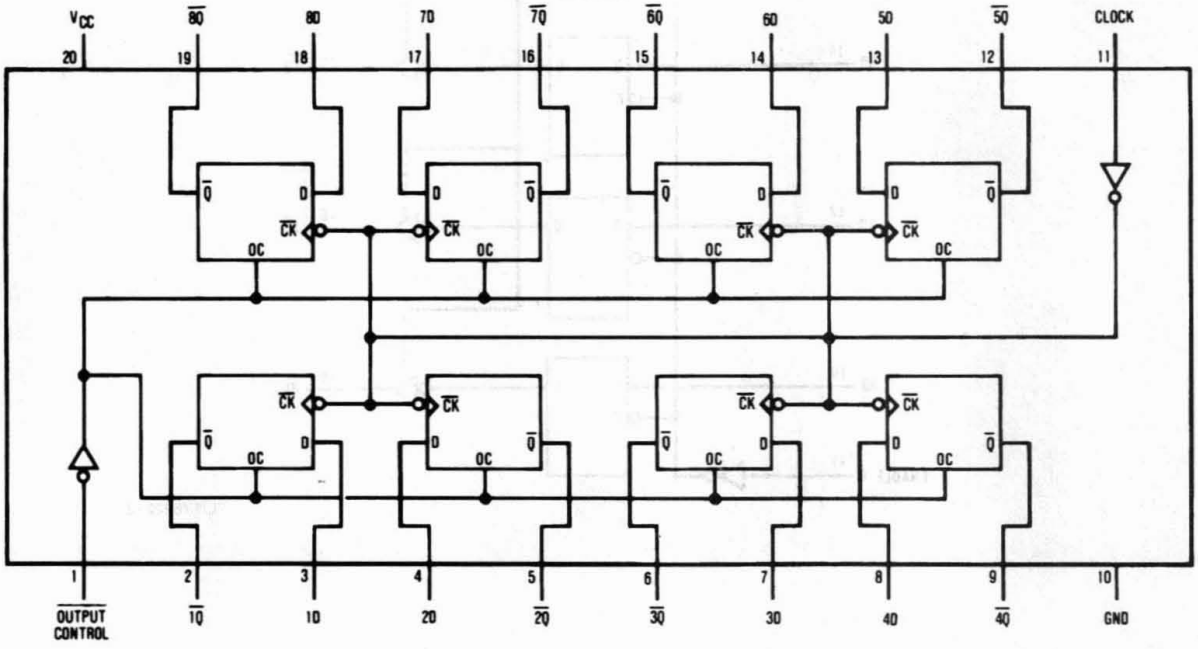
The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- TRI-STATE buffer-type outputs drive bus lines directly

Connection Diagram

Dual-In-Line Package



TL/F/6223–1

Order Number DM54ALS534J, DM74ALS534WM or DM74ALS534N
See NS Package Number J20A, M20B or N20A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Voltage Applied to Disabled Output	5.5V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54ALS534			DM74ALS534			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−1			−2.6	mA
I_{OL}	Low Level Output Current				12			24	mA
f_{CLOCK}	Clock Frequency		0		30	0		35	MHz
t_W	Width of Clock Pulse	High	16.5			14			ns
		Low	16.5			14			ns
t_{SU}	Data Setup Time		10 ↑			10 ↑			ns
t_H	Data Hold Time		0 ↑			0 ↑			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V V_{IL} = V_{IL}Max	I_{OH} = Max	2.4	3.2		V
		V_{CC} = 4.5V to 5.5V I_{OH} = −400 μA	54/74ALS	V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V	54/74ALS I_{OL} = 12 mA		0.25	0.4	V
			74ALS I_{OL} = 24 mA		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V	All Others			−0.2	mA
			CLK, OC			−0.1	
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA

Electrical Characteristics (Continued)

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{OZH}	Off-State Output Current High Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V V_O = 2.7V				20	μA
I_{OZL}	Off-State Output Current Low Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V V_O = 0.4V				−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		11	19	mA
			Outputs Low		19	28	mA
			Outputs Disabled		20	31	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From	To	DM54ALS534		DM74ALS534		Units
					Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF			30		35		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output		Clock	Any $\overline{Q}$	3	15	3	12	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Clock	Any $\overline{Q}$	5	18	5	16	ns
t_{PZH}	Output Enable Time to High Level Output		Output Control	Any $\overline{Q}$	5	19	5	17	ns
t_{PZL}	Output Enable Time to Low Level Output		Output Control	Any $\overline{Q}$	7	20	7	18	ns
t_{PHZ}	Output Disable Time from High Level Output		Output Control	Any $\overline{Q}$	2	12	2	10	ns
t_{PLZ}	Output Disable Time from Low Level Output		Output Control	Any $\overline{Q}$	2	16	2	14	ns

Note 1: See Section 1 for test waveforms and output load.

Function Table

$\overline{\text{Output Control}}$	Clock	D	Output $\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

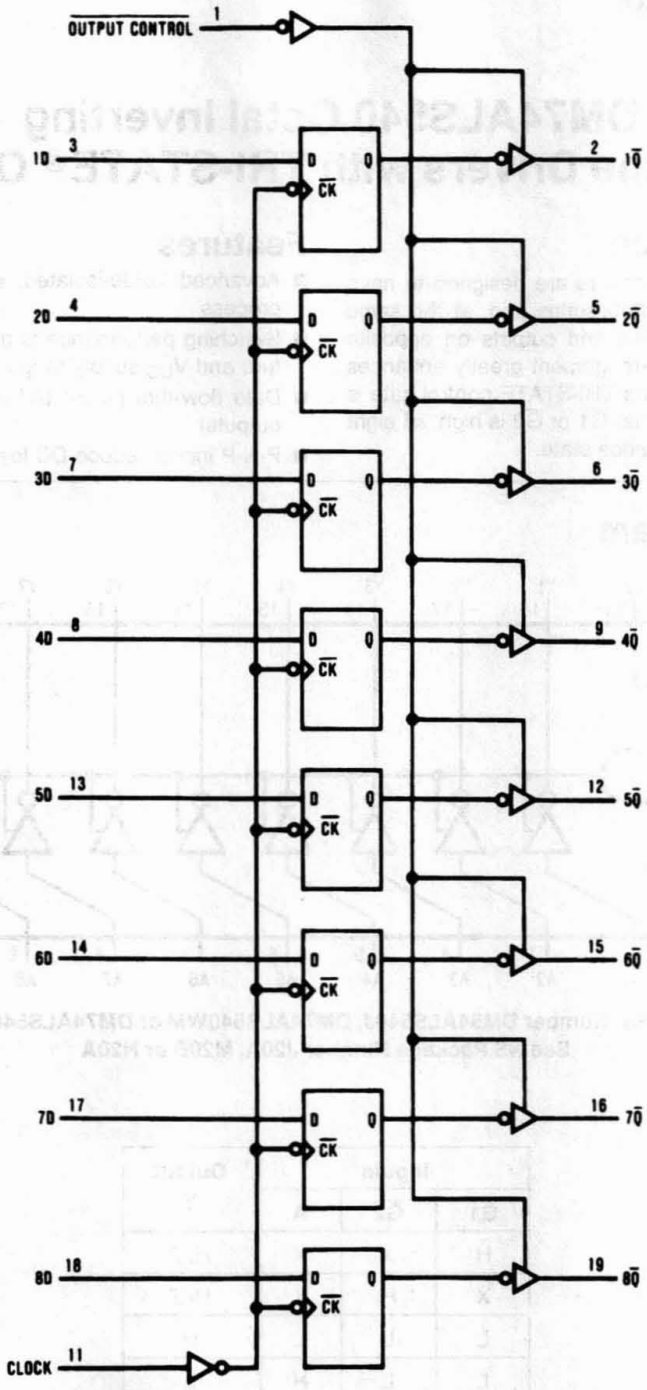
L = Low State, H = High State, X = Don't Care

↑ = Positive Edge Transition

Z = High Impedance State

$\overline{Q}_0$ = Previous Condition of $\overline{Q}$

Logic Diagram



TL/F/6223-2

National Semiconductor Corporation

PRELIMINARY

DM54ALS540/DM74ALS540 Octal Inverting Buffers and Line Drivers with TRI-STATE® Outputs

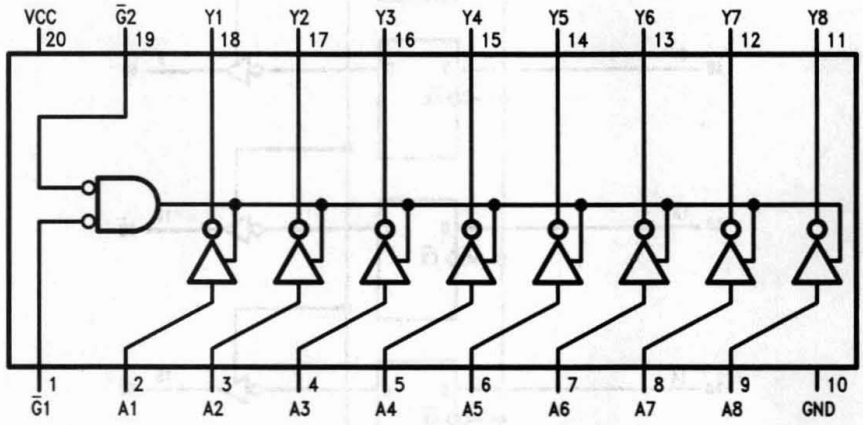
General Description

These octal buffers and line drivers are designed to have the performance of the 'ALS240 series and, at the same time, offer a pinout with inputs and outputs on opposite sides of the package. This arrangement greatly enhances printed circuit board layout. The TRI-STATE control gate is a 2-input NOR such that if either $\overline{G}1$ or $\overline{G}2$ is high, all eight outputs are in the high impedance state.

Features

- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Switching performance is guaranteed over full temperature and V_{CC} supply range
- Data flow-thru pinout (All inputs on opposite side from outputs)
- P-N-P inputs reduce DC loading

Connection Diagram



TL/F/9170–1

Order Number DM54ALS540J, DM74ALS540WM or DM74ALS540N
See NS Package Number J20A, M20B or N20A

Function Table

Inputs			Output
$\overline{G}1$	$\overline{G}2$	A	Y
H	X	X	Hi-Z
X	H	X	Hi-Z
L	L	L	H
L	L	H	L

H = High Logic Level, L = Low Logic Level
X = Don't Care (Either High or Low Logic Level)
Hi-Z = High Impedance (Off) State

This document contains information on a product under development. NSC reserves the right to change or discontinue this product without notice.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Voltage Applied to a Disabled TRI-STATE Output	5.5V
Operating Free-Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS540			DM74ALS540			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended free air temperature range

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V	I_{OH} = −0.4 mA	V_{CC} − 2			V
		V_{CC} = Max	I_{OH} = −3 mA	2.4	3.2		
			I_{OH} = Max	2			
V_{OL}	Low Level Output Voltage	V_{CC} = Min	54/74ALS I_{OL} = 12 mA		0.25	0.4	mA
			74ALS I_{OL} = 24 mA		0.35	0.5	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				100	μA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−100	μA
I_{OZH}	High Level TRI-STATE Output Current	V_{CC} = Max, V_O = 2.7V				20	μA
I_{OZL}	Low Level TRI-STATE Output Current	V_{CC} = Max, V_O = 0.4V				−20	μA
I_O	Output Drive Current	V_{CC} = Max, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = Max	Outputs High		5	10	mA
			Outputs Low		13	22	
			Outputs Disabled		11	19	

Switching Characteristics over recommended free air operating temperature range

Symbol	Parameter	Conditions	From (Input) To (Output)	DM54ALS540		DM74ALS540		Units
				Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V, $R_1 = R_2 = 500\Omega$, C_L = 50 pF (Note 1)	A or B to Y	2	14	2	12	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		A or B to Y	2	11	2	9	ns
t_{PZH}	Output Enable Time to High Level Output		$\overline{G}$ to Y	5	18	5	15	ns
t_{PZL}	Output Enable Time to Low Level Output		$\overline{G}$ to Y	8	24	8	20	ns
t_{PHZ}	Output Disable Time from High Level Output		$\overline{G}$ to Y	1	12	1	10	ns
t_{PLZ}	Output DisableTime from Low Level Output		$\overline{G}$ to Y	2	14	2	12	ns

Note 1: See Section 1 for output load and test waveforms.

National Semiconductor Corporation

PRELIMINARY

DM54ALS541/DM74ALS541
Octal Buffers and Line Drivers with TRI-STATE® Outputs

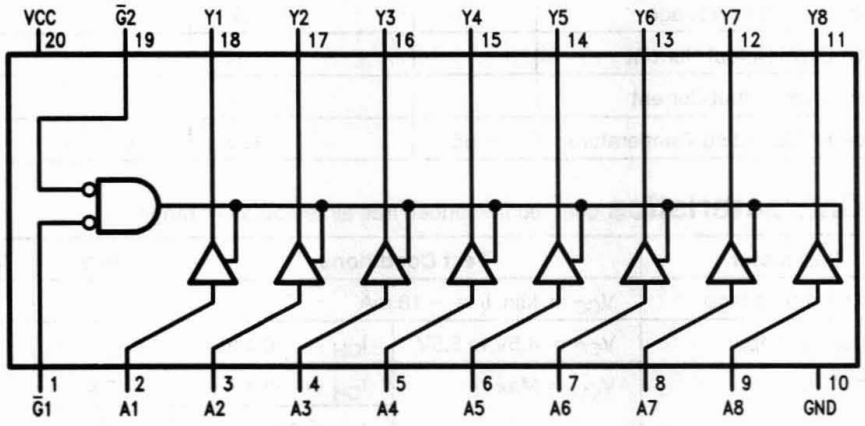
General Description

These octal buffers and line drivers are designed to have the performance of the 'ALS240 series and, at the same time, offer a pinout with inputs and outputs on opposite sides of the package. This arrangement greatly enhances circuit board layout. The TRI-STATE control gate is a 2-input NOR such that if either G1 or G2 is high, all eight outputs are in the high impedance state.

Features

- Advanced oxide-isolated ion-implanted Schottky TTL process
- Switching performance is guaranteed over full temperature and V_{CC} supply range
- Data flow-thru pinout (all inputs on opposite side from outputs)
- P-N-P Inputs reduce DC loading

Connection Diagram



TL/F/9171–1

Order Number DM54ALS541J, DM74ALS451WM or DM74ALS541N
See NS Package Number J20A, M20B or N20A

Function Table

Input			Output
$\overline{G}1$	$\overline{G}2$	A	Y
H	X	X	Hi-Z
X	H	X	Hi-Z
L	L	L	L
L	L	H	H

H = High Logic Level, L = Low Logic Level
X = Don't Care (Either Low or High Logic Level)
Hi-Z = High Impedance (Off) State

2

This document contains information on a product under development. NSC reserves the right to change or discontinue this product without notice.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage: Control Inputs	7V
Voltage Applied to a Disabled TRI-STATE Output	5.5V
Operating Free-Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS541			DM74ALS541			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended free air temperature range

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V	I_{OH} = −0.4 mA	V_{CC} − 2			V
		V_{CC} = Max	I_{OH} = −3 mA	2.4	3.2		
			I_{OH} = Max	2			
V_{OL}	Low Level Output Voltage	V_{CC} = Min	54/74ALS I_{OL} = 12 mA		0.25	0.4	mA
			74ALS I_{OL} = 24 mA		0.35	0.5	
I_I	Input Current at Max Input Voltage	V_{CC} = Max, V_I = 7V				100	μA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V (Note 1)				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V (Note 1)				−100	μA
I_{OZH}	High Level TRI-STATE Output Current	V_{CC} = Max, V_O = 2.7V				20	μA
I_{OZL}	Low Level TRI-STATE Output Current	V_{CC} = Max, V_O = 0.4V				−20	μA
I_O	Output Drive Current	V_{CC} = Max, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = Max	Outputs High		6	14	mA
			Outputs Low		15	25	
			Outputs Disabled		13.5	22	

Switching Characteristics over recommended operating free air temperature range

Symbol	Parameter	Conditions	From (Input) To (Output)	DM54ALS541		DM74ALS541		Units
				Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V, $R_1 = R_2 = 500\Omega$, C_L = 50 pF (Note 1)	A or B to Y	4	17	4	14	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		A or B to Y	2	12	2	10	ns
t_{PZH}	Output Enable Time to High Level Output		$\overline{G}$ to Y	5	18	5	15	ns
t_{PZL}	Output Enable Time to Low Level Output		$\overline{G}$ to Y	8	24	8	20	ns
t_{PHZ}	Output Disable Time from High Level Output		$\overline{G}$ to Y	1	12	1	10	ns
t_{PLZ}	Output DisableTime from Low Level Output		$\overline{G}$ to Y	2	14	2	12	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM54ALS563A/DM74ALS563A Octal D-Type Transparent Latches with TRI-STATE® Outputs

General Description

These 8-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight inverting latches of the ALS563A are transparent D-type latches. While the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the complement of the level of the data that was set up.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

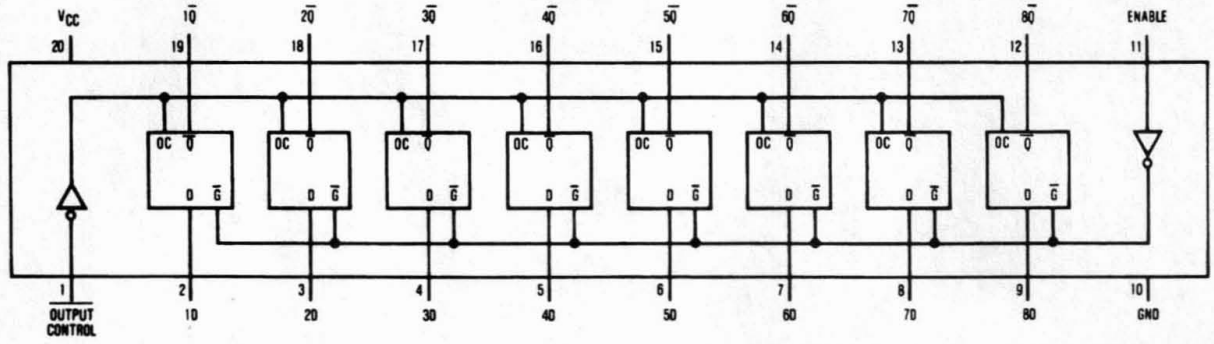
The output control does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- TRI-STATE buffer-type outputs drive bus lines directly

Connection Diagram

Dual-In-Line Package



TL/F/9162–1

Order Number DM54ALS563AJ, DM74ALS563AWM or DM74ALS563AN
See NS Package Number J20A, M20B or N20A

Function Table

$\overline{\text{Output}}$ Control	Enable G	D	Output $\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

L = Low State, H = High State, X = Don't Care

Z = High Impedance State

$\overline{Q}_0$ = Previous Condition of $\overline{Q}$

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Voltage Applied to Disabled Output	5.5V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS563A			DM74ALS563A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
t_W	Width of Enable Pulse, High or Low	15			15			ns
t_{SU}	Data Setup Time	10 ↓			10 ↓			ns
t_H	Data Hold Time	10 ↓			10 ↓			ns
T_A	Free Air Operating Temperature	−55		125	0		70	°C

The (↓) arrow indicates the negative edge of the enable is used for reference.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V V_{IL} = V_{IL} Max	I_{OH} = Max	2.4	3.2		V
		V_{CC} = 4.5V to 5.5V	I_{OH} = −400 μA	V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V	54/74ALS I_{OL} = 12 mA		0.25	0.4	V
			74ALS I_{OL} = 24 mA		0.35	0.5	V
I_I	Input Current @ Max. Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{OZH}	Off-State Output Current High Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V V_O = 2.7V				20	μA
I_{OZL}	Off-State Output Current Low Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V V_O = 0.4V				−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		10	17	mA
			Outputs Low		16	26	mA
			Outputs Disabled		17	29	mA

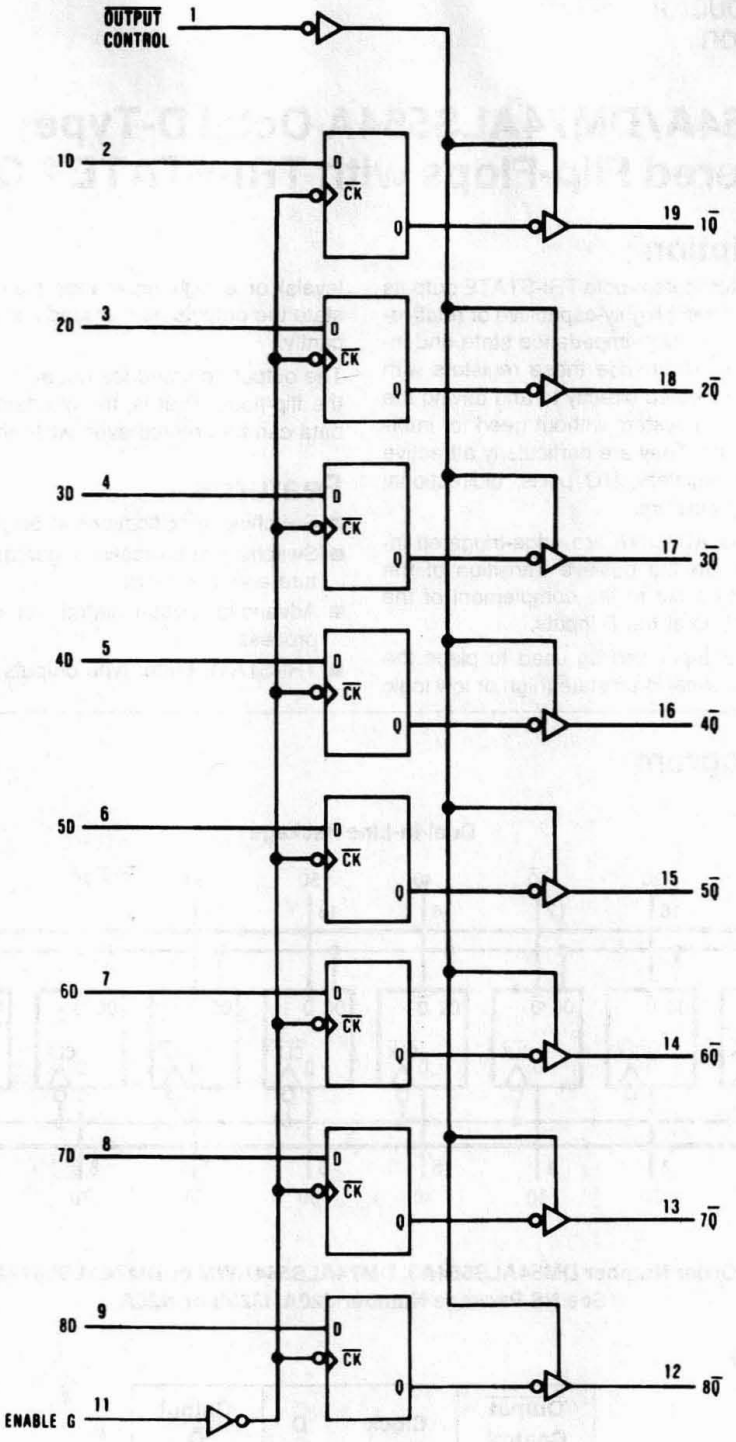
2

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From	To	DM54ALS563A		DM74ALS563A		Units
					Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	Data	Any $\overline{Q}$	3	21	3	18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Data	Any $\overline{Q}$	3	15	3	14	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		Enable	Any $\overline{Q}$	8	29	8	22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Enable	Any $\overline{Q}$	8	22	8	21	ns
t_{PZH}	Output Enable Time to High Level Output		Output Control	Any $\overline{Q}$	4	21	4	18	ns
t_{PZL}	Output Enable Time to Low Level Output		Output Control	Any $\overline{Q}$	4	21	4	18	ns
t_{PHZ}	Output Disable Time from High Level Output		Output Control	Any $\overline{Q}$	2	12	2	10	ns
t_{PLZ}	Output Disable Time from Low Level Output		Output Control	Any $\overline{Q}$	3	18	3	15	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/9162–2

National Semiconductor Corporation

DM54ALS564A/DM74ALS564A Octal D-Type Edge-Triggered Flip-Flops with TRI-STATE® Outputs

General Description

These 8-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the ALS564A are edge-triggered inverting D-type flip-flops. On the positive transition of the clock, the $\overline{Q}$ outputs will be set to the complement of the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

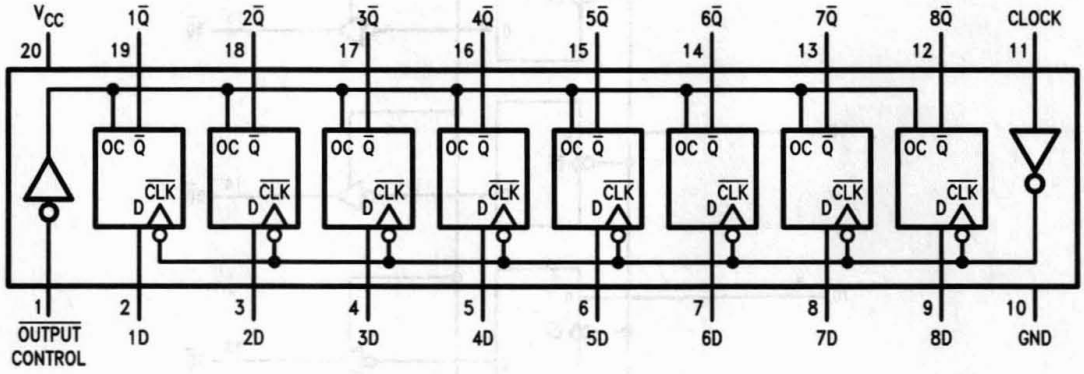
The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- TRI-STATE buffer-type outputs drive bus lines directly

Connection Diagram

Dual-In-Line Package



TL/F/6225–1

Order Number DM54ALS564AJ, DM74ALS564AWM or DM74ALS564AN
See NS Package Number J20A, M20B or N20A

Function Table

$\overline{\text{Output}}$ Control	Clock	D	Output $\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

L = Low State, H = High State, X = Don't Care

↑ = Positive Edge Transition

Z = High Impedance State

$\overline{Q}_0$ = Previous Condition of $\overline{Q}$

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Voltage Applied to Disabled Output	5.5V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54ALS564A			DM74ALS564A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−1			−2.6	mA
I_{OL}	Low Level Output Current				12			24	mA
f_{CLOCK}	Clock Frequency		0		25	0		30	MHz
t_W	Width of Clock Pulse	High	16.5			14			ns
		Low	16.5			14			ns
t_{SU}	Data Setup Time		15 ↑			15 ↑			ns
t_H	Data Hold Time		4 ↑			0 ↑			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V V_{IL} = V_{IL} Max	I_{OH} = Max	2.4	3.2		V
		V_{CC} = 4.5V to 5.5V	I_{OH} = −400 μA	V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V	54/74ALS I_{OL} = 12 mA		0.25	0.4	V
			74ALS I_{OL} = 24 mA		0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{OZH}	Off-State Output Current High Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V V_O = 2.7V				20	μA
I_{OZL}	Off-State Output Current Low Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V V_O = 0.4V				−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		10	18	mA
			Outputs Low		15	24	mA
			Outputs Disabled		16	30	mA

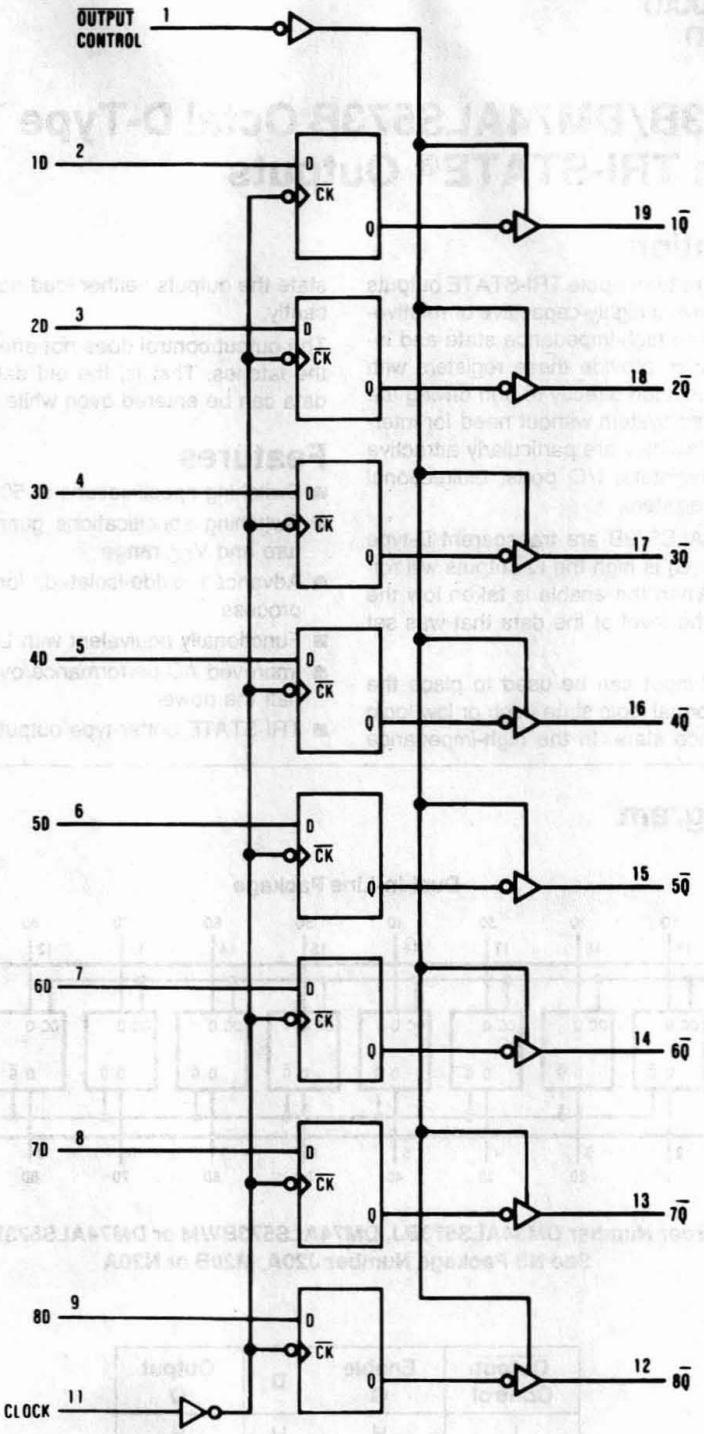
2

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From	To	DM54ALS564A		DM74ALS564A		Units
					Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF			25		30		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output		Clock	Any $\overline{Q}$	4	15	4	14	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Clock	Any $\overline{Q}$	4	15	4	14	ns
t_{PZH}	Output Enable Time to High Level Output		Output Control	Any $\overline{Q}$	4	21	4	18	ns
t_{PZL}	Output Enable Time to Low Level Output		Output Control	Any $\overline{Q}$	4	21	4	18	ns
t_{PHZ}	Output Disable Time from High Level Output		Output Control	Any $\overline{Q}$	2	12	2	10	ns
t_{PLZ}	Output Disable Time from Low Level Output		Output Control	Any $\overline{Q}$	3	17	3	15	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6225–2

National Semiconductor Corporation

DM54ALS573B/DM74ALS573B Octal D-Type Transparent Latches with TRI-STATE® Outputs

General Description

These 8-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the ALS573B are transparent D-type latches. While the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was set up.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

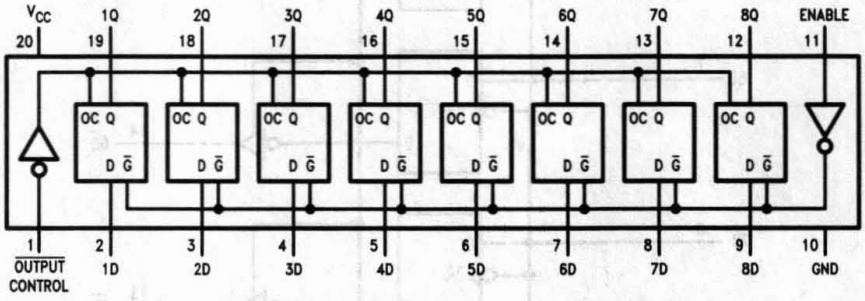
The output control does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally equivalent with LS373
- Improved AC performance over LS373 at approximately half the power
- TRI-STATE buffer-type outputs drive bus lines directly

Connection Diagram

Dual-In-Line Package



TL/F/6226–1

Order Number DM54ALS573BJ, DM74ALS573BWM or DM74ALS573BN
See NS Package Number J20A, M20B or N20A

Function Table

$\overline{\text{Output}}$ Control	Enable G	D	Output Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

L = Low State, H = High State, X = Don't Care

Z = High Impedance State

Q_0 = Previous Condition of Q

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Voltage Applied to Disabled Output	5.5V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS573B			DM74ALS573B			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
t_W	Width of Enable Pulse, High	10			10			ns
t_{SU}	Data Setup Time	10↓			10↓			ns
t_H	Data Hold Time	7↓			7↓			ns
T_A	Free Air Operating Temperature	−55		125	0		70	°C

The (↓) arrow indicates the negative edge of the enable is used for reference.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V V_{IL} = V_{IL} Max	I_{OH} = Max	2.4	3.2		V
		V_{CC} = 4.5V to 5.5V	I_{OH} = −400 μA	V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V	54/74ALS I_{OL} = 12 mA		0.25	0.4	V
			74ALS I_{OL} = 24 mA		0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{OZH}	Off-State Output Current High Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V V_O = 2.7V				20	μA
I_{OZL}	Off-State Output Current Low Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V V_O = 0.4V				−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		10	17	mA
			Outputs Low		15	24	mA
			Outputs Disabled		15.5	27	mA

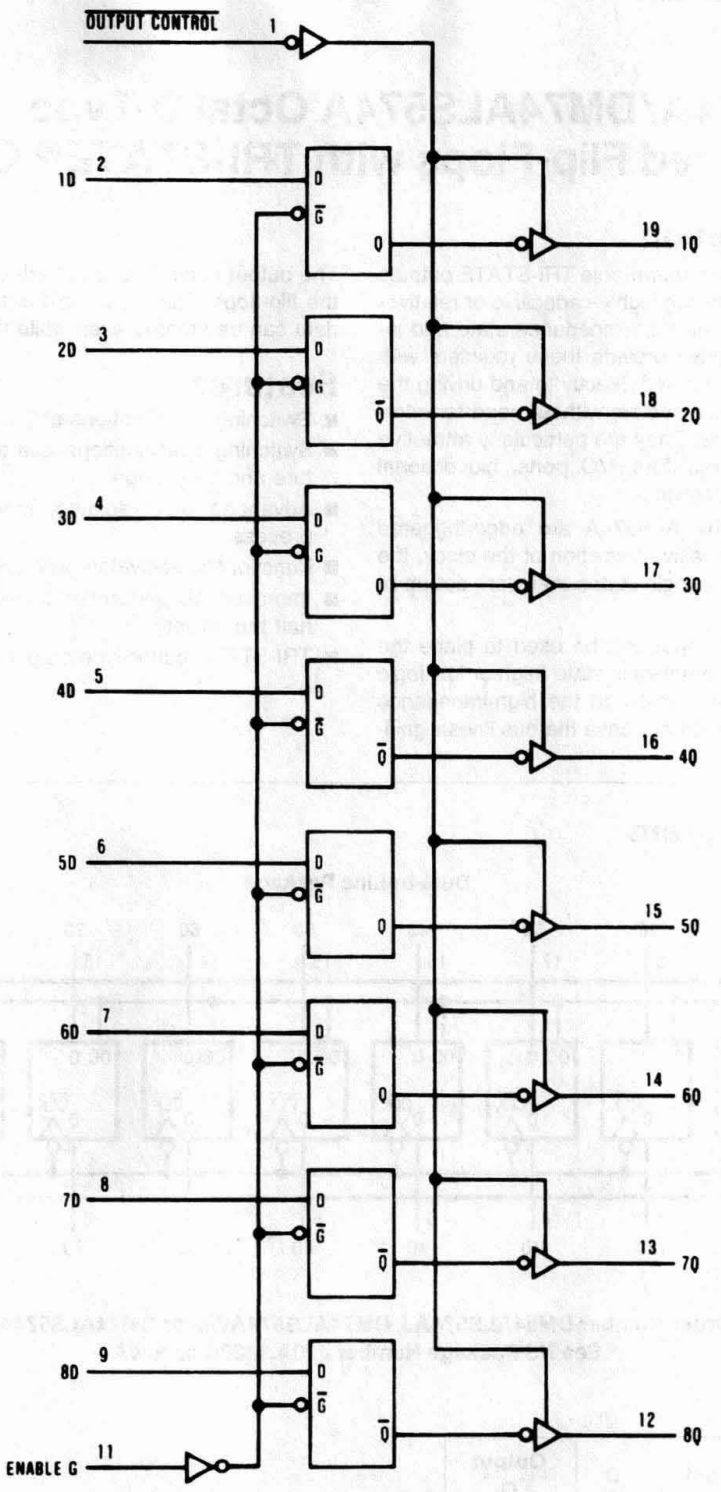
2

Switching Characteristics over recommended operating free air temperature range (Note 1).

Symbol	Parameter	Conditions	From	To	DM54ALS573B		DM74ALS573B		Units
					Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	Data	Any Q	2	15	2	14	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Data	Any Q	2	15	2	14	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		Enable	Any Q	8	25	8	20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Enable	Any Q	8	20	8	19	ns
t_{PZH}	Output Enable Time to High Level Output		Output Control	Any Q	4	21	4	18	ns
t_{PZL}	Output Enable Time to Low Level Output		Output Control	Any Q	4	21	4	18	ns
t_{PHZ}	Output Disable Time from High Level Output		Output Control	Any Q	2	12	2	10	ns
t_{PLZ}	Output Disable Time from Low Level Output		Output Control	Any Q	2	18	2	15	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6226–2

National Semiconductor Corporation

DM54ALS574A/DM74ALS574A Octal D-Type Edge-Triggered Flip-Flops with TRI-STATE® Outputs

General Description

These 8-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the ALS574A are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

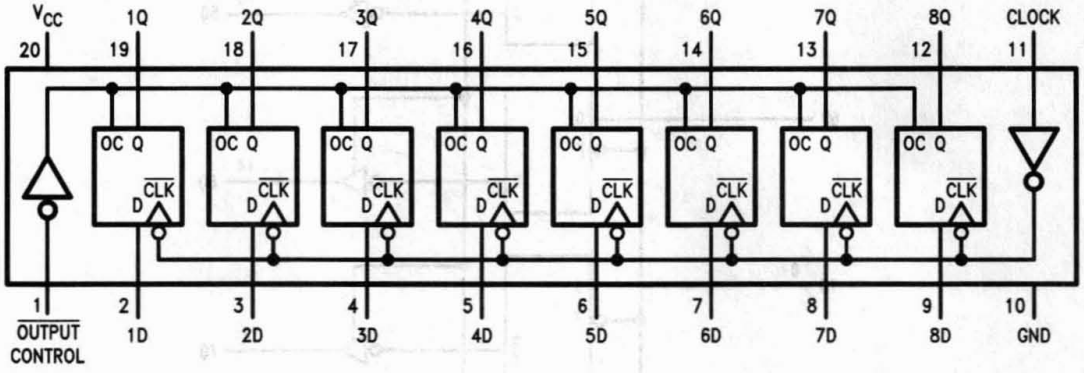
The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally equivalent with LS374
- Improved AC performance over LS374 at approximately half the power
- TRI-STATE buffer-type outputs drive bus lines directly

Connection Diagram

Dual-In-Line Package



TL/F/6110–1

Order Number DM54ALS574AJ, DM74ALS574AWM or DM74ALS574AN
See NS Package Number J20A, M20B or N20A

Function Table

$\overline{\text{Output}}$ Control	Clock	D	Output Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

L = Low State, H = High State, X = Don't Care

↑ = Positive Edge Transition

Z = High Impedance State

Q_0 = Previous Condition of Q

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Voltage Applied to Disabled Output	5.5V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54ALS574A			DM74ALS574A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−1			−2.6	mA
I_{OL}	Low Level Output Current				12			24	mA
f_{CLOCK}	Clock Frequency		0		28	0		35	MHz
t_W	Width of Clock Pulse	High	16.5			14			ns
		Low	16.5			14			ns
t_{SU}	Data Setup Time		15↑			15↑			ns
t_H	Data Hold Time		4↑			0↑			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

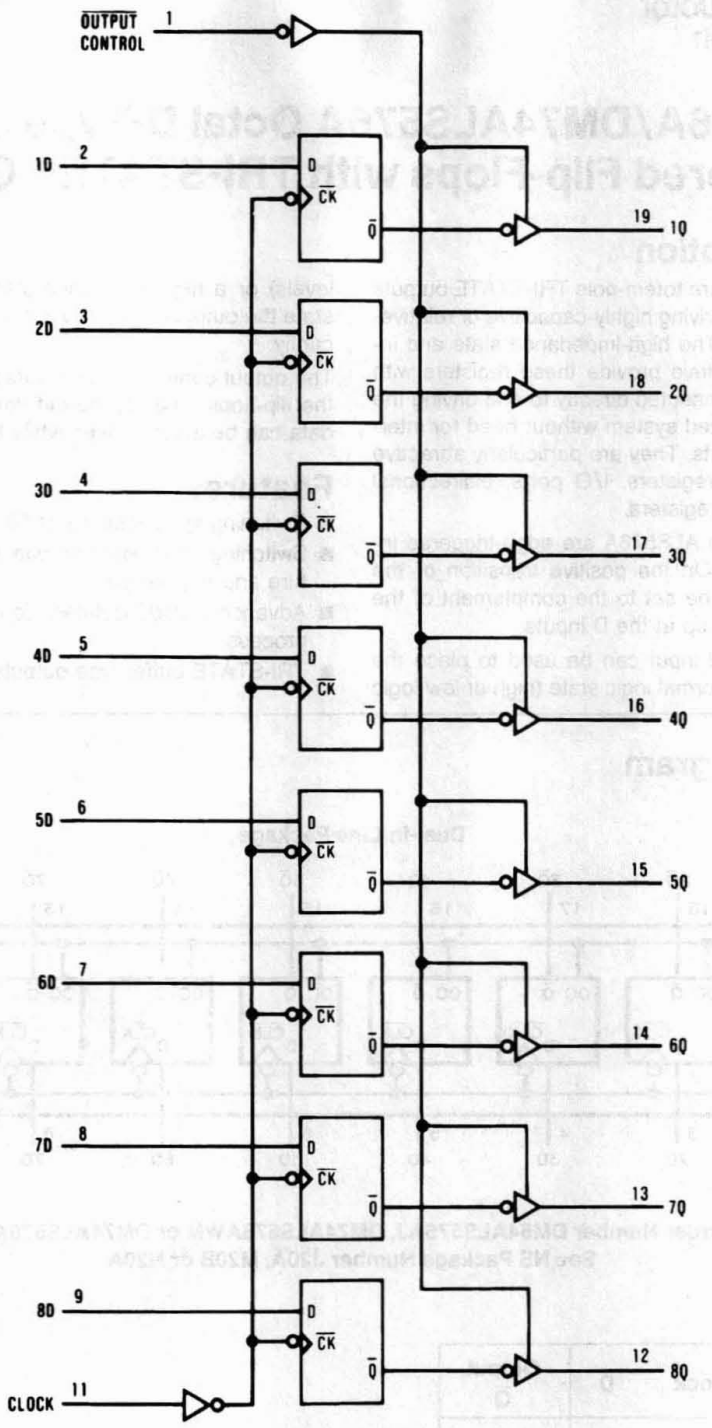
Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, V_{IL} = V_{IL} Max	I_{OH} = Max	2.4	3.2		V
		V_{CC} = 4.5V to 5.5V	I_{OH} = −400 μA	V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, V_{IH} = 2V	54/74ALS I_{OL} = 12 mA		0.25	0.4	V
			74ALS I_{OL} = 24 mA		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{OZH}	Off-State Output Current High Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V, V_O = 2.7V				20	μA
I_{OZL}	Off-State Output Current Low Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V, V_O = 0.4V				−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V, Outputs Open	Outputs High		11	18	mA
			Outputs Low		17	27	mA
			Outputs Disabled		17	28	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From	To	DM54ALS574A		DM74ALS574A		Units
					Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF			28		35		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output		Clock	Any Q	4	22	4	14	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Clock	Any Q	4	17	4	14	ns
t_{PZH}	Output Enable Time to High Level Output		Output Control	Any Q	4	21	4	18	ns
t_{PZL}	Output Enable Time to Low Level Output		Output Control	Any Q	4	26	4	18	ns
t_{PHZ}	Output Disable Time from High Level Output		Output Control	Any Q	2	16	2	10	ns
t_{PLZ}	Output Disable Time from Low Level Output		Output Control	Any Q	2	25	2	12	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6110–2

National Semiconductor Corporation

DM54ALS576A/DM74ALS576A Octal D-Type Edge-Triggered Flip-Flops with TRI-STATE® Outputs

General Description

These 8-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the ALS576A are edge-triggered inverting D-type flip-flops. On the positive transition of the clock, the $\overline{Q}$ outputs will be set to the complement of the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

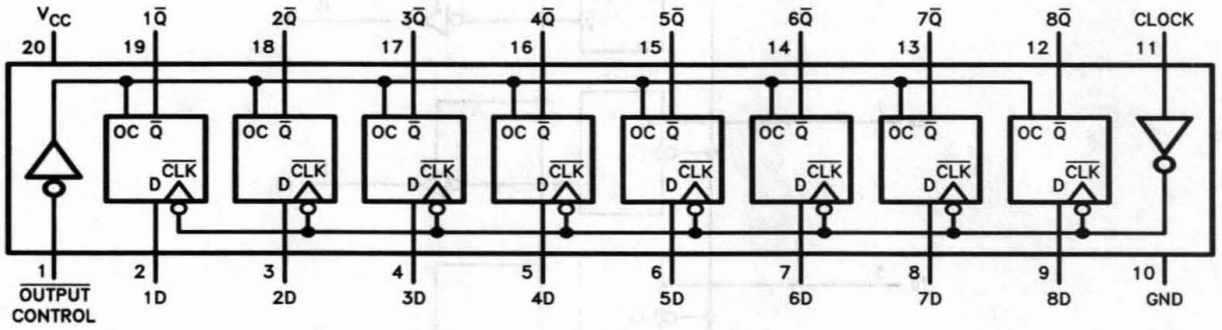
The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- TRI-STATE buffer-type outputs drive bus lines directly

Connection Diagram

Dual-In-Line Package



TL/F/6228–1

Order Number DM54ALS576AJ, DM74ALS576AWM or DM74ALS576AN
See NS Package Number J20A, M20B or N20A

Function Table

$\overline{\text{Output Control}}$	Clock	D	Output $\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

L = Low State, H = High State, X = Don't Care

↑ = Positive Edge Transition

Z = High Impedance State

$\overline{Q}_0$ = Previous Condition of $\overline{Q}$

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Voltage Applied to Disabled Output	5.5V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54ALS576A			DM74ALS576A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−1			−2.6	mA
I_{OL}	Low Level Output Current				12			24	mA
f_{CLOCK}	Clock Frequency		0		25	0		30	MHz
t_W	Width of Clock Pulse	High	20			16.5			ns
		Low	20			16.5			ns
t_{SU}	Data Setup Time		15↑			15↑			ns
t_H	Data Hold Time		4↑			0↑			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, V_{IL} = V_{IL} Max	I_{OH} = Max	2.4	3.2		V
		V_{CC} = 4.5V to 5.5V	I_{OH} = −400 μA	V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, V_{IH} = 2V	54/74ALS I_{OL} = 12 mA		0.25	0.4	V
			74ALS I_{OL} = 24 mA		0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{OZH}	Off-State Output Current High Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V, V_O = 2.7V				20	μA
I_{OZL}	Off-State Output Current Low Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V, V_O = 0.4V				−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V, Outputs Open	Outputs High		10	18	mA
			Outputs Low		15	24	mA
			Outputs Disabled		16	30	mA

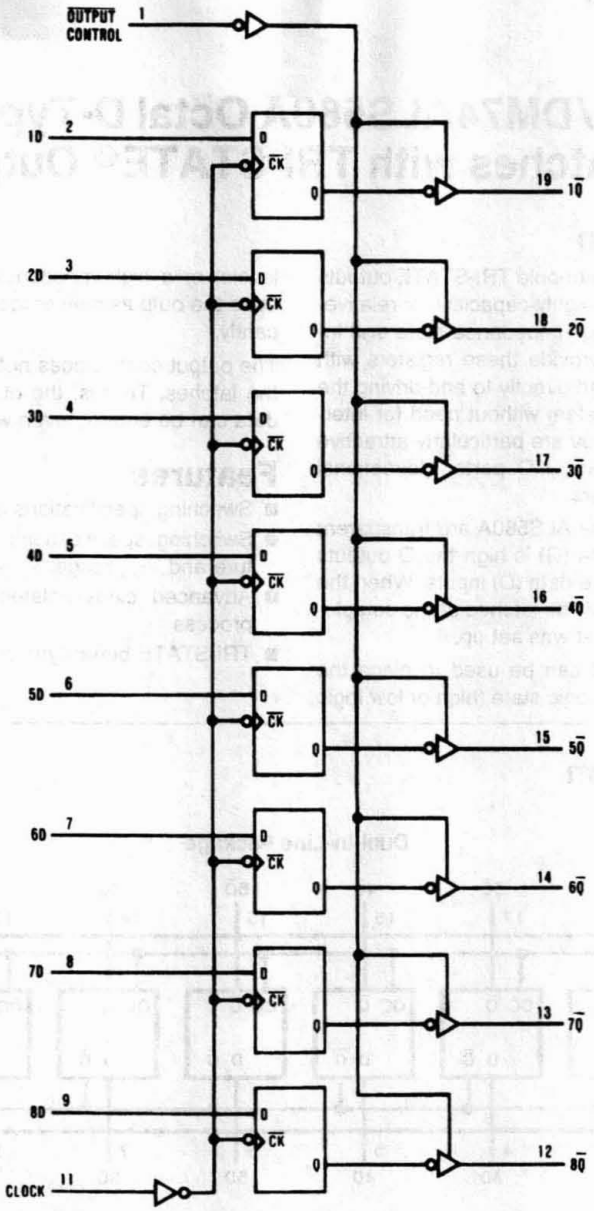
2

Switching Characteristics over recommended operating free air temperature range (Note 1).

Symbol	Parameter	Conditions	From	To	DM54ALS576A		DM74ALS576A		Units
					Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF			25		30		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output		Clock	Any $\overline{Q}$	4	15	4	14	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Clock	Any $\overline{Q}$	4	15	4	14	ns
t_{PZH}	Output Enable Time to High Level Output		Output Control	Any $\overline{Q}$	4	21	4	18	ns
t_{PZL}	Output Enable Time to Low Level Output		Output Control	Any $\overline{Q}$	4	21	4	18	ns
t_{PHZ}	Output Disable Time from High Level Output		Output Control	Any $\overline{Q}$	2	12	2	10	ns
t_{PLZ}	Output Disable Time from Low Level Output		Output Control	Any $\overline{Q}$	3	17	3	15	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6228–2

National Semiconductor Corporation

DM54ALS580A/DM74ALS580A Octal D-Type Transparent Latches with TRI-STATE® Outputs

General Description

These 8-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight inverting latches of the ALS580A are transparent D-type latches. While the enable (G) is high the Q outputs will follow the complement of the data (D) inputs. When the enable is taken low the output will be latched at the complement of the level of the data that was set up.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

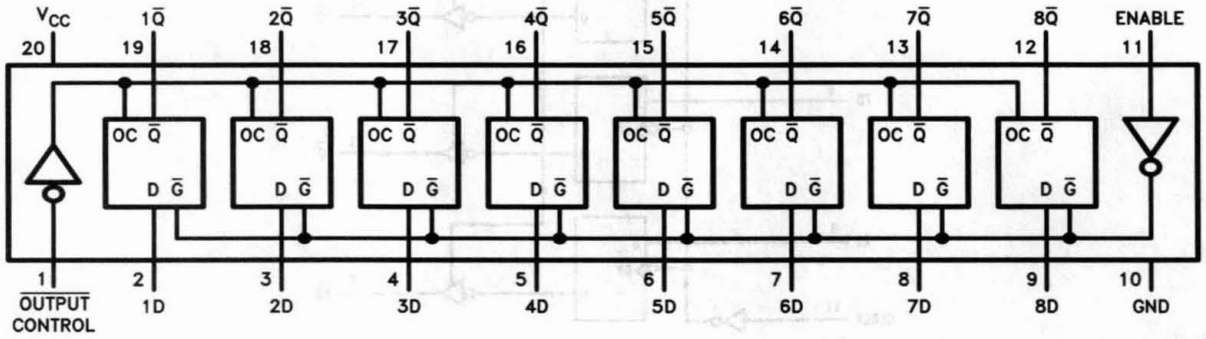
The output control does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- TRI-STATE buffer-type outputs drive bus lines directly

Connection Diagram

Dual-In-Line Package



TL/F/6229–1

Order Number DM54ALS580AJ, DM74ALS580AWM or DM74ALS580AN
See NS Package Number J20A, M20B or N20A

Function Table

$\overline{\text{Output}}$ Control	Enable G	D	Output $\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

L = Low State, H = High State, X = Don't Care

Z = High Impedance State

$\overline{Q}_0$ = Previous Condition of $\overline{Q}$

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Voltage Applied to Disabled Output	5.5V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS580A			DM74ALS580A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
t_W	Width of Enable Pulse, High or Low	15			15			ns
t_{SU}	Data Setup Time	10 ↓			10 ↓			ns
t_H	Data Hold Time	10 ↓			10 ↓			ns
T_A	Free Air Operating Temperature	−55		125	0		70	°C

The (↓) arrow indicates the negative edge of the enable is used for reference.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

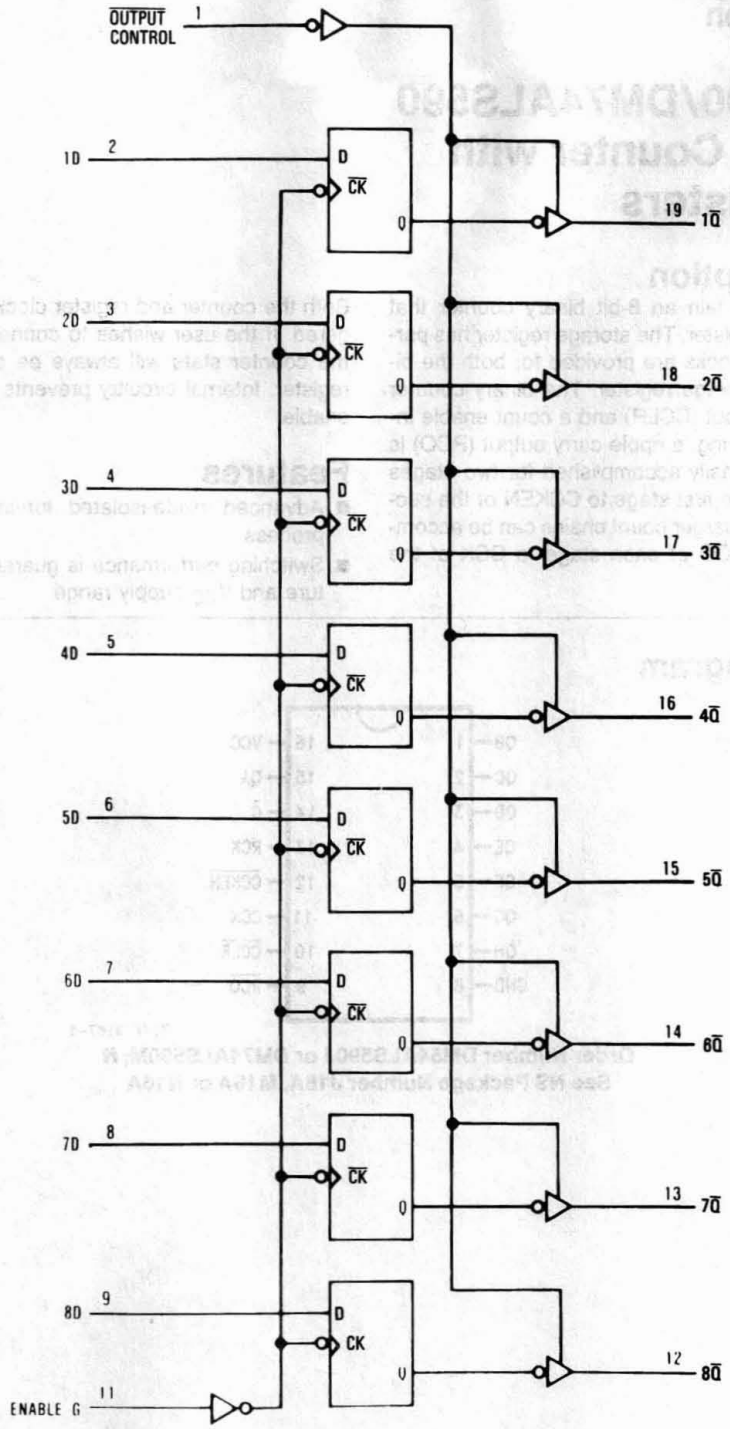
Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V V_{IL} = V_{IL} Max	I_{OH} = Max	2.4	3.2		V
		V_{CC} = 4.5V to 5.5V	I_{OH} = −400 μA	V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V	54/74ALS I_{OL} = 12 mA		0.25	0.4	V
			74ALS I_{OL} = 24 mA		0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{OZH}	Off-State Output Current High Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V V_O = 2.7V				20	μA
I_{OZL}	Off-State Output Current Low Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V V_O = 0.4V				−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		10	17	mA
			Outputs Low		16	26	mA
			Outputs Disabled		17	29	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From	To	DM54ALS580A		DM74ALS580A		Units
					Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	Data	Any $\overline{Q}$	3	21	3	18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Data	Any $\overline{Q}$	3	15	3	14	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		Enable	Any $\overline{Q}$	8	29	8	22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Enable	Any $\overline{Q}$	8	22	8	21	ns
t_{PZH}	Output Enable Time to High Level Output		Output Control	Any $\overline{Q}$	4	21	4	18	ns
t_{PZL}	Output Enable Time to Low Level Output		Output Control	Any $\overline{Q}$	4	21	4	18	ns
t_{PHZ}	Output Disable Time from High Level Output		Output Control	Any $\overline{Q}$	2	12	2	10	ns
t_{PLZ}	Output Disable Time from Low Level Output		Output Control	Any $\overline{Q}$	3	18	3	15	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6229–2

National Semiconductor Corporation

PRELIMINARY

DM54ALS590/DM74ALS590 8-Bit Binary Counter with Output Registers

General Description

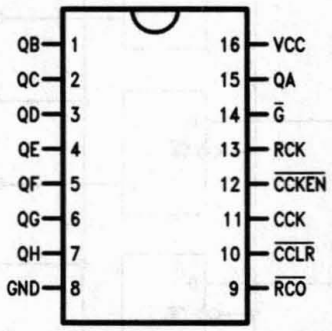
These devices each contain an 8-bit binary counter that feeds an 8-bit storage register. The storage register has parallel outputs. Separate clocks are provided for both the binary counter and the storage register. The binary counter features a direct clear input (CCLR) and a count enable input (CCKEN). For cascading, a ripple carry output (RCO) is provided. Expansion is easily accomplished for two stages by connecting RCO of the first stage to CCKEN of the second stage. Cascading for larger count chains can be accomplished by connecting RCO of each stage to CCK of the following stage.

Both the counter and register clocks are positive edge triggered. If the user wishes to connect both clocks together, the counter state will always be one count ahead of the register. Internal circuitry prevents clocking from the clock enable.

Features

- Advanced oxide-isolated ion-implanted Schottky TTL process
- Switching performance is guaranteed over full temperature and V_{CC} supply range

Connection Diagram



TL/F/9167–1

Order Number DM54ALS590J or DM74ALS590M, N
See NS Package Number J16A, M16A or N16A

This document contains information on a product under development. NSC reserves the right to change or discontinue this product without notice.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Voltage Applied to Disabled Output	5.5V
Operating Free-Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54ALS590			DM74ALS590			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current	$\overline{RCO}$			−1			−1	mA
		Q			−1			−2.6	
I_{OL}	Low Level Output Current	$\overline{RCO}$			8			16	mA
		Q			12			24	
f_{CCK}	Counter Clock Frequency		0			0			MHz
f_{RCK}	Register Clock Frequency		0			0			MHz
t_W (CCK)	Width of Counter Clock Pulse								ns
t_W ($\overline{CCLR}$)	Width of Counter Clear Pulse								ns
t_W (RCK)	Width of Register Clock Pulse								ns
t_{SU}	Setup Time	$\overline{CCKEN}$ Low before CCK P							ns
		$\overline{CCLR}$ Inactive before CCK P							
		CCK before RCK P (Note 1)							
t_H	Hold Time	$\overline{CCKEN}$ Low after CCK P							ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: This setup time ensures the register will see stable data from the counter outputs. The clocks may be tied together in which case the register state will be one clock pulse behind the counter.

Electrical Characteristics over recommended free air temperature range

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5 to 5.5V, I_{OH} = −0.4 mA		V_{CC} − 2			V
		V_{CC} = Min, I_{OH} = Max		2.4	3.2		
V_{OL}	Low Level Output Voltage	V_{CC} = Min	54/74ALS I_{OL} = 12 mA		0.25	0.4	V
			74ALS I_{OL} = 24 mA		0.35	0.5	
I_{OZH}	Off-State Output Current With High Level Voltage Applied	V_{CC} = Min, V_{IL} = Max, V_{IH} = Min, V_O = 2.7V				20	μA
I_{OZL}	Off-State Output Current With Low Level Voltage Applied	V_{CC} = Min, V_{IL} = Max, V_{IH} = Min, V_O = 0.4V				−20	μA

Electrical Characteristics over recommended free air temperature range (Continued)

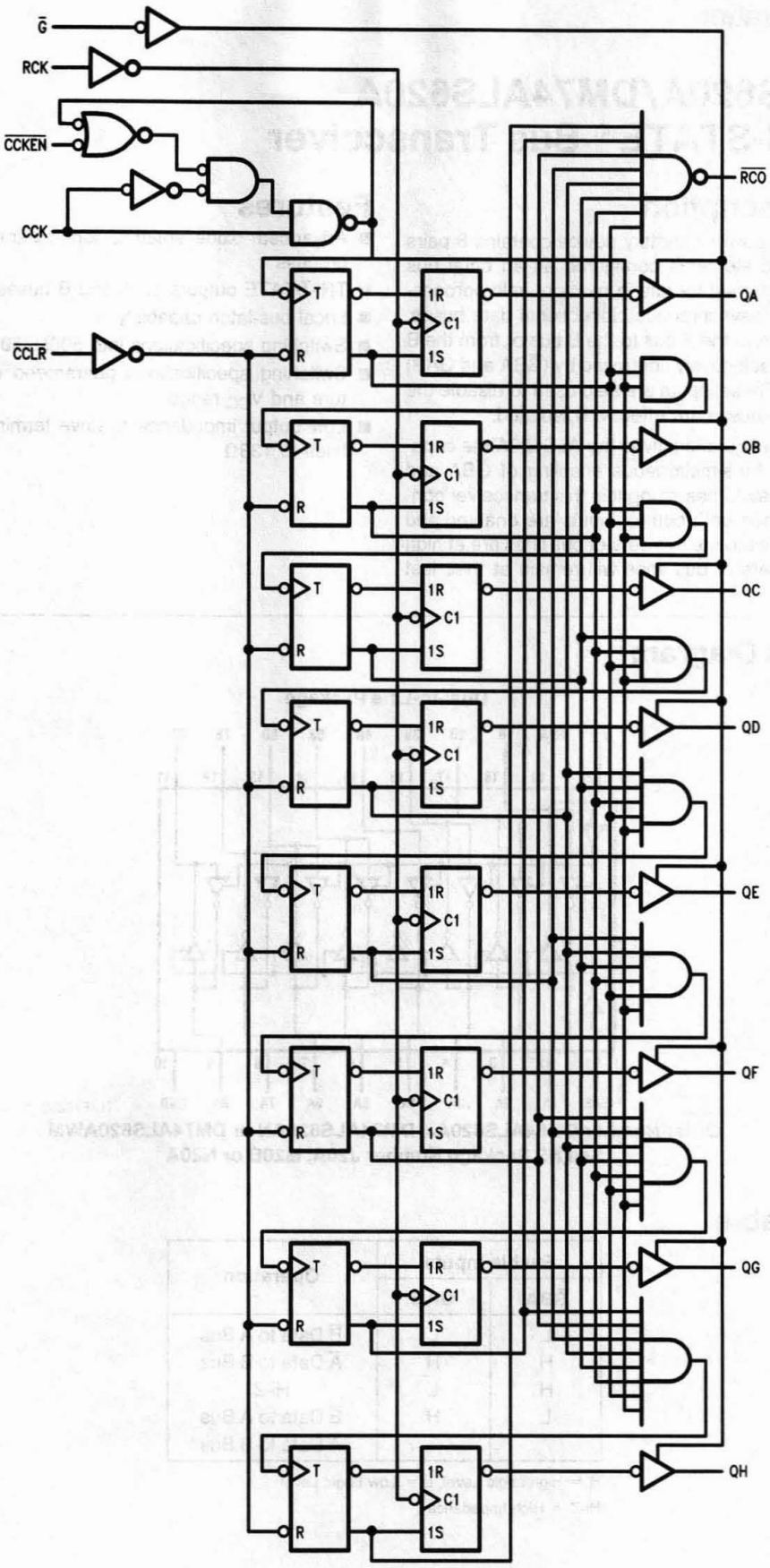
Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
I_I	Input Current at Max Input Voltage	V_{CC} = Max, V_I = 7V				100	μA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−100	μA
I_O	Output Drive Current	V_{CC} = Max, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = Max	Outputs High		33		mA
			Outputs Low		46		
			Outputs Disabled		44		

Switching Characteristics over recommended operating free air temperature range

Symbol	Parameter	Conditions	From (Input) To (Output)	DM54ALS590		DM74ALS590		Units
				Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	V_{CC} = 4.5 to 5.5V, R_L = 480 Ω, $R_1 = R_2$ = 500Ω, T_A = Min to Max	CCK to $\overline{RCO}$					MHz
t_{PLH}	Propagation Delay Time Low to High Level Output		CCK to $\overline{RCO}$					ns
t_{PHL}	Propagation Delay Time High to Low Level Output		CCK to $\overline{RCO}$					ns
t_{PLH}	Propagation Delay Time Low to High Level Output		$\overline{CCLR}$ to $\overline{RCO}$					ns
t_{PLH}	Propagation Delay Time Low to High Level Output		RCK to Q					ns
t_{PHL}	Propagation Delay Time High to Low Level Output		RCK to Q					ns
t_{PLH}	Propagation Delay Time Low to High Level Output		$\overline{G}$ to Q					ns
t_{PHL}	Propagation Delay Time High to Low Level Output		$\overline{G}$ to Q					ns
t_{PZH}	Output Enable Time to High Level Output		$\overline{G}$ to Q					ns
t_{PZL}	Output Enable Time to Low Level Output		$\overline{G}$ to Q					ns
t_{PHZ}	Output Disable Time from High Level Output		$\overline{G}$ to Q					ns
t_{PLZ}	Output DisableTime from Low Level Output		$\overline{G}$ to Q					ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/9167–2

National Semiconductor Corporation

PRELIMINARY

DM54ALS620A/DM74ALS620A Octal TRI-STATE® Bus Transceiver

General Description

This advanced low power Schottky device contains 8 pairs of TRI-STATE logic elements configured as an octal bus transceiver. It is designed for use in memory, microprocessor systems and in asynchronous bidirectional data buses. Data transmission from the A bus to the B bus or from the B bus to the A bus is selectively controlled by ($\overline{G}$BA and GAB) the enable inputs. These inputs are also used to disable the devices so that the buses are effectively isolated.

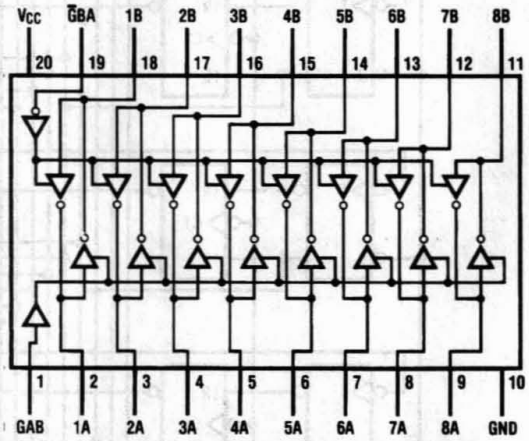
The dual-enable configuration gives the ALS620A the capability to store data by simultaneous enabling of $\overline{G}$BA and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines will remain at their last logic states.

Features

- Advanced oxide-isolated, ion-implanted Schottky TTL process
- TRI-STATE outputs on A and B buses
- Local bus-latch capability
- Switching specifications into 500Ω/50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Low output impedance to drive terminated transmission lines to 133Ω

Connection Diagram

Dual-In-Line Package



TL/F/6230–1

Order Number DM54ALS620AJ, DM74ALS620AN or DM74ALS620AWM
See NS Package Number J20A, M20B or N20A

Function Table

Enable Inputs		Operation
$\overline{G}$BA	GAB	
L	L	$\overline{B}$ Data to A Bus
H	H	$\overline{A}$ Data to B Bus
H	L	Hi-Z
L	H	$\overline{B}$ Data to A Bus, $\overline{A}$ Data to B Bus

H = High Logic Level, L = Low Logic Level

Hi-Z = High Impedance

This document contains information on a product under development. NSC reserves the right to change or discontinue this product without notice.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	
Enable Inputs	7V
I/O Ports	5.5V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS620A			DM74ALS620A			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

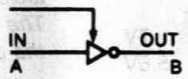
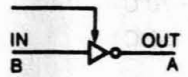
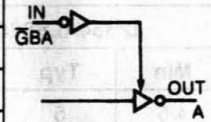
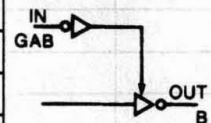
Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		DM54ALS620A			DM74ALS620A			Units
				Min	Typ	Max	Min	Typ	Max	
V_{IK}	Input Clamp Voltage	V_{CC} = 45V, I_{IN} = −18 mA				−1.5			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, I_{OH} = −3mA		2.4	3.2		2.4	3.2		V
		V_{CC} = 4.5V, I_{OH} = Max		2			2			V
		I_{OH} = −0.4 mA, V_{OL} = 4.5V to 5.5V		V_{CC} − 2			V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IN} = 7V (V_{IN} = 5.5V for A or B Ports)				0.1			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IN} = 2.7V (Note 1)				20			20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V (Note 1)				−0.1			−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_{OUT} = 2.25V		−30		−112	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Output High		24	39		24	34	mA
			Output Low		25	49		31	44	mA
			TRI-STATE		27	52		33	47	mA

Note 1: For I/O ports, the parameters I_{IH} and I_{IL} include the off-state current (I_{OZH}, I_{OZL}).

Switching Characteristics over recommended operating free air temperature range (Notes 1 and 2)

Symbol	Parameter	Circuit Configuration	DM54ALS620A		DM74ALS620A		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time, Low to High Level Output		2	12	2	10	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output		2	12	2	10	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output		2	12	2	10	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output		2	12	2	10	ns
t_{PZL}	Output Enable Time to Low Level Output		5	31	5	25	ns
t_{PZH}	Output Enable Time to High Level Output		3	23	3	17	ns
t_{PLZ}	Output Disable Time from Low Level Output		3	22	3	18	ns
t_{PHZ}	Output Disable Time from High Level Output		2	14	2	12	ns
t_{PZL}	Output Enable Time to Low Level Output		5	31	5	25	ns
t_{PZH}	Output Enable Time to High Level Output		3	23	3	18	ns
t_{PLZ}	Output Disable Time from Low Level Output		3	22	3	18	ns
t_{PHZ}	Output Disable Time from High Level Output		2	14	2	12	ns

Note 1: See Section 1 for test waveforms and output load.

Note 2: Switching characteristic conditions are V_{CC} = 4.5V to 5.5V, $R_1 = R_2$ = 500Ω, C_L = 50 pF.

National Semiconductor Corporation

DM54ALS640A/DM74ALS640A Inverting Octal Bus Transceivers

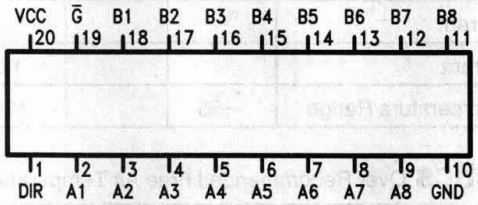
General Description

These inverting octal bus transceivers are designed for asynchronous two-way communication between data busses. These devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input (G) can be used to disable the device so the busses are effectively isolated.

Features

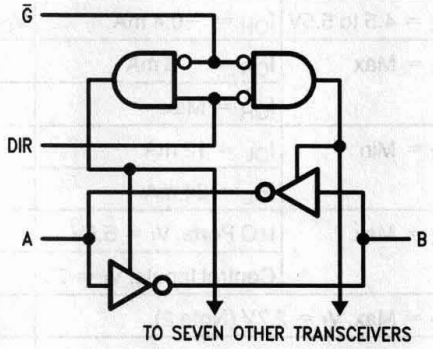
- Advanced Oxide-isolated Ion-implanted Schottky TTL process
- Switching performance is guaranteed over full temperature and V_{CC} supply range
- Switching performance specified at 50 pF
- PNP input design reduces input loading

Connection and Logic Diagrams



TL/F/8640–1

Order Number DM54ALS640AJ, DM74ALS640AWM or DM74ALS640AN
See NS Package Number J20A, M20B or N20A



TL/F/8640–2

Function Table

Control Inputs		Operation
$\overline{G}$	DIR	
L	L	$\overline{B}$ Data to A Bus
L	H	$\overline{A}$ Data to B Bus
H	X	Isolation

L = Low Logic Level
H = High Logic Level
X = Either Low or High Logic Level

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage; Control Inputs	7V
I/O ports	5.5V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS640A			DM74ALS640A			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Operating Free Air Temperature Range	−55		125	0		70	°C

Electrical Characteristics Over Recommended Free Air Temperature Range

Symbol	Parameter	Test Conditions		DM54ALS640A			DM74ALS640A			Units
				Min	Typ	Max	Min	Typ	Max	
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5 to 5.5V	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = Max	I_{OH} = − 3 mA	2.4	3.2		2.4	3.2		
			I_{OH} = Max	2			2			
V_{OL}	Low Level Output Voltage	V_{CC} = Min	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max.	I/O Ports, V_I = 5.5V			100			100	μA
			Control Inputs, V_I = 7V			100			100	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V (Note 2)				20			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V (Note 2)				−100			−100	μA
I_O	Output Drive Current	V_{CC} = Max, V_O = 2.25V		−30		−112	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = Max	Outputs High		19	35		19	30	mA
			Outputs Low		27	45		27	40	
			Outputs Disabled		28	48		28	43	

Note 2: For I/O ports, I_{IH} and I_{IL} parameters include the TRI-STATE output current (I_{OZL} and I_{OZH}).

Switching Characteristics Over Recommended Operating Free Air Temperature Range

Symbol	Parameter	From (Input)	To (Output)	Conditions	DM54ALS640A		DM74ALS640A		Units
					Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	A or B	B or A	V_{CC} = 4.5 to 5.5V, C_L = 50 pF, R1 = R2 = 500Ω (Note 1)	2	14	2	11	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A or B	B or A		2	13	2	10	ns
t_{PZH}	Output Enable Time to High Level Output	$\overline{G}$	A or B		5	25	5	21	ns
t_{PZL}	Output Enable Time to Low Level Output	$\overline{G}$	A or B		8	27	8	24	ns
t_{PHZ}	Output Disable Time from High Level Output	$\overline{G}$	A or B		2	12	2	10	ns
t_{PLZ}	Output Disable Time from Low Level Output	$\overline{G}$	A or B		3	20	3	15	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM54ALS645A/DM74ALS645A Octal Bus Transceivers

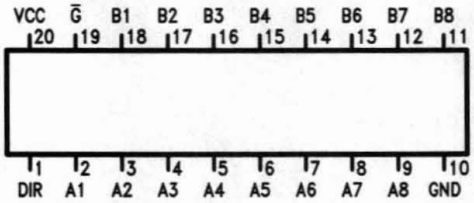
General Description

These octal bus transceivers are designed for asynchronous two-way communication between data busses. These devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input (G) can be used to disable the device so the busses are effectively isolated.

Features

- Advanced Oxide-isolated Ion-implanted Schottky TTL process
- Switching performance is guaranteed over full temperature and V_{CC} supply range
- Switching performance specified at 50 pF
- PNP input design reduces input loading

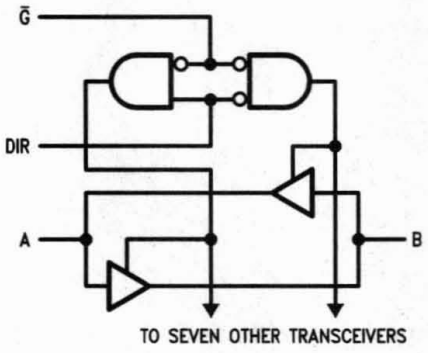
Connection and Logic Diagrams



TL/F/9304–1

Order Number DM54ALS645AJ, DM74ALS645AWM or DM74ALS645AN
See NS Package Number J20A, M20B or N20A

'ALS645A



TL/F/9304–2

Function Table

Control Inputs		Operation
G̅	DIR	
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	Isolation

Low = Low Logic Level
High = High Logic Level
X = Either Low or High Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage; Control Inputs	7V
I/O ports	5.5V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS645A			DM74ALS645A			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Operating Free Air Temperature Range	−55		125	0		70	°C

Electrical Characteristics Over Recommended Free Air Temperature Range

Symbol	Parameter	Test Conditions		DM54ALS645A			DM74ALS645A			Units
				Min	Typ	Max	Min	Typ	Max	
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5 to 5.5V	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = Max	I_{OH} = − 3 mA	2.4	3.2		2.4	3.2		
			I_{OH} = Max	2			2			
V_{OL}	Low Level Output Voltage	V_{CC} = Min	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	I/O Ports, V_I = 5.5V			100			100	μA
			Control Inputs, V_I = 7V			100			100	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V (Note 2)				20			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V (Note 2)				−100			−100	μA
I_O	Output Drive Current	V_{CC} = Max, V_O = 2.25V		−30		−112	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = Max	Outputs High		30	48		30	45	mA
			Outputs Low		36	60		36	55	
			Outputs Disabled		38	63		38	58	

Note 2: For I/O ports, I_{IH} and I_{IL} parameters include the TRI-STATE® output current (I_{OZL} and I_{OZH}).

Switching Characteristics Over Recommended Operating Free Air Temperature Range

Symbol	Parameter	From (Input)	To (Output)	Conditions	DM54ALS645A		DM74ALS645A		Units
					Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	A or B	B or A	V_{CC} = 4.5 to 5.5V, C_L = 50 pF, R1 = R2 = 500Ω (Note 1)	1	15	3	10	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A or B	B or A		1	13	3	10	ns
t_{PZH}	Output Enable Time to High Level Output	$\overline{G}$	A or B		2	30	5	20	ns
t_{PZL}	Output Enable Time to Low Level Output	$\overline{G}$	A or B		2	29	5	20	ns
t_{PHZ}	Output Disable Time from High Level Output	$\overline{G}$	A or B		2	14	2	10	ns
t_{PLZ}	Output Disable Time from Low Level Output	$\overline{G}$	A or B		2	30	4	15	ns

Note 1: See Section 1 for Test Waveforms and Output Load.

National Semiconductor Corporation

PRELIMINARY

DM54ALS646/DM74ALS646 Octal TRI-STATE® Bus Transceivers and Registers

General Description

This device incorporates an octal bus transceiver and an octal D-type register configured to enable multiplexed transmission of data from bus to bus or internal register to bus.

This bus transceiver features totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic level drive provides this device with the capability of being connected directly to and driving the bus lines in a bus-organized system without the need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The registers in the ALS646 are edge-triggered D-type flip-flops. On the positive transition of the clock (CAB or CBA), the input bus data is stored into the appropriate register. The CAB input controls the transfer of data into the A register and the CBA input controls the B register.

The SAB and SBA control pins are provided to select whether real-time data or stored data is transferred. A low input level selects real-time data, and a high level selects stored data. The select controls have a "make before break" configuration to eliminate a glitch which would normally occur in a typical multiplexer during the transition between store and real-time data.

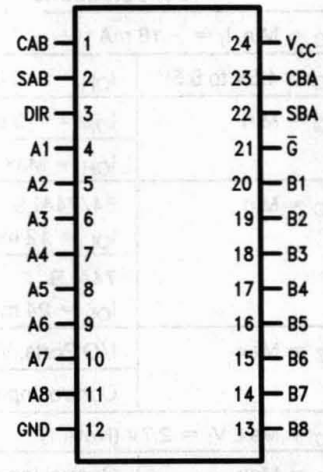
The enable $\overline{G}$ and direction control pins provide four modes of operation: real-time data transfer from bus A to B, real-time data transfer from bus B to A, real-time bus A and/or B data transfer to internal storage, or internally stored data transfer to bus A or B.

When the enable $\overline{G}$ pin is low, the direction pin selects which bus receives data. When the enable G pin is high, both buses become disabled yet their input function is still enabled.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- TRI-STATE buffer outputs drive bus lines directly
- Multiplexed real-time and stored data
- Independent registers for A and B buses

Connection Diagram



TL/F/9172–1

Order Number DM54ALS646J or DM74ALS646WM, N
See NS Number Package J24A, M24B or N24A

This document contains information on a product under development. NSC reserves the right to change or discontinue this product without notice.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	
Control Inputs	7V
I/O Ports	5.5V
Operating Free-Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS646			DM74ALS646			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			12			24	mA
f_{CLK}	Clock Frequency	0		35	0		40	MHz
t_W	Pulse Duration, Clocks Low or High	14.5			12.5			ns
t_{SU}	Data Setup Time, A before CAB or B before CBA	15 ↑			10 ↑			ns
t_H	Data Hold Time, A after CAB or B after CBA	0 ↑			0 ↑			ns
T_A	Free Air Operating Temperature	−55		125	0		70	°C

↑ = With reference to the low to high transition of the respective clock.

Electrical Characteristics over recommended free air temperature range

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V	I_{OH} = −0.4 mA	V_{CC} − 2			V
		V_{CC} = Min	I_{OH} = −3 mA	2.4	3.2		
			I_{OH} = Max	2			
V_{OL}	Low Level Output Voltage	V_{CC} = Min	54/74ALS I_{OL} = 12 mA		0.25	0.4	V
			74ALS I_{OL} = 24 mA		0.35	0.5	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	I/O Ports, V_I = 5.5V			100	μA
			Control Inputs, V_I = 7V			100	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V (Note 1)				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V, (Note 1)	Control Inputs			−200	μA
			I/O Ports			−200	
I_O	Output Drive Current	V_{CC} = Max, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = Max	Outputs High		47	76	mA
			Outputs Low		55	88	
			Outputs Disabled		55	88	

Note 1: For I/O ports the TRI-STATE output currents (I_{OZH} and I_{OZL}) are included in the I_{IH} and I_{IL} parameters.

Switching Characteristics over recommended operating free air temperature range

Symbol	Parameter	Conditions	From (Input) To (Output)	DM54ALS646		DM74ALS646		Units
				Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, $R_1 = R_2$ = 500Ω, T_A = Min to Max (Note 1)	CBA or CAB to A or B	10	35	10	30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		CBA or CAB to A or B	5	20	5	17	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		A or B to B or A	5	22	5	20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		A or B to B or A	3	15	3	12	ns
t_{PLH}	Propagation Delay Time Low to High Level Output (with A or B Low) (Note 2)		SBA or SAB to A or B	15	40	15	35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output (with A or B Low) (Note 2)		SBA or SAB to A or B	5	23	5	20	ns
t_{PLH}	Propagation Delay Time Low to High Level Output (with A or B High) (Note 2)		SBA or SAB to A or B	8	30	8	25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output (with A or B High) (Note 2)		SBA or SAB to A or B	5	24	5	20	ns
t_{PZH}	Output Enable Time to High Level Output		$\overline{G}$ to A or B	3	20	3	17	ns
t_{PZL}	Output Enable Time to Low Level Output		$\overline{G}$ to A or B	5	22	5	20	ns
t_{PHZ}	Output Disable Time from High Level Output		$\overline{G}$ to A or B	1	12	1	10	ns
t_{PLZ}	Output Disable Time from Low Level Output		$\overline{G}$ to A or B	2	20	2	16	ns
t_{PZH}	Output Enable Time to High Level Output		DIR to A or B	10	38	10	30	ns
t_{PZL}	Output Enable Time to Low Level Output		DIR to A or B	5	30	5	25	ns
t_{PHZ}	Output Disable Time from High Level Output		DIR to A or B	1	12	1	10	ns
t_{PLZ}	Output Disable Time from Low Level Output		DIR to A or B	2	21	2	16	ns

Note 1: See Section 1 for test waveforms and output load.

Note 2: These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

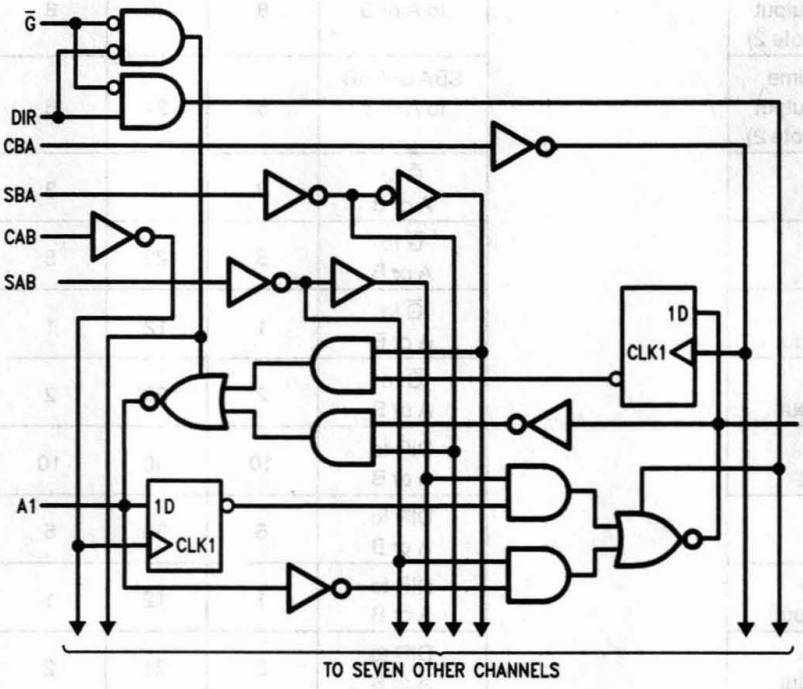
Function Table

Inputs						Data I/O (Note 1)		Operation or Function
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A1 thru A8	B1 thru B8	
X	X	↑	X	X	X	Input	Not Specified	Store A, B Unspecified
X	X	X	↑	X	X	Not Specified	Input	Store B, A Unspecified
H	X	↑	↑	X	X	Input	Input	Store A and B Data
H	X	H/L	H/L	X	X	Input	Input	Isolation, Hold Storage
L	L	X	X	X	L	Output	Input	Real-Time B Data to a Bus
L	L	X	H/L	X	H	Output	Input	Stored B Data to a Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
L	H	H/L	X	H	X	Input	Output	Stored A Data to B Bus

Note 1: The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

H = High Logic Level, L = Low Logic Level, X = Don't Care (Either Low or High Logic Levels including transitions), H/L = Either Low or High Logic Level excluding transitions, ↑ = Positive going edge of pulse.

Logic Diagram



TL/F/9172–2

National Semiconductor Corporation

PRELIMINARY

DM54ALS648/DM74ALS648 Octal TRI-STATE® Inverting Bus Transceivers

General Description

This device incorporates an octal bus transceiver and an octal D-type register configured to enable multiplexed transmission of data from bus to bus or internal register to bus.

This bus transceiver features totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic level drive provides this device with the capability of being connected directly to and driving the bus lines in a bus-organized system without the need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The registers in the ALS648 are edge-triggered D-type flip-flops. On the positive transition of the clock (CAB or CBA), the input bus data is stored into the appropriate register. The CAB input controls the transfer of data into the A register and the CBA input controls the B register.

The SAB and SBA control pins are provided to select whether real-time data or stored data is transferred. A low input level selects real-time data, and a high level selects stored data. The select controls have a "make before break" configuration to eliminate a glitch which would normally occur in a typical multiplexer during the transition between stored and real-time data.

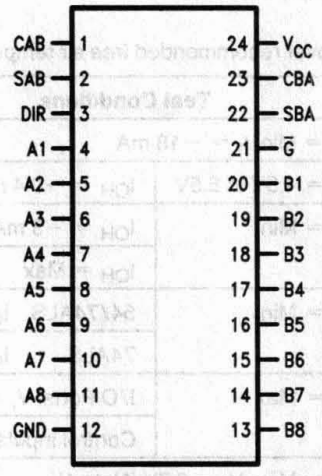
The enable $\overline{G}$ and direction control pins provide four modes of operation: real-time data transfer from bus A to B, real-time data transfer from bus B to A, real-time bus A and/or B data transfer to internal storage, or internally stored data transfer to bus A or B.

When the enable $\overline{G}$ pin is low, the direction pin selects which bus receives data. When the enable G pin is high, both buses became disabled yet their input function is still enabled.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- TRI-STATE buffer outputs drive bus lines directly
- Multiplexed real-time and stored data
- Independent registers for A and B buses

Connection Diagram



TL/F/9173–1

Order Number DM54ALS648J or DM74ALS648WM, N
See NS Package Number J24A, M24B or N24A

2

This document contains information on a product under development. NSC reserves the right to change or discontinue this product without notice.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	
Control Inputs	7V
I/O Ports	5.5V
Operating Free-Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS648			DM74ALS648			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			12			24	mA
f_{CLOCK}	Clock Frequency	0		35	0		40	MHz
t_W	Pulse Duration, Clocks Low or High	14.5			12.5			ns
t_{SU}	Data Setup Time, A before CAB or B before CBA	15↑			10↑			ns
t_H	Data Hold Time, A after CAB or B after CBA	0↑			0↑			ns
T_A	Free Air Operating Temperature Range	−55		125	0		70	°C

↑ = With reference to the low to high transition of the respective clock.

Electrical Characteristics over recommended free air temperature range

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V	I_{OH} = −0.4 mA	V_{CC} − 2			
		V_{CC} = Min	I_{OH} = −3 mA	2.4	3.2		V
			I_{OH} = Max	2			
V_{OL}	Low Level Output Voltage	V_{CC} = Min	54/74ALS I_{OL} = 12 mA		0.25	0.4	V
			74ALS I_{OL} = 24 mA		0.35	0.5	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	I/O Ports, V_I = 5.5V			100	μA
			Control Inputs, V_I = 7V			100	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V (Note 1)				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V (Note 1)	Control Inputs			−200	μA
			I/O Ports			−200	
I_O	Output Drive Current	V_{CC} = Max, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = Max	Outputs High		47	76	mA
			Outputs Low		57	88	
			Outputs Disabled		57	88	

Note 1: For I/O ports the TRI-STATE output currents (I_{OZH} and I_{OZL}) are included in the I_{IH} and I_{IL} parameters.

Switching Characteristics over recommended operating free air temperature range

Symbol	Parameter	Conditions	From (Input) To (Output)	DM54ALS648		DM74ALS648		Units
				Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, $R_1 = R_2 = 500\Omega$, T_A = Min to Max (Note 1)	CBA or CAB to A or B	8	39	8	33	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		CBA or CAB to A or B	5	23	5	20	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		A or B to B or A	3	20	3	17	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		A or B to B or A	2	12	2	10	ns
t_{PLH}	Propagation Delay Time Low to High Level Output (with A or B Low)(Note 2)		SBA or SAB to A or B	5	44	5	39	ns
t_{PHL}	Propagation Delay Time High to Low Level Output (with A or B Low)(Note 2)		SBA or SAB to A or B	4	26	4	22	ns
t_{PLH}	Propagation Delay Time Low to High Level Output (with A or B High)(Note 2)		SBA or SAB to A or B	6	30	6	25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output (with A or B High)(Note 2)		SBA or SAB to A or B	6	25	6	21	ns
t_{PZH}	Output Enable Time to High Level Output		$\overline{G}$ to A or B	4	25	4	22	ns
t_{PZL}	Output Enable Time to Low Level Output		$\overline{G}$ to A or B	4	25	4	22	ns
t_{PHZ}	Output Disable Time from High Level Output		$\overline{G}$ to A or B	1	12	1	10	ns
t_{PLZ}	Output Disable Time from Low Level Output		$\overline{G}$ to A or B	2	21	2	15	ns
t_{PZH}	Output Enable Time to High Level Output		DIR to A or B	4	35	4	27	ns
t_{PZL}	Output Enable Time to Low Level Output		DIR to A or B	3	25	3	19	ns
t_{PHZ}	Output Disable Time from High Level Output		DIR to A or B	1	17	1	14	ns
t_{PLZ}	Output Disable Time from Low Level Output		DIR to A or B	2	22	2	15	ns

Note 1: See Section 1 for test waveforms and output load.

Note 2: These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

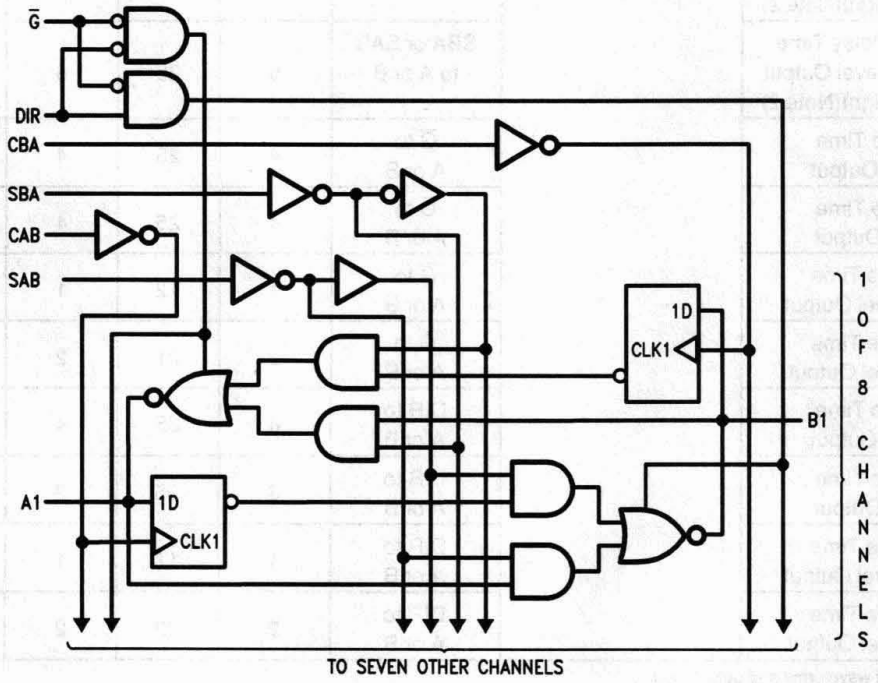
Function Table

Inputs						Data I/O (Note 3)		Operation or Function
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A1 thru A8	B1 thru B8	
X	X	↑	X	X	X	Input	Not Specified	Store A, B Unspecified
X	X	X	↑	X	X	Not Specified	Input	Store B, A Unspecified
H	X	↑	↑	X	X	Input	Input	Store A and B Data
H	X	H/L	H/L	X	X	Input	Input	Isolation, Hold Storage
L	L	X	X	X	L	Output	Input	Real-Time $\overline{B}$ Data to A Bus
L	L	X	H/L	X	H	Output	Input	Stored $\overline{B}$ Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time $\overline{A}$ Data to B Bus
L	H	H/L	X	H	X	Input	Output	Stored $\overline{A}$ Data to B Bus

Note 3: The data output functions may be enabled or disabled by various signals at the G and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

H = High Logic Level, L = Low Logic Level, X = Don't Care (Either Low or High Logic Levels including transitions), H/L = Either Low or High Logic Level excluding transitions, ↑ = Positive-going edge of pulse.

Logic Diagram



TL/F/9173–2

National Semiconductor Corporation

DM54ALS652/DM74ALS652 Octal TRI-STATE® Bus Transceivers and Registers

General Description

This device incorporates an octal transceiver and an octal D-type register configured to enable transmission of data from bus to bus or internal register to bus.

This bus transceiver features totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high level logic drive provide this device with the capability of being connected directly to and driving the bus lines in a bus organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The registers in the AS652 are edge-triggered D-type flip-flops. On the positive transition of the clock (CAB or CBA), the input data is stored into the appropriate register. The CAB input controls the transfer of data into the A register and the CBA input controls the B register.

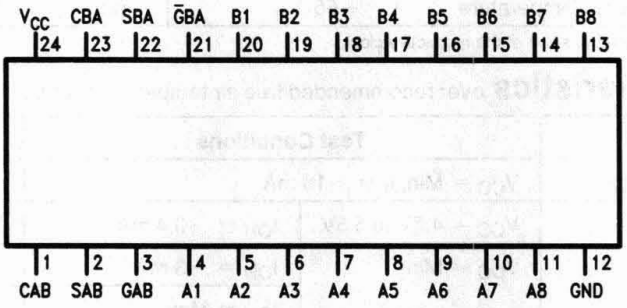
The SAB and SBA control pins are provided to select whether real-time data or stored data is transferred. A low input level selects real-time data and a high level selects stored data. The select controls have a "make before break" configuration to eliminate a glitch which would normally occur in a typical multiplexer during the transition between stored and real-time data.

The enable (GAB and $\overline{G}$BA) control pins provide four modes of operation: real-time data transfer from bus A to B, real-time data transfer from bus B to A, real-time bus A and/or B data transfer to internal storage, or internal stored data transfer to bus A and/or B.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- TRI-STATE buffer-type outputs drive bus lines directly
- Independent registers and enables for A and B buses
- Multiplexed real-time and stored data

Connection Diagram



TL/F/9174–1

Order Number DM54ALS652J, DM74ALS652N or DM74ALS652WM
See NS Package Number J24A, M24B or N24A

This document contains information on a product under development. NSC reserves the right to change or discontinue this product without notice.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	
Control Inputs	7V
I/O Ports	5.5V
Operating Free-Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS652			DM74ALS652			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			12			24	mA
f_{CLK}	Clock Frequency	0		35	0		40	MHz
t_W	Pulse Duration, Clocks Low or High	14.5			12.5			ns
t_{SU}	Data Setup Time, A before CAB or B before CBA	15↑			10↑			ns
t_H	Data Hold Time, A after CAB or B after CBA	5↑			0↑			ns
T_A	Free Air Operating Temperature	−55		125	0		70	°C

↑ = with reference to the low to high transition of the respective clock.

Electrical Characteristics over recommended free air temperature range

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V	I_{OH} = −0.4 mA	V_{CC} − 2			V
		V_{CC} = Min	I_{OH} = −3 mA	2.4	3.2		
			I_{OH} = Max	2			
V_{OL}	Low Level Output Voltage	V_{CC} = Min	54/74ALS I_{OL} = 12 mA		0.25	0.4	V
			74ALS I_{OL} = 24 mA		0.35	0.5	
I_I	Input Current at Max Input Voltage	V_{CC} = Max	I/O Ports, V_I = 5.5V			100	μA
			Control Inputs, V_I = 7V			100	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V, (Note 1)				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V (Note 1)	Control Inputs			−200	μA
			I/O Ports			−200	
I_O	Output Drive Current	V_{CC} = Max, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = Max	Outputs High		47	76	mA
			Outputs Low		55	88	
			Outputs Disabled		55	88	

Note 1: For I/O ports the TRI-STATE output currents (I_{OZH} and I_{OZL}) are included in the I_{IH} and I_{IL} parameters.

Switching Characteristics over recommended operating free air temperature range

Symbol	Parameter	Conditions	From (Input) To (Output)	DM54ALS652		DM74ALS652		Units
				Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, $R_1 = R_2 = 500\Omega$, T_A = Min to Max (Note 1)	CBA or CAB to A or B	10	35	10	30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		CBA or CAB to A or B	5	20	5	17	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		A or B to B or A	5	20	5	18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		A or B to B or A	3	15	3	12	ns
t_{PLH}	Propagation Delay Time Low to High Level Output (with A or B Low) (Note 2)		SBA or SAB to A or B	15	40	15	35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output (with A or B Low) (Note 2)		SBA or SAB to A or B	6	23	6	20	ns
t_{PLH}	Propagation Delay Time Low to High Level Output (with A or B High) (Note 2)		SBA or SAB to A or B	8	30	8	25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output (with A or B High) (Note 2)		SBA or SAB to A or B	5	24	5	20	ns
t_{PZH}	Output Enable Time to High Level Output		$\overline{G}$BA to A or B	3	20	3	17	ns
t_{PZL}	Output Enable Time to Low Level Output		$\overline{G}$BA to A or B	5	22	5	18	ns
t_{PHZ}	Output Disable Time from High Level Output		$\overline{G}$BA to A or B	1	12	1	10	ns
t_{PLZ}	Output Disable Time from Low Level Output		$\overline{G}$BA to A or B	2	20	2	16	ns
t_{PZH}	Output Enable Time to High Level Output		GAB to A or B	8	25	8	22	ns
t_{PZL}	Output Enable Time to Low Level Output		GAB to A or B	6	21	6	18	ns
t_{PHZ}	Output Disable Time from High Level Output		GAB to A or B	1	12	1	10	ns
t_{PLZ}	Output Disable Time from Low Level Output		GAB to A or B	2	21	2	16	ns

Note 1: See Section 1 for test waveforms and output load.
Note 2: These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

2

Function Table

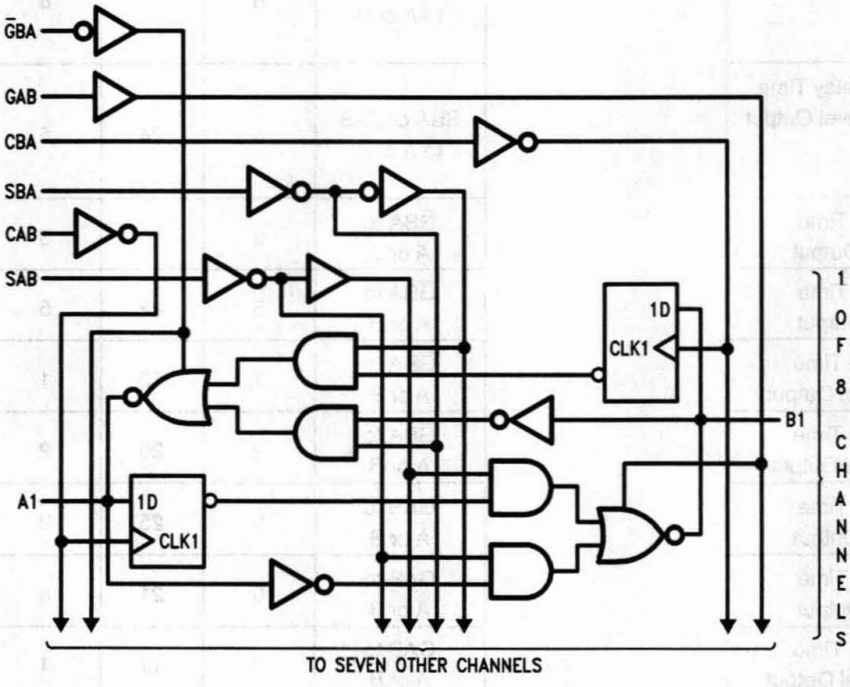
Inputs						Data I/O (Note 3)		Operation or Function
$\overline{G}$AB	GBA	CAB	CBA	SAB	SBA	A1 thru A8	B1 thru B8	
X	H	↑	H/L	X	X	Input	Not Specified	Store A, Hold B
L	X	H/L	↑	X	X	Not Specified	Input	Store B, Hold A
L	H	↑	↑	X	X	Input	Input	Store A and B Data
L	H	H/L	H/L	X	X	Input	Input	Isolation, Hold Storage
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H/L	X	H	Output	Input	Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
H	H	↑	↑	X	X	Input	Output	Stored A Data to B Bus
H	H	↑	↑	X (Note 4)	X	Input	Output	Store A in both Registers
L	L	↑	↑	X	X (Note 4)	Output	Input	Store B in both Registers

Note 3: The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

Note 4: Select control = L; clocks can occur simultaneously
Select control = H; clocks must be staggered in order to load both registers.

H = High Logic Level, L = Low Logic Level, X = Don't Care (Either Low or High Logic Levels, including transitions), H/L = Either Low or High Logic Level excluding transitions, ↑ = Positive-going edge of pulse.

Logic Diagram



TL/F/9174–2

National Semiconductor Corporation

DM54ALS689/DM74ALS689 8-Bit Comparator

General Description

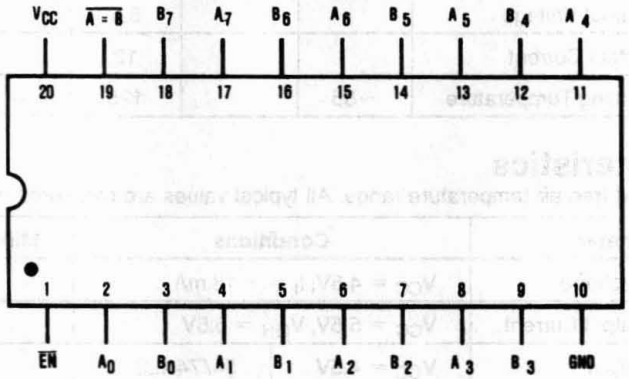
This comparator performs an "equal to" comparison of two eight-bit words with provision for expansion or external enabling. The matching of the two 8-bit inputs plus a logic LOW on the $\overline{EN}$ input produces the output $\overline{A = B}$. The ALS689 has an open collector output for wire AND cascading.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with LS family TTL counterpart
- Improved output transient handling capability

Connection Diagram

Dual-In-Line Package



TL/F/6238–1

Order Number DM54ALS689J, DM74ALS689WM or DM74ALS689N
See NS Package Number J20A, M20B or N20A

Function Table

Inputs		Output
$\overline{EN}$	Data	$\overline{A = B}$
L	A = B	L
L	A ≠ B	H
H	X	H

H = High Level, L = Low Level, X = Don't Care

National Semiconductor Corporation

DM54ALS689/DM74ALS689 8-Bit Comparator

General Description

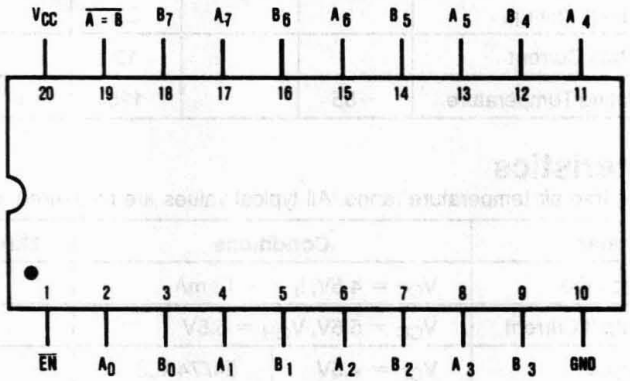
This comparator performs an "equal to" comparison of two eight-bit words with provision for expansion or external enabling. The matching of the two 8-bit inputs plus a logic LOW on the $\overline{EN}$ input produces the output $\overline{A = B}$. The ALS689 has an open collector output for wire AND cascading.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with LS family TTL counterpart
- Improved output transient handling capability

Connection Diagram

Dual-In-Line Package



TL/F/6238–1

Order Number DM54ALS689J, DM74ALS689WM or DM74ALS689N
See NS Package Number J20A, M20B or N20A

Function Table

Inputs		Output
$\overline{EN}$	Data	$\overline{A = B}$
L	A = B	L
L	A ≠ B	H
H	X	H

H = High Level, L = Low Level, X = Don't Care

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Off State Output Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS689			DM74ALS689			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
I_{OH}	High Level Output Current	V_{CC} = 5.5V, V_{OH} = 5.5V				0.1	mA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 12 mA		0.25	0.4	V
			74ALS I_{OL} = 24 mA		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_{CC}	Supply Current	V_{CC} = 5.5V (Note 1)			12	19	mA

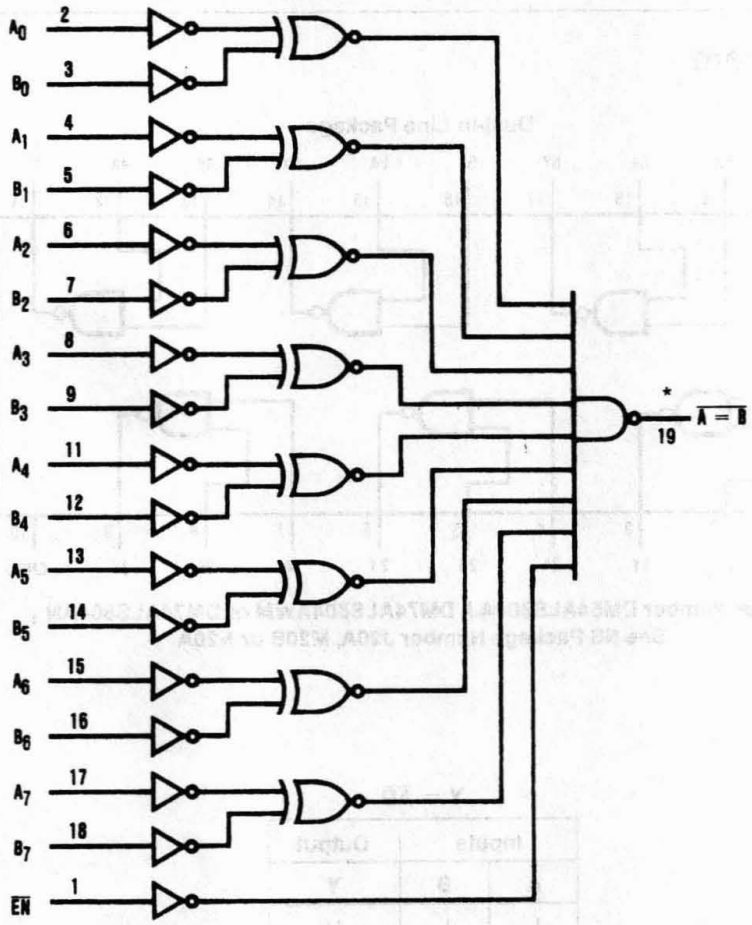
Note 1: I_{CC} is measured with $\overline{EN}$ grounded, A and B inputs at 4.5V.

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From (Input)	To (Output)	DM54ALS689		DM74ALS689		Units
					Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V C_L = 50 pF R_L = 667Ω	A or B Data	$\overline{A = B}$	10	30	10	25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		A or B Data	$\overline{A = B}$	5	25	5	23	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		$\overline{EN}$	$\overline{A = B}$	8	30	8	25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		$\overline{EN}$	$\overline{A = B}$	8	30	8	25	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6238–2

*Output is open collector

National Semiconductor Corporation

DM54ALS804A/DM74ALS804A Hex 2-Input NAND Drivers

General Description

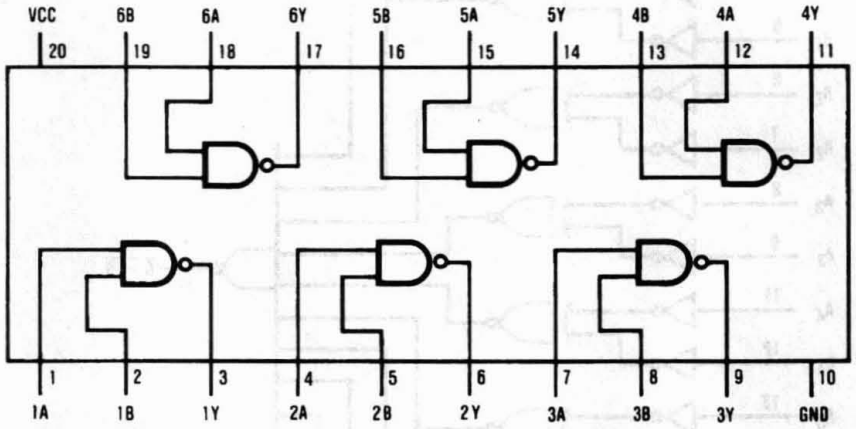
These devices contain six independent 2-input drivers, each of which performs the logic NAND function.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky and low power Schottky TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts

Connection Diagram

Dual-In-Line Package



TL/F/6239–1

Order Number DM54ALS804AJ, DM74ALS804AWM or DM74ALS804AN
See NS Package Number J20A, M20B or N20A

Function Table

$$Y = \overline{AB}$$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level

L = Low Logic Level

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS804A			DM74ALS804A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

*Applies for the DM74ALS804-1 option only.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA, V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
		I_{OH} = −3 mA, V_{CC} = 4.5V		2.4			V
		I_{OH} = Max, V_{CC} = 4.5V		2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 12 mA		0.25	0.4	V
			74ALS I_{OL} = 24 mA		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	V_I = 0V, Outputs High		0.9	2.5	mA
			V_I = 4.5V, Outputs Low		7	12	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	DM54ALS804A		DM74ALS804A		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V, R_L = 500Ω, C_L = 50 pF	2	9	2	7	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		2	9	2	8	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM54ALS805A/DM74ALS805A Hex 2-Input NOR Drivers

General Description

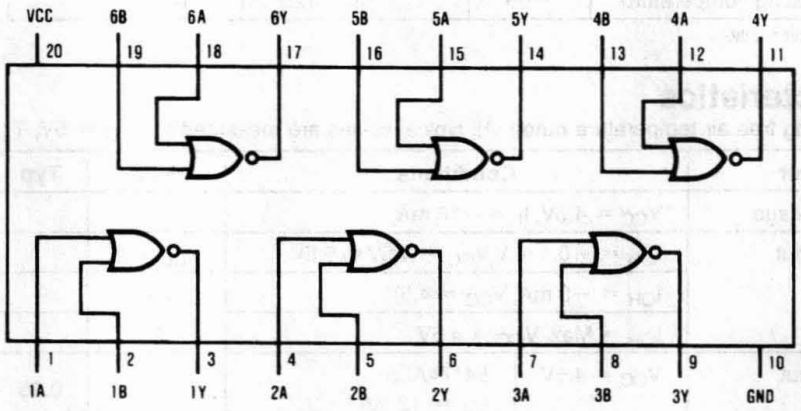
These devices contain six independent 2-input drivers, each of which performs the logic NOR function.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky and low power Schottky TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts

Connection Diagram

Dual-In-Line Package



TL/F/6240–1

Order Number DM54ALS805AJ, DM74ALS805AWM or DM74ALS805AN
See NS Package Number J20A, M20B or N20A

Function Table

$$Y = \overline{A + B}$$

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS805A			DM74ALS805A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

*Applies for the DM74ALS805-1 option only.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA, V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
		I_{OH} = −3 mA, V_{CC} = 4.5V		2.4			V
		I_{OH} = Max, V_{CC} = 4.5V		2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 12 mA		0.25	0.4	V
			74ALS I_{OL} = 24 mA		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	V_I = 0V, Outputs High		2	4	mA
			V_I = 4.5V, Outputs Low		8	14	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	DM54ALS805A		DM74ALS805A		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V, R_L = 500Ω, C_L = 50 pF	2	9	2	7	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		2	9	2	8	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM54ALS808A/DM74ALS808A Hex 2-Input AND Drivers

General Description

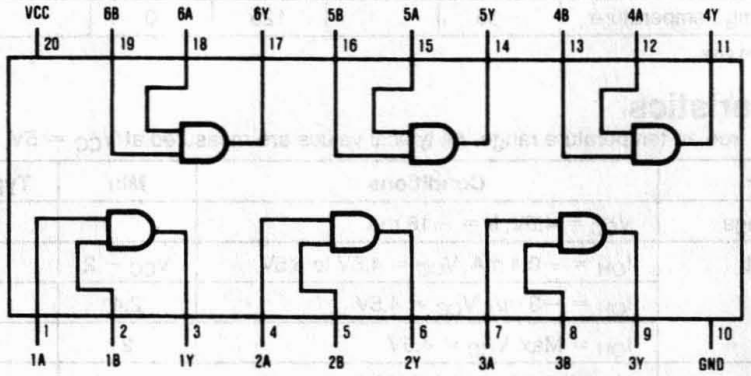
These devices contain six independent 2-input drivers, each of which performs the logic AND function.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky and low power Schottky TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts

Connection Diagram

Dual-In-Line Package



TL/F/6241–1

Order Number DM54ALS808AJ, DM74ALS808AWM or DM74ALS808AN
See NS Package Number J20A, M20B or N20A

Function Table

$Y = AB$

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS808A			DM74ALS808A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = 0.4 mA, V_{CC} = 4.5 to 5.5V		V_{CC} − 2			V
		I_{OH} = −3 mA, V_{CC} = 4.5V		2.4			V
		I_{OH} = Max, V_{CC} = 4.5V		2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 12 mA		0.25	0.4	V
			74ALS I_{OL} = 24 mA		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		4.5	7	mA
			Outputs Low		8	16	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	DM54ALS808A		DM74ALS808A		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V, R_L = 500Ω, C_L = 50 pF	2	11	2	9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		1	10	1	8	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM54ALS810/DM74ALS810 Quad 2-Input Exclusive-NOR Gates

General Description

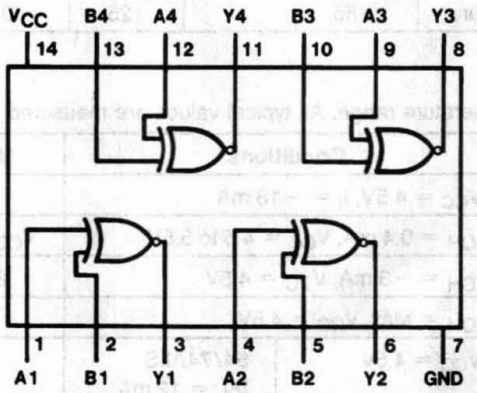
This device contains four independent gates, each of which performs the logic exclusive-NOR function.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky and low power Schottky TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts

Connection Diagram

Dual-In-Line Package



TL/F/6714–1

Order Number DM54ALS810J, DM74ALS810M or DM74ALS810N
See NS Package Number J14A, M14A or N14A

Function Table

$$\overline{Y} = A \oplus B$$

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS810			DM74ALS810			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted).

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	V_{CC} − 2	3.4		V
			DM74	V_{CC} − 2	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IL} = Max, V_{IH} = Min	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = Max, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 2)			5	7.5	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: I_{CC} is measured with all outputs open, one input of each gate at 4.5V, and the other inputs grounded.

Switching Characteristics over recommended operating free air temperature range

Symbol	Parameter	Conditions	DM54ALS810		DM74ALS810		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Other Input Low V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	5	23	5	20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		3	17	3	14	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Other Input High V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	5	21	5	18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		3	17	3	14	ns

National Semiconductor Corporation

DM54ALS811/DM74ALS811 Quad 2-Input Exclusive-NOR Gates with Open-Collector Outputs

General Description

This device contains four independent gates, each of which performs the logic exclusive-NOR function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

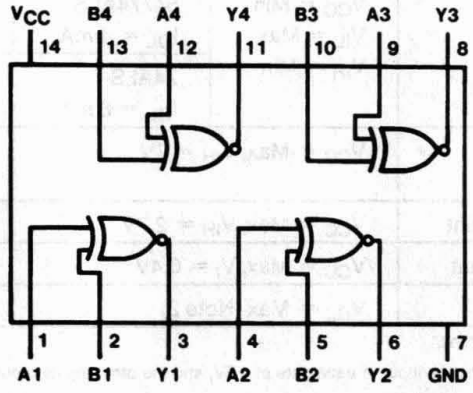
$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky and low power Schottky TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts

Connection Diagram

Dual-In-Line Package



TL/F/6715–1

Order Number DM54ALS811J or DM74ALS811M, N
See NS Package Number J14A, M14A or N14A

Function Table

$$\overline{Y} = A \oplus B$$

Inputs		Output
A	B	$\overline{Y}$
L	L	H
L	H	L
H	L	L
H	H	H

H = High Logic Level

L = Low Logic Level

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS811			DM74ALS811			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max, V_{IH} = Min				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min V_{IL} = Max V_{IH} = Min	54/74ALS I_{OL} = 4 mA		0.25	0.4	V
			74ALS I_{OL} = 8 mA		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = Max, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.1	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 2)			5	7.5	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: I_{CC} is measured with all outputs open, one input of each gate at 4.5V, and the other inputs grounded.

Switching Characteristics over recommended operating free air temperature range

Symbol	Parameter	Conditions	DM54ALS811		DM74ALS811		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Other Input Low V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	25	60	25	55	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		5	30	5	28	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Other Input High V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	20	55	20	50	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		5	28	5	23	ns

National Semiconductor Corporation

DM54ALS832A/DM74ALS832A Hex 2-Input OR Drivers

General Description

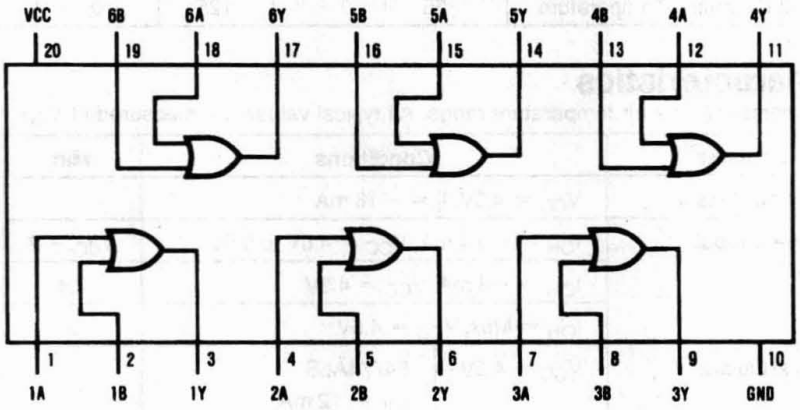
These devices contain six independent drivers, each of which performs the logic OR function.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky and low power Schottky TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts

Connection Diagram

Dual-In-Line Package



TL/F/6242–1

Order Number DM54ALS832AJ or DM74ALS832AWM, N
See NS Package Number J20A, M20B or N20A

Function Table

$Y = A + B$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

H = High Logic Level
L = Low Logic Level

2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS832A			DM74ALS832A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA, V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
		I_{OH} = −3 mA, V_{CC} = 4.5V		2.4			V
		I_{OH} = Max, V_{CC} = 4.5V		2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 12 mA		0.25	0.4	V
			74ALS I_{OL} = 24 mA		0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	V_I = 4.5V, Outputs High		6	9	mA
			V_I = 0V, Outputs Low		9.5	16	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	DM54ALS832A		DM74ALS832A		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V, R_L = 500Ω, C_L = 50 pF	2	11	2	9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		1	10	1	8	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM54ALS873B/DM74ALS873B Dual 4-Bit D-Type Transparent Latches with TRI-STATE® Outputs

General Description

These dual 4-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the ALS873B are transparent D-type latches. While the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was set up.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

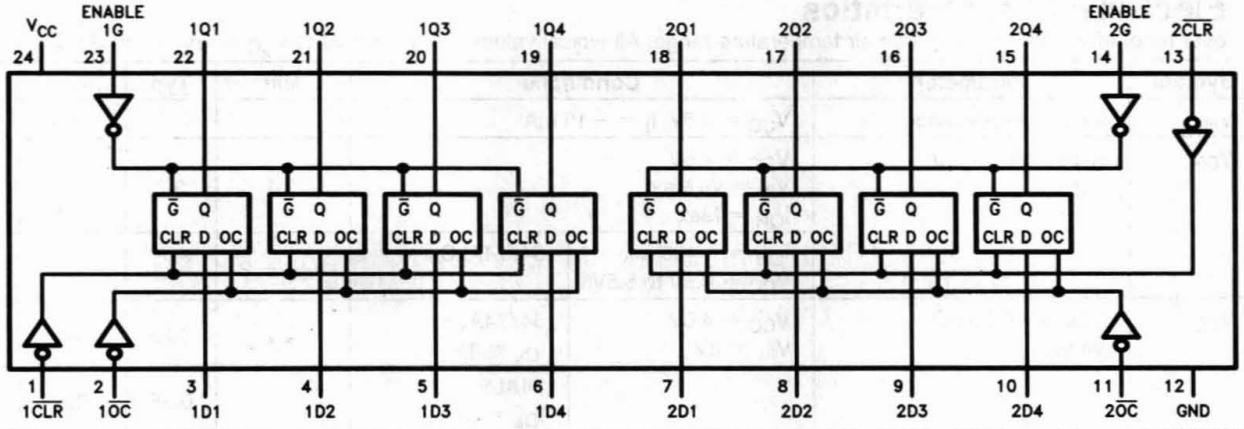
The output control does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- TRI-STATE buffer-type outputs drive bus lines directly
- Space saving 300 mil wide package

Connection Diagram

Dual-In-Line Package



TL/F/6243–1

Order Number DM54ALS873BJ, DM74ALS873BWM or DM74ALS873BNT
See NS Package Number J24A, M24B or N24C

2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Voltage Applied to Disabled Output	5.5V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54ALS873B			DM74ALS873B			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−1			−2.6	mA
I_{OL}	Low Level Output Current				12			24	mA
t_W	Pulse Width	Enable High	10			10			ns
		Clear Low	15			15			ns
t_{SU}	Data Setup Time		10↓			10↓			ns
t_H	Data Hold Time		7↓			7↓			ns
T_A	Operating Free Air Temperature		−55		125	0		70	°C

The (↓) arrow indicates the negative edge of the enable is used for reference.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V V_{IL} = V_{IL}Max I_{OH} = Max		2.4	3.2		V
		I_{OH} = −400 μA V_{CC} = 4.5V to 5.5V	54/74ALS	V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V	54/74ALS I_{OL} = 12 mA		0.25	0.4	V
			74ALS I_{OL} = 24 mA		0.35	0.5	V
I_I	Input Current @ Max. Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{OZH}	Off-State Output Current High Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V V_O = 2.7V				20	μA
I_{OZL}	Off-State Output Current Low Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V V_O = 0.4V				−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		11	21	mA
			Outputs Low		16	29	mA
			Outputs Disabled		20	31	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From	To	DM54ALS873B		DM74ALS873B		Units
					Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	Data	Any Q	2	17	2	14	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Data	Any Q	2	15	2	14	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		Enable	Any Q	8	29	8	22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Enable	Any Q	8	26	8	21	ns
t_{PZH}	Output Enable Time to High Level Output		Output Control	Any Q	4	22	4	18	ns
t_{PZL}	Output Enable Time to Low Level Output		Output Control	Any Q	4	23	4	18	ns
t_{PHZ}	Output Disable Time from High Level Output		Output Control	Any Q	2	12	2	10	ns
t_{PLZ}	Output Disable Time from Low Level Output		Output Control	Any Q	2	21	2	15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Clear	Any Q	6	24	6	20	ns

Note 1: See Section 1 for test waveforms and output load.

Function Table

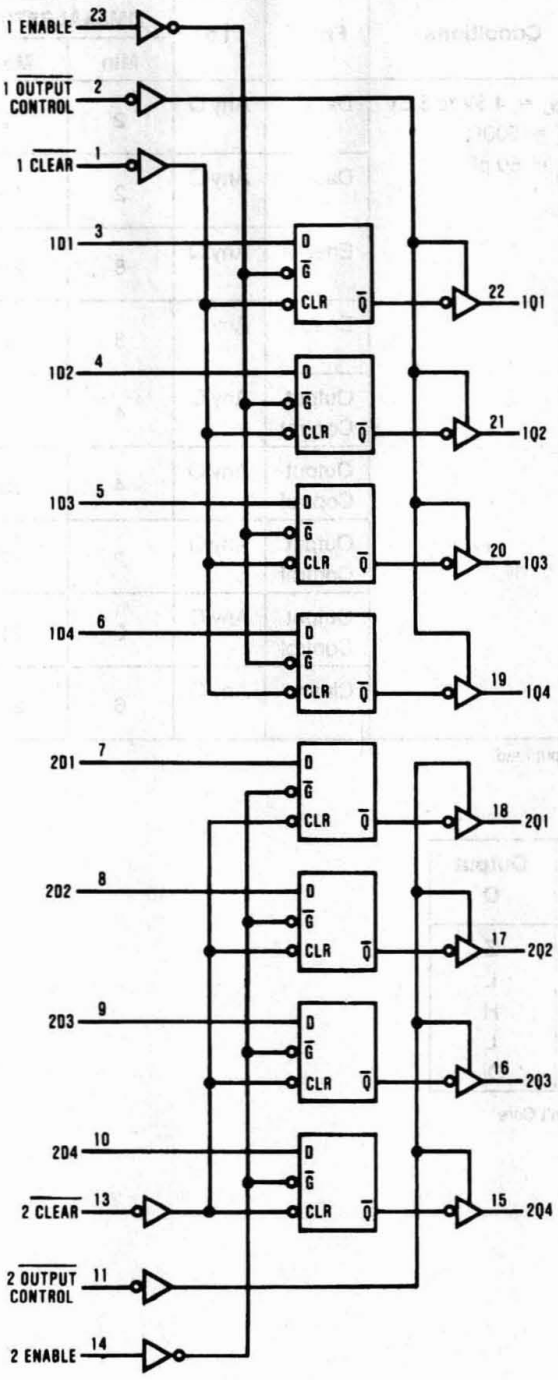
Inputs				Output Q
$\overline{CLR}$	D	EN	$\overline{OC}$	
X	X	X	H	Z
L	X	X	L	L
H	H	H	L	H
H	L	H	L	L
H	X	L	L	Q_0

L = Low State, H = High State, X = Don't Care

Z = High Impedance State

Q_0 = Previous Condition of Q

Logic Diagram



TL/F/6243–2

National Semiconductor Corporation

DM54ALS874B/DM74ALS874B Dual 4-Bit D-Type Edge-Triggered Flip-Flops with TRI-STATE® Outputs

General Description

These dual 4-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the ALS874B are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

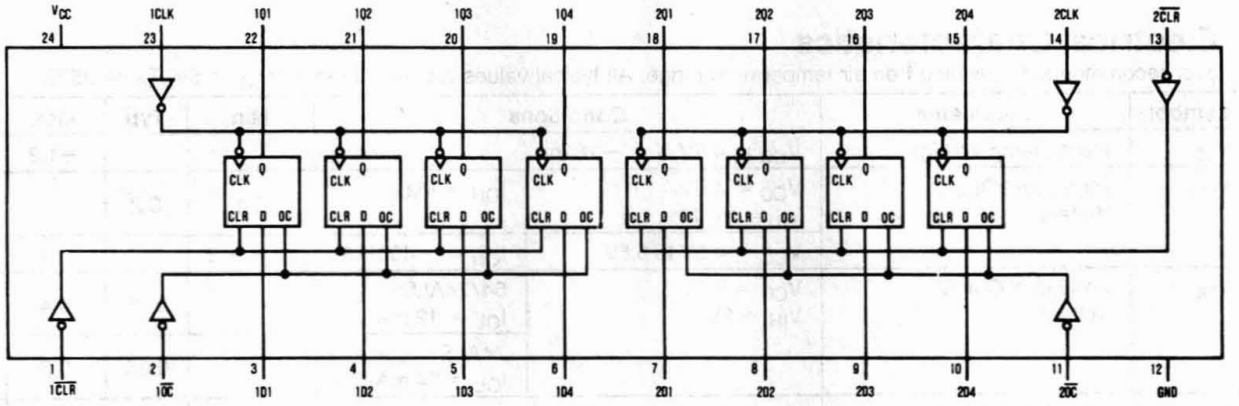
The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- TRI-STATE buffer-type outputs drive bus lines directly
- Space saving 300 mil wide package
- Asynchronous clear

Connection Diagram

Dual-In-Line Package



TL/F/6244–1

Order Number DM54ALS874BJ, DM74ALS874BWM or DM74ALS874BNT
See NS Package Number J24A, M24B or N24C

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Voltage Applied to Disabled Output	5.5V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54ALS874B			DM74ALS874B			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−1			−2.6	mA
I_{OL}	Low Level Output Current				12			24	mA
f_{CLK}	Clock Frequency		0		25	0		30	MHz
t_{WCLK}	Width of Clock Pulse	High	20			16.5			ns
		Low	20			16.5			ns
t_{WCLR}	Width of Clear Pulse	Low	10			10			ns
t_{SU}	Data Setup Time		15↑			15↑			ns
t_H	Data Hold Time		4↑			0↑			ns
t_{SU}	Clear Inactive		10			10			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V V_{IL} = V_{IL} Max	I_{OH} = Max	2.4	3.2		V
		V_{CC} = 4.5V to 5.5V	I_{OH} = −400 μA	V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V	54/74ALS I_{OL} = 12 mA		0.25	0.4	V
			74ALS I_{OL} = 24 mA		0.35	0.5	V
I_I	Input Current @Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{OZH}	Off-State Output Current High Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V V_O = 2.7V				20	μA
I_{OZL}	Off-State Output Current Low Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V V_O = 0.4V				−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		14	21	mA
			Outputs Low		19	30	mA
			Outputs Disabled		20	32	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

Symbol	Parameter	Conditions	From	To	DM54ALS874B		DM74ALS874B		Units
					Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF			25		30		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output		Clock	Any Q	4	15	4	14	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Clock	Any Q	4	15	4	14	ns
t_{PZH}	Output Enable Time to High Level Output		Output Control	Any Q	4	21	4	18	ns
t_{PZL}	Output Enable Time to Low Level Output		Output Control	Any Q	4	21	4	18	ns
t_{PHZ}	Output Disable Time from High Level Output		Output Control	Any Q	2	12	2	10	ns
t_{PLZ}	Output Disable Time from Low Level Output		Output Control	Any Q	3	15	3	12	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Clear	Any Q	5	20	5	17	ns

Note 1: See Section 1 for test waveforms and output load.

Function Table

Inputs				Output
$\overline{CLR}$	D	CLK	$\overline{OC}$	Q
X	X	X	H	Z
L	X	X	L	L
H	H	↑	L	H
H	L	↑	L	L
H	X	L	L	Q_0

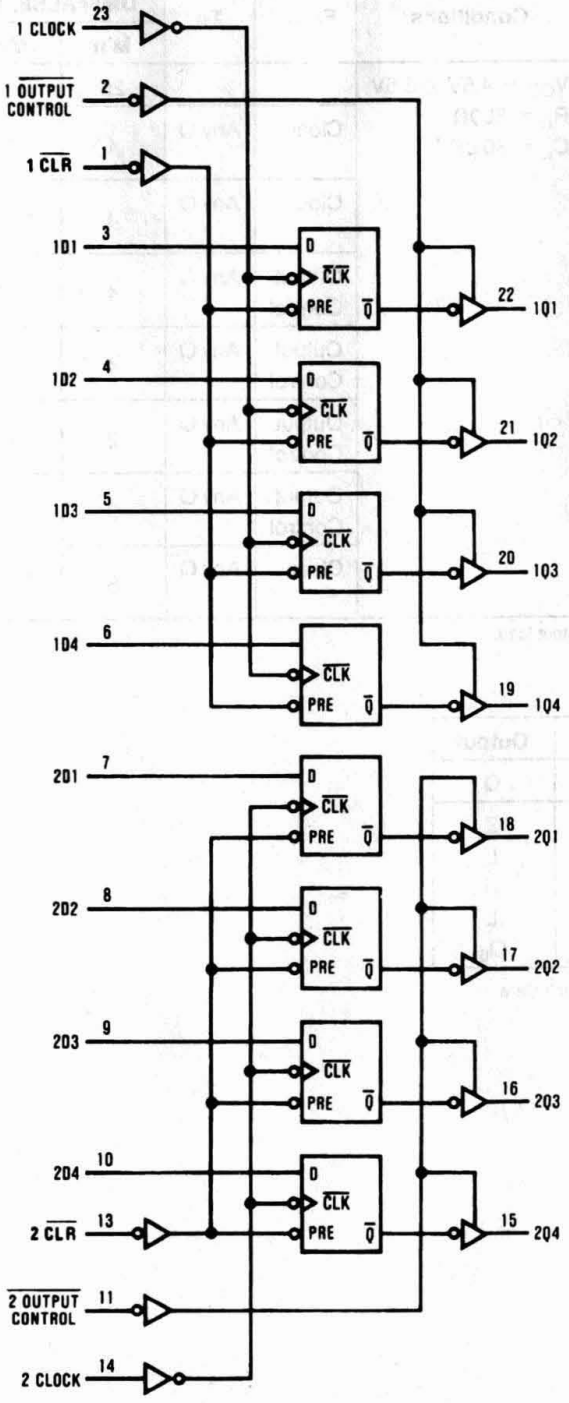
L = Low State, H = High State, X = Don't Care

↑ = Positive Edge Transition

Z = High Impedance State

Q_0 = Previous Condition of Q

Logic Diagram



TL/F/6244–2

National Semiconductor Corporation

DM54ALS876A/DM74ALS876A Dual 4-Bit D-Type Edge-Triggered Flip-Flops with TRI-STATE® Outputs

General Description

These inverting dual 4-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the ALS876A are edge-triggered inverting D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the complement of the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

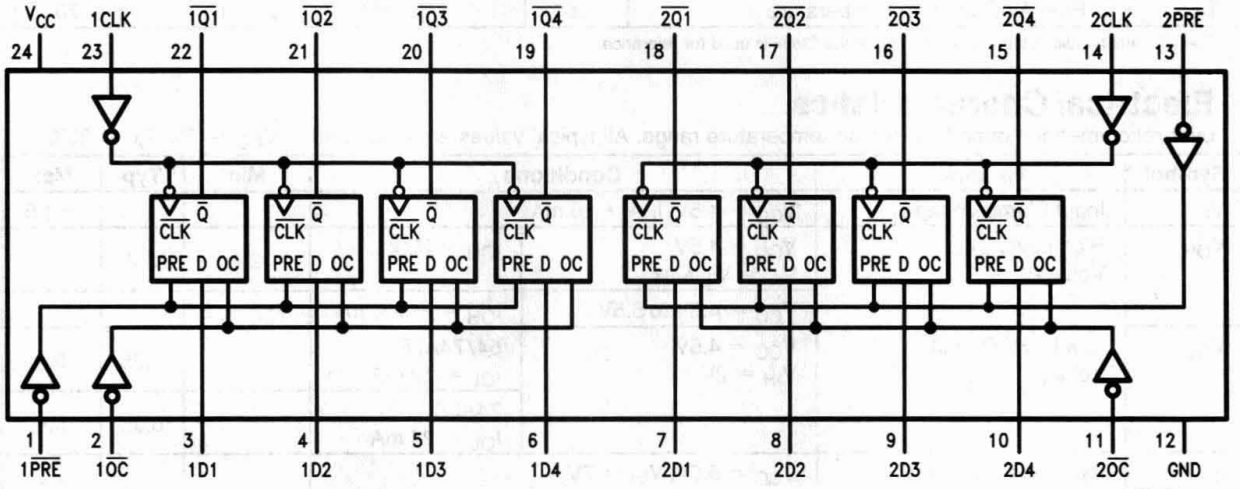
The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- TRI-STATE buffer-type outputs drive bus lines directly
- Space saving 300 mil wide package
- Asynchronous preset

Connection Diagram

Dual-In-Line Package



TL/F/6245–1

Order Number DM54ALS876AJ, DM74ALS876AWM or DM74ALS876ANT
See NS Package Number J24A, M24B or N24C

2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Voltage Applied to Disabled Output	5.5V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54ALS876A			DM74ALS876A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−1			−2.6	mA
I_{OL}	Low Level Output Current				12			24	mA
f_{CLK}	Clock Frequency		0		25	0		30	MHz
t_{WCLK}	Width of Clock Pulse	High	20			16.5			ns
		Low	20			16.5			ns
t_{WPRE}	Width of Preset Pulse	Low	10			10			ns
t_{SU}	Data Setup Time		15↑			15↑			ns
t_H	Data Hold Time		4↑			0↑			ns
t_{SU}	Preset Inactive		10↑			10↑			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, V_{IL} = V_{IL} Max	I_{OH} = Max	2.4	3.2		V
		V_{CC} = 4.5V to 5.5V	I_{OH} = −400 μA	V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, V_{IH} = 2V	54/74ALS I_{OL} = 12 mA		0.25	0.4	V
			74ALS I_{OL} = 24 mA		0.35	0.5	V
I_I	Input Current @ Max. Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{OZH}	Off-State Output Current High Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V, V_O = 2.7V				20	μA
I_{OZL}	Off-State Output Current Low Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V, V_O = 0.4V				−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		14	21	mA
			Outputs Low		18	29	mA
			Outputs Disabled		20	31	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From	To	DM54ALS876A		DM74ALS876A		Units
					Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF			25		30		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output		Clock	Any $\overline{Q}$	4	15	4	14	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Clock	Any $\overline{Q}$	4	15	4	14	ns
t_{PZH}	Output Enable Time to High Level Output		Output Control	Any $\overline{Q}$	4	21	4	18	ns
t_{PZL}	Output Enable Time to Low Level Output		Output Control	Any $\overline{Q}$	4	21	4	18	ns
t_{PHZ}	Output Disable Time from High Level Output		Output Control	Any $\overline{Q}$	2	12	2	10	ns
t_{PLZ}	Output Disable Time from Low Level Output		Output Control	Any $\overline{Q}$	3	15	3	13	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Preset	Any $\overline{Q}$	6	22	6	19	ns

Note 1: See Section 1 for test waveforms and output load.

Function Table

Inputs				Output
$\overline{PRE}$	D	CLK	$\overline{OC}$	$\overline{Q}$
X	X	X	H	Z
L	X	X	L	L
H	H	↑	L	L
H	L	↑	L	H
H	X	L	L	$\overline{Q}_0$

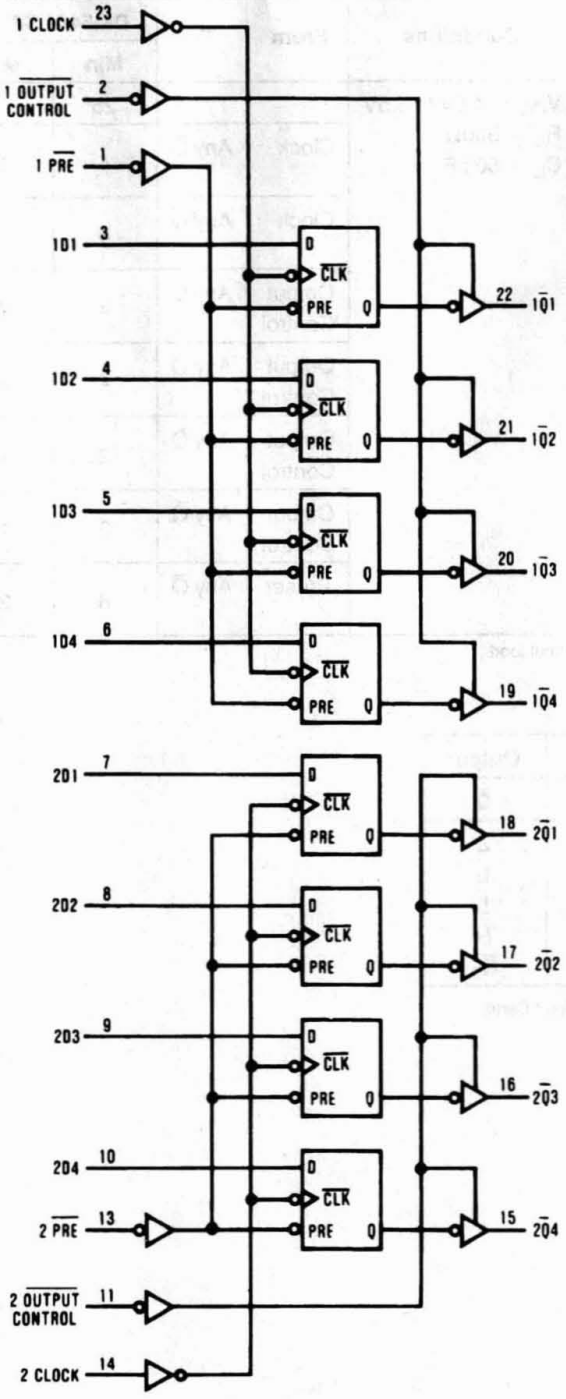
L = Low State, H = High State, X = Don't Care

↑ = Positive Edge Transition

Z = High Impedance State

$\overline{Q}_0$ = Previous Condition of $\overline{Q}$

Logic Diagram



TL/F/6245–2

National Semiconductor Corporation

DM54ALS880A/DM74ALS880A Dual 4-Bit D-Type Transparent Latches with TRI-STATE® Outputs

General Description

These dual 4-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight inverting latches of the ALS880A are transparent D-type latches. While the enable (G) is high the $\overline{Q}$ outputs will follow the complement of the data (D) inputs. When the enable is taken low the output will be latched at the complement of the level of the data that was set up.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

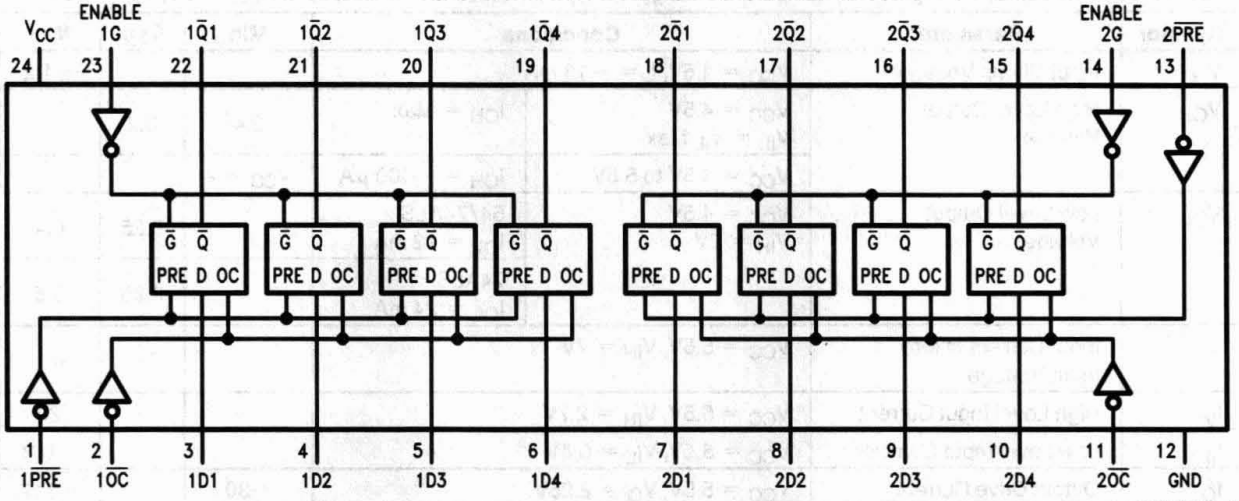
The output control does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- TRI-STATE buffer-type outputs drive bus lines directly
- Space saving 300 mil wide package

Connection Diagram

Dual-In-Line Package



TL/F/6248–1

Order Number DM54ALS880AJ, DM74ALS880AWM or DM74ALS880ANT
See NS Package Number J24A, M24B or N24C

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Voltage Applied to Disabled Output	5.5V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54ALS880A			DM74ALS880A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−1			−2.6	mA
I_{OL}	Low Level Output Current				12			24	mA
t_W	Pulse Width	Enable High	15			15			ns
		Preset Low	15			15			ns
t_{SU}	Data Setup Time		10↓			10↓			ns
t_H	Data Hold Time		10↓			10↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

The (↓) arrow indicates the negative edge of the enable is used for reference.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V V_{IL} = V_{IL} Max	I_{OH} = Max	2.4	3.2		V
		V_{CC} = 4.5V to 5.5V	I_{OH} = −400 μA	V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V	54/74ALS I_{OL} = 12 mA		0.25	0.4	V
			74ALS I_{OL} = 24 mA		0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.2	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{OZH}	Off-State Output Current High Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V V_O = 2.7V				20	μA
I_{OZL}	Off-State Output Current Low Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V V_O = 0.4V				−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		14	21	mA
			Outputs Low		19	29	mA
			Outputs Disabled		20	31	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From	To	DM54ALS880A		DM74ALS880A		Units
					Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	Data	Any $\overline{Q}$	3	23	3	20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Data	Any $\overline{Q}$	3	15	3	14	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		Enable	Any $\overline{Q}$	8	31	8	24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Enable	Any $\overline{Q}$	8	22	8	21	ns
t_{PZH}	Output Enable Time to High Level Output		Output Control	Any $\overline{Q}$	4	21	5	18	ns
t_{PZL}	Output Enable Time to Low Level Output		Output Control	Any $\overline{Q}$	4	21	5	18	ns
t_{PHZ}	Output Disable Time from High Level Output		Output Control	Any $\overline{Q}$	2	12	2	10	ns
t_{PLZ}	Output Disable Time from Low Level Output		Output Control	Any $\overline{Q}$	3	21	3	17	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Preset	Any $\overline{Q}$	6	24	6	21	ns

Note 1: See Section 1 for test waveforms and output load.

Function Table

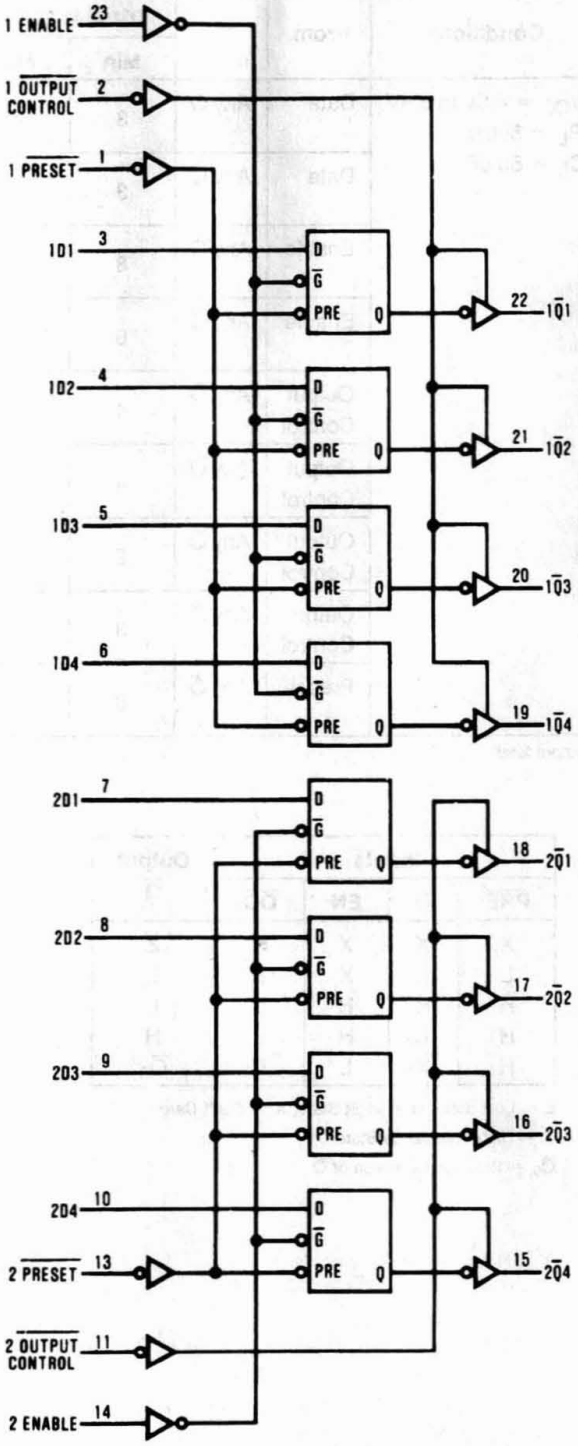
Inputs				Output
$\overline{PRE}$	D	EN	$\overline{OC}$	$\overline{Q}$
X	X	X	H	Z
L	X	X	L	L
H	H	H	L	L
H	L	H	L	H
H	X	L	L	$\overline{Q}_0$

L = Low State, H = High State, X = Don't Care

Z = High Impedance State

$\overline{Q}_0$ = Previous Condition of $\overline{Q}$

Logic Diagram



TL/F/6248–2

National Semiconductor Corporation

DM54ALS1000A/DM74ALS1000A Quadruple 2-Input NAND Buffers

General Description

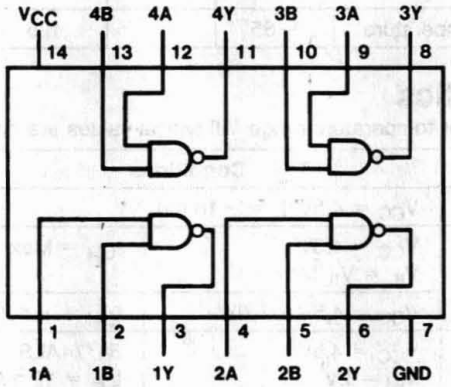
These devices contain four independent 2-input buffer/drivers, each of which performs the logic NAND function. The 'ALS1000A is a buffer/driver version of the 'ALS00A.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Improved line receiving characteristics

Connection Diagram

Dual-In-Line Package



TL/F/6249–1

Order Number DM54ALS1000AJ, DM74ALS1000AM or DM74ALS1000AN
See NS Package Number J14A, M14A or N14A

Function Table

$Y = \overline{AB}$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS1000A			DM74ALS1000A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, V_{IL} = V_{IL} Max	I_{OH} = Max	2.4	3.2		V
		V_{CC} = 4.5V to 5.5V	I_{OH} = −400 μA	V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, V_{IH} = 2V	54/74ALS I_{OL} = 12 mA		0.25	0.4	V
			74ALS I_{OL} = 24 mA		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = 5.5V, V_I = 0V			0.86	1.6	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = 5.5V, V_I = 4.5V			4.8	7.8	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	DM54ALS1000A		DM74ALS1000A		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V, R_L = 500Ω, C_L = 50 pF	2	10	2	8	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		2	10	2	7	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM54ALS1002A/DM74ALS1002A Quadruple 2-Input Positive-NOR Buffers

General Description

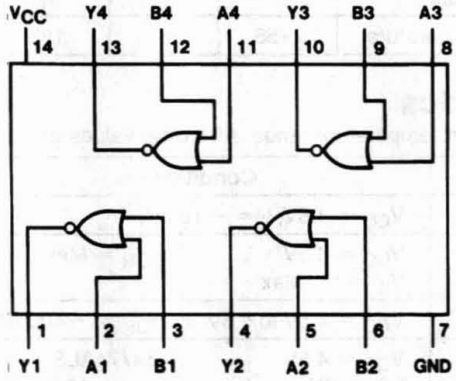
This device contains four independent 2-input buffers, each of which performs the logic NOR function. The 'ALS1002A is a buffer verision of the 'ALS02.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Improved line receiving characteristics

Connection Diagram

Dual-In-Line Package



TL/F/6250–1

Order Number DM54ALS1002AJ, DM74ALS1002AM or DM74ALS1002AN
See NS Package Number J14A, M14A or N14A

Function Table

$$Y = \overline{A + B}$$

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

H = High Logic Level

L = Low Logic Level

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS1002A			DM74ALS1002A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V V_{IL} = V_{IL} Max	I_{OH} = Max	2.4	3.2		V
		V_{CC} = 4.5V to 5.5V	I_{OH} = −400 μA	V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V	54/74ALS I_{OL} = 12 mA		0.25	0.4	V
			74ALS I_{OL} = 24 mA		0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = 5.5V, V_I = 0V			1.7	2.8	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = 5.5V, V_I = 4.5V			5.6	9	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	DM54ALS1002A		DM74ALS1002A		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	2	10	2	8	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		2	10	3	7	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM54ALS1003A/DM74ALS1003A Quadruple 2-Input NAND Buffers with Open-Collector Outputs

General Description

This device contains four independent 2-input buffers, each of which performs the logic NAND function. The outputs require an external pull-up resistor for proper logical operation. The 'ALS1003A is a buffer version of the 'ALS03A.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with LS TTL counterpart
- Improved line receiving characteristics

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

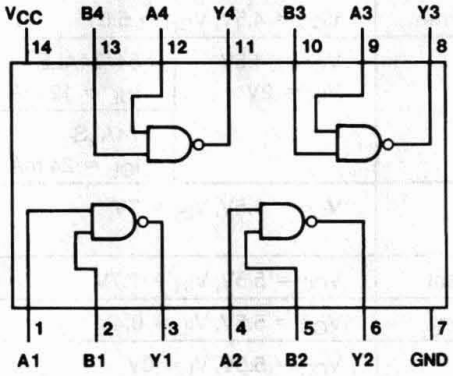
Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Connection Diagram

Dual-In-Line Package



TL/F/6251–1

Order Number DM54ALS1003AJ, DM74ALS1003AM or DM74ALS1003AN
See NS Package Number J14A, M14A or N14A

Function Table

$$Y = \overline{AB}$$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level

L = Low Logic Level

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Off State (High Level) Output Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS1003A			DM74ALS1003A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
I_{OH}	High Level Output Current	V_{CC} = 4.5V, V_{OH} = 5.5V				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, V_{IH} = 2V	54/74ALS I_{OL} = 12 mA		0.25	0.4	V
			74ALS I_{OL} = 24 mA		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = 5.5V, V_I = 0V			0.86	1.6	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = 5.5V, V_I = 4.5V			4.8	7.8	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	DM54ALS1003A		DM74ALS1003A		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V, R_L = 667Ω, C_L = 50 pF	10	40	10	33	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		2	18	2	12	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM54ALS1004/DM74ALS1004 Hex Inverting Drivers

General Description

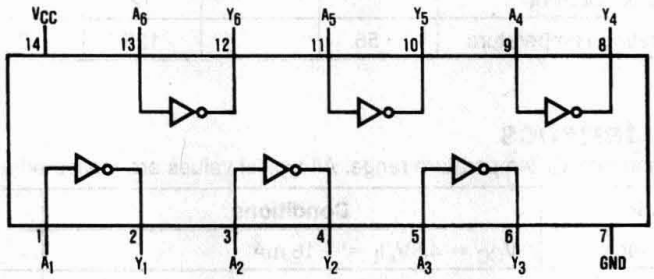
These devices contain six independent drivers, each of which performs the logic inverter/complement function. The 'ALS1004 is a driver version of the 'ALS04A.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky and low power Schottky TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts

Connection Diagram

Dual-In-Line Package



TL/F/6252–1

Order Number DM54ALS1004J or DM74ALS1004M, N
See NS Package Number J14A, M14A or N14A

Function Table

$$Y = \overline{A}$$

Input	Output
A	Y
L	H
H	L

H = High Logic Level

L = Low Logic Level

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS1004			DM74ALS1004			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA, V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
		I_{OH} = Max, V_{CC} = 4.5V		2			
		I_{OH} = −3 mA, V_{CC} = 4.5V		2.4			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 12 mA		0.25	0.4	V
			74ALS I_{OL} = 24 mA		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		0.84	3	mA
			Outputs Low		7	12	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	DM54ALS1004		DM74ALS1004		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	1	9	1	7	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		1	8	1	6	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM54ALS1005/DM74ALS1005 Hex Inverting Drivers with Open Collector Outputs

General Description

These devices contain six independent drivers, each of which performs the logic INVERT/Complement function. The outputs require external pull-up resistors for proper logical operation. The 'ALS1005 is a driver version of the 'ALS05A.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky and low power Schottky TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

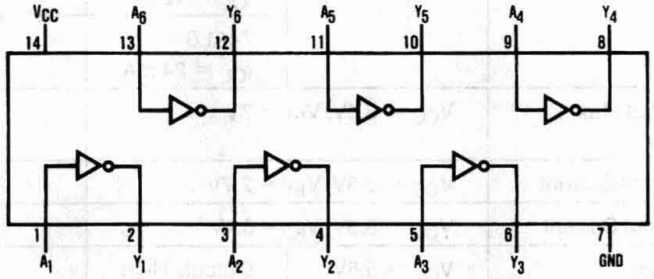
Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Connection Diagram

Dual-In-Line Package



TL/F/6253–1

Order Number DM54ALS1005J or DM74ALS1005M, N
See NS Package Number J14A, M14A or N14A

Function Table

$Y = \overline{A}$

Input A	Output Y
H	L
L	H

L = Low Logic Level

H = High Logic Level

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Off-State Output Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS1005			DM74ALS1005			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
I_{OH}	High Level Output Current	V_{CC} = 4.5V, V_{OH} = 5.5V				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 12 mA		0.25	0.4	V
			74ALS I_{OL} = 24 mA		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		0.9	3	mA
			Outputs Low		7	12	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	DM54ALS1005		DM74ALS1005		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V, R_L = 667Ω, C_L = 50 pF	5	35	5	30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		2	12	2	10	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM54ALS1008A/DM74ALS1008A Quadruple 2-Input AND Buffers

General Description

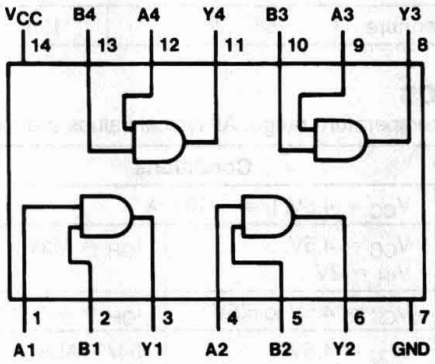
These devices contain four independent 2-input buffers, each of which performs the logic AND function. The 'ALS1008A is a buffer version of the 'ALS08.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Improved line receiving characteristics

Connection Diagram

Dual-In-Line Package



TL/F/6254–1

Order Number DM54ALS1008AJ, DM74ALS1008AM or DM74ALS1008AN
See NS Package Number J14A, M14A or N14A

Function Table

$Y = AB$

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

L = Low Logic Level
H = High Logic Level

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS1008A			DM74ALS1008A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V	I_{OH} = Max	2.4	3.2		V
		V_{CC} = 4.5V to 5.5V	I_{OH} = −400 μA	V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V	54/74ALS I_{OL} = 12 mA		0.25	0.4	V
			74ALS I_{OL} = 24 mA		0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = 5.5V, V_I = 0V			1.8	3	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = 5.5V, V_I = 4.5V			5.7	9.3	mA

Switching Characteristics

over recommended operating free air temperature range (Note 1).

Symbol	Parameter	Conditions	DM54ALS1008A		DM74ALS1008A		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	2	11	2	9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		3	11	3	9	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM54ALS1010A/DM74ALS1010A Triple 3-Input NAND Buffers

General Description

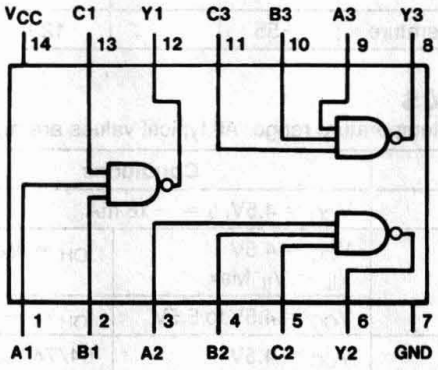
These devices contain three independent buffers, each of which performs the logic NAND function. The 'ALS1010A is a buffer version of the 'ALS10A.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Improved line receiving characteristics

Connection Diagram

Dual-In-Line Package



TL/F/6255–1

Order Number DM54ALS1010AJ, DM74ALS1010AM or DM74ALS1010AN
See NS Package Number J14A, M14A or N14A

Function Table

$$Y = \overline{ABC}$$

Inputs			Output
A	B	C	Y
L	X	X	H
X	L	X	H
X	X	L	H
H	H	H	L

L = Low Logic Level
H = High Logic Level
X = Either Low or High Logic Level

2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS1010A			DM74ALS1010A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V V_{IL} = V_{IL} Max	I_{OH} = Max	2.4	3.2		V
		V_{CC} = 4.5V to 5.5V	I_{OH} = −400 μA	V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V	54/74ALS I_{OL} = 12 mA		0.25	0.4	V
			74ALS I_{OL} = 24 mA		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = 5.5V, V_I = 0V			0.65	1.2	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = 5.5V, V_I = 4.5V			3.6	5.8	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	DM54ALS1010A		DM74ALS1010A		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	2	12	2	8	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		2	12	2	8	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM54ALS1011A/DM74ALS1011A Triple 3-Input AND Buffers

General Description

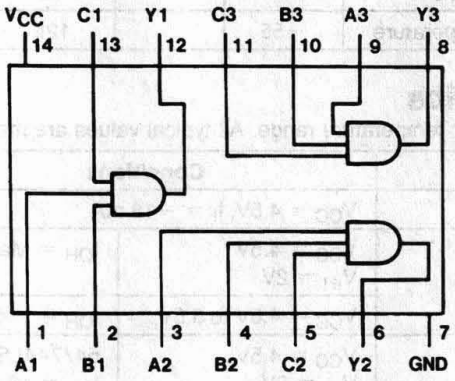
These devices contain three independent buffers, each of which performs the logic AND function. The 'ALS1011A is a buffer version of the 'ALS11A.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Improved line receiving characteristics

Connection Diagram

Dual-In-Line Package



TL/F/6256–1

Order Number DM54ALS1011AJ, DM74ALS1011AM or DM74ALS1011AN
See NS Package Number J14A, M14A or N14A

Function Table

$Y = ABC$

Inputs			Output
A	B	C	Y
L	X	X	L
X	L	X	L
X	X	L	L
H	H	H	H

L = Low Logic Level
H = High Logic Level
X = Either Low or High Logic Level

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS1011A			DM74ALS1011A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V	I_{OH} = Max	2.4	3.2		V
		V_{CC} = 4.5V to 5.5V	I_{OH} = −400 μA	V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V	54/74ALS I_{OL} = 12 mA		0.25	0.4	V
			74ALS I_{OL} = 24 mA		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = 5.5V, V_I = 0V			1.4	2.3	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = 5.5V, V_I = 4.5V			4.3	7	mA

Switching Characteristics

over recommended operating free air temperature range (Note 1).

Symbol	Parameter	Conditions	DM54ALS1011A		DM74ALS1011A		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	2	12	2	10	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		3	11	3	9	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM54ALS1020A/DM74ALS1020A Dual 4-Input NAND Buffers

General Description

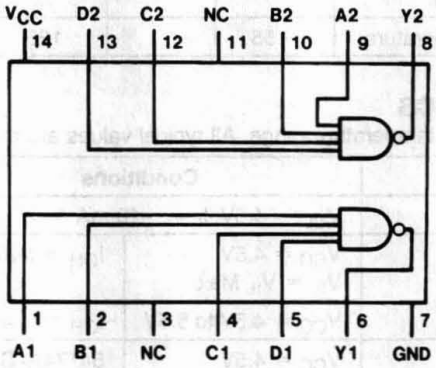
These devices contain two independent 4-input buffers, each of which performs the logic NAND function. The 'ALS1020A is a buffer version of the 'ALS20A.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Improved line receiving characteristics

Connection Diagram

Dual-In-Line Package



TL/F/6257–1

Order Number DM54ALS1020AJ, DM74ALS1020AM or DM74ALS1020AN
See NS Package Number J14A, M14A or N14A

Function Table

$$Y = \overline{ABCD}$$

Inputs				Output
A	B	C	D	Y
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

L = Low Logic Level
H = High Logic Level
X = Either Low or High Logic Level

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS1020A			DM74ALS1020A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V V_{IL} = V_{IL} Max	I_{OH} = Max	2.4	3.2		V
		V_{CC} = 4.5V to 5.5V	I_{OH} = −400 μA	V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V	54/74ALS I_{OL} = 12 mA		0.25	0.4	V
			74ALS I_{OL} = 24 mA		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = 5.5V, V_I = 0V			0.5	0.8	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = 5.5V, V_I = 4.5V			2.4	3.9	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	DM54ALS1020A		DM74ALS1020A		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	2	10	2	8	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		2	10	2	7	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM54ALS1032A/DM74ALS1032A Quadruple 2-Input OR Buffers

General Description

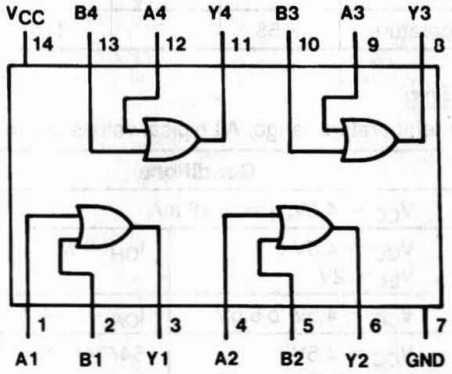
These devices contain four independent buffers, each of which performs the logic OR function. The 'ALS1032A is a buffer version of the 'ALS32.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Improved line receiving characteristics

Connection Diagram

Dual-In-Line Package



TL/F/6258–1

Order Number DM54ALS1032AJ, DM74ALS1032AM or DM74ALS1032AN
See NS Package Number J14A, M14A or N14A

Function Table

$Y = A + B$

Inputs		Output
A	B	Y
L	L	L
H	X	H
X	H	H

L = Low Logic Level
H = High Logic Level
X = Either Low or High Logic Level

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS1032A			DM74ALS1032A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, V_{IH} = 2V	I_{OH} = Max	2.4	3.2		V
		V_{CC} = 4.5V to 5.5V	I_{OH} = −400 μA	V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, V_{IH} = 0.8V	54/74ALS I_{OL} = 12 mA		0.25	0.4	V
			74ALS I_{OL} = 24 mA		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = 5.5V, V_I = 4.5V			2.5	5	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = 5.5V, V_I = 0V			6.6	10.6	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	DM54ALS1032A		DM74ALS1032A		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V, R_L = 500Ω, C_L = 50 pF	2	12	2	9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		3	15	3	12	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM54ALS1034/DM74ALS1034 Hex Non-Inverting Drivers

General Description

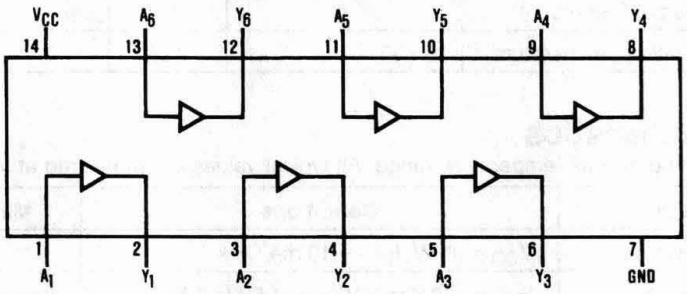
These devices contain six independent drivers, each of which performs the logic identity function.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky and Low Power Schottky TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts

Connection Diagram

Dual-In-Line Package



TL/F/6259–1

Order Number DM54ALS1034J or DM74ALS1034M, N
See NS Package Number J14A, M14A or N14A

Function Table

$Y = A$

Input A	Output Y
H	H
L	L

L = Low Logic Level

H = High Logic Level

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS1034			DM74ALS1034			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA, V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
		I_{OH} = Max, V_{CC} = 4.5V		2			V
		I_{OH} = −3 mA, V_{CC} = 4.5V		2.4			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 12 mA		0.25	0.4	V
			74ALS I_{OL} = 24 mA		0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_I = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		3	6	mA
			Outputs Low		8	14	mA

Switching Characteristics over recommended operating free air temperature range (Note 1).

Symbol	Parameter	Conditions	DM54ALS1034		DM74ALS1034		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	1	11	1	8	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		1	13	1	8	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM54ALS1035/DM74ALS1035 Hex Non-Inverting Drivers with Open Collector Outputs

General Description

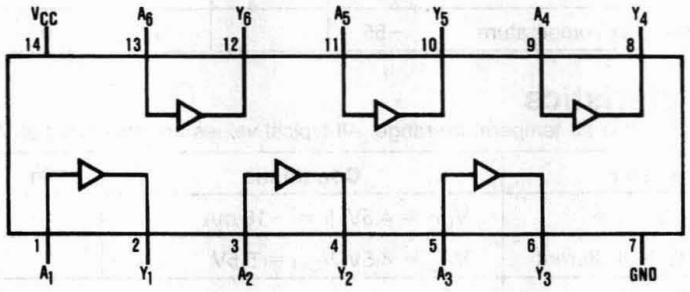
These devices contain six independent drivers, each of which performs the logic identity function. The outputs require an external pull-up resistor for proper logical operation.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky and low power Schottky TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts

Connection Diagram

Dual-In-Line Package



TL/F/6260–1

Order Number DM54ALS1035J or DM74ALS1035M, N
See NS Package Number J14A, M14A or N14A

Function Table

$Y = A$

Input A	Output Y
L	L
H	H

L = Low Logic Level

H = High Logic Level

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Off-State Output Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS1035			DM74ALS1035			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5	V
I_{OH}	High Level Output Current	V_{CC} = 4.5V, V_{OH} = 5.5V				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 12 mA		0.25	0.4	V
			74ALS I_{OL} = 24 mA		0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		3	6	mA
			Outputs Low		8	14	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	DM54ALS1035		DM74ALS1035		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 680Ω C_L = 50 pF	5	35	5	30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		2	14	2	12	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

PRELIMINARY

DM54ALS1240/DM74ALS1240/ DM54ALS1241A/DM74ALS1241A Octal TRI-STATE® Bus Drivers

General Description

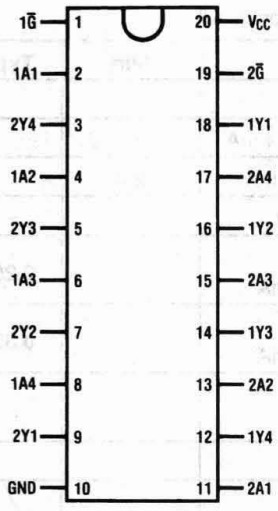
These octal TRI-STATE bus drivers are designed to provide the designer with flexibility in implementing a bus interface with memory, microprocessor, or communication systems, and are low power dissipation versions of the 'ALS240 and 'ALS241. The output TRI-STATE gating control is organized into two separate groups of four buffers. The 'ALS1240 control inputs symmetrically enable the respective outputs when set logic low, while the 'ALS1241A has complementary enable gating. The TRI-STATE circuitry contains a feature that maintains the buffer outputs in TRI-STATE (high impedance state) during power supply ramp-up or ramp-down. This eliminates bus glitching problems that arise during power-up and power-down.

Features

- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Switching response specified into 500Ω and 50 pF load
- Switching response specifications guaranteed over full temperature and V_{CC} supply range
- PNP input design reduces input loading
- Low power dissipation version of the DM54/74ALS240, 241
- Low level drive current: 54ALS = 8 mA, 74ALS = 16 mA

Connection Diagrams

Dual-In-Line Package

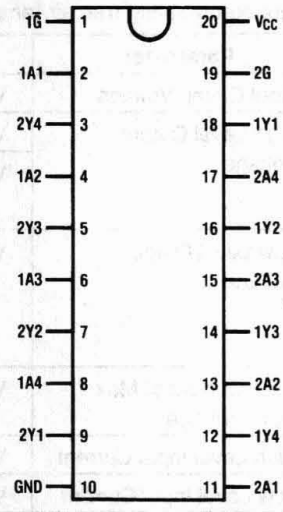


TL/F/6261–1

Top View

Order Number DM54ALS1240J, DM74ALS1240WM or DM74ALS1240N
See NS Package Number J20A, M20B or N20A

Dual-In-Line Package



TL/F/6261–2

Top View

Order Number DM54ALS1241AJ, DM74ALS1241AWM or DM74ALS1241AN
See NS Package Number J20A, M20B or N20A

Function Tables

'ALS1240

Input		Output
$\overline{G}$	A	Y
L	L	H
L	H	L
H	X	Z

'ALS1241A

Input		Output
2G	2A	Y
H	L	L
H	H	H
L	X	Z

'ALS1241A

Input		Output
1G	1A	Y
L	L	L
L	H	H
H	X	Z

H = High Level Logic State L = Low Level Logic State X = Don't Care (Either Low or High Level Logic State) Z = High Impedance (Off) State

This document contains information on a product under development. NSC reserves the right to change or discontinue this product without notice.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Voltage Applied to Disabled Output	5.5V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS1240 DM54ALS1241A			DM74ALS1240 DM74ALS1241A			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			8			16	mA
T_A	Operating Free Air Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise specified)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V	I_{OH} = −0.4 mA	V_{CC} − 2			V
		V_{CC} = 4.5V	I_{OH} = −3 mA	2.4			V
			I_{OH} = Max	2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	54/74ALS I_{OL} = 12 mA		0.25	0.4	V
			74ALS I_{OL} = 24 mA		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{OZH}	High Level TRI-STATE Output Current	V_{CC} = 5.5V, V_O = 2.7V				20	μA
I_{OZL}	Low Level TRI-STATE Output Current	V_{CC} = 5.5V, V_O = 0.4V				−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V, ALS1240 Outputs High			5	8	mA
		Outputs Low			8	14	mA
		Outputs TRI-STATE			8	13	mA
		V_{CC} = 5.5V, ALS1241 Outputs High			7		mA
		Outputs Low			10		mA
		Outputs TRI-STATE			11		mA

'ALS1240 Switching Characteristics

over recommended operating free air temperature range (see Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input)	To (Output)	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R1 = 500Ω, R2 = 500Ω, T_A = Min to Max				Units
				DM54ALS1240		DM74ALS1240		
				Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	A	Y	2	16	2	13	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			2	16	2	13	ns
t_{PZH}	Output Enable Time to High Level Output	$\overline{G}$	Y	4	23	4	20	ns
t_{PZL}	Output Enable Time to Low Level Output			6	28	6	22	ns
t_{PHZ}	Output Disable Time from High Level Output	$\overline{G}$	Y	2	12	2	10	ns
t_{PLZ}	Output Disable Time from Low Level Output			3	18	3	13	ns

'ALS1241A Switching Characteristics

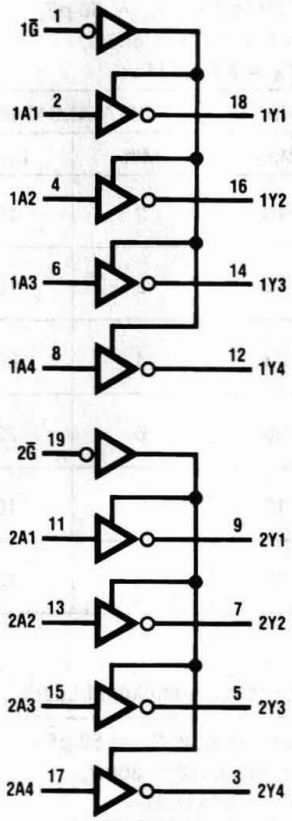
over recommended operating free-air temperature range (see Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input)	To (Output)	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R1 = 500Ω, R2 = 500Ω, T_A = Min to Max				Units
				DM54ALS1241A		DM74ALS1241A		
				Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	A	Y					ns
t_{PHL}	Propagation Delay Time High to Low Level Output							ns
t_{PZH}	Output Enable Time to High Level Output	$\overline{G}$ or G	Y					ns
t_{PZL}	Output Enable Time to Low Level Output							ns
t_{PHZ}	Output Disable Time from High Level Output	$\overline{G}$ or G	Y					ns
t_{PLZ}	Output Disable Time from Low Level Output							ns

2

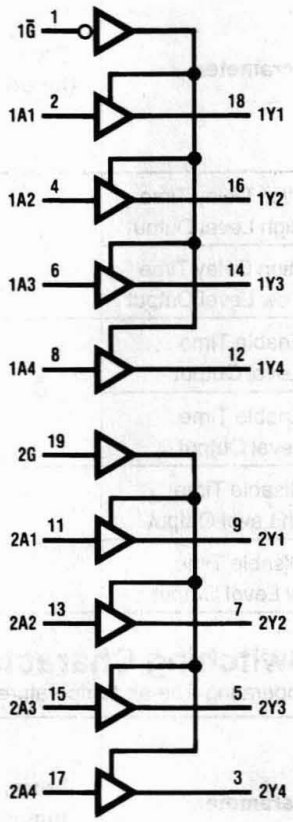
Logic Diagrams

DM54/74ALS1240



TL/F/6261–3

DM54/74ALS1241A



TL/F/6261–4

National Semiconductor Corporation

PRELIMINARY

DM54ALS1242/DM74ALS1242/ DM54ALS1243A/DM74ALS1243A Quad Bidirectional Bus Drivers

General Description

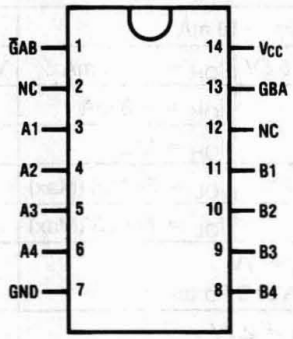
These octal TRI-STATE® bus drivers are designed to provide the designer with flexibility in implementing a bus interface with memory, microprocessor, or communication systems, and are low power dissipation versions of the 'ALS242 and 'ALS243. The 'ALS1242 has inverting buffers, while the 'ALS1243A has non-inverting buffers. The direction enable gating is configured with separate control over either buffer direction and the two control buffers are complementary. Connecting these control inputs to one common line implements single line direction control, while individual control can put both buffer directions into TRI-STATE simultaneously (disabled state) or put both buffer directions into the active state (data latch state). The TRI-STATE circuitry contains a feature that maintains the buffer outputs in TRI-STATE (high impedance state) during power supply ramp-up or ramp-down. This eliminates bus glitching problems that arise during power-up and power-down.

Features

- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Switching response specified into 500Ω and 50 pF load
- Switching response specifications guaranteed over full temperature and V_{CC} supply range
- PNP input design reduces input loading
- Low power dissipation version of the DM54/74ALS242, 243
- Low level drive current: 54ALS = 8 mA, 74ALS = 16 mA

Connection Diagram

Dual-In-Line Package



TL/F/6262–1

Top View

Order Number DM54ALS1242J, DM54ALS1243AJ, DM74ALS1242M, DM74ALS1243AM, DM74ALS1242N or DM74ALS1243AN
See NS Package Number J14A, M14A or N14A

Function Table

Inputs		ALS1242A	ALS1243A
$\overline{G}AB$	GBA		
L	L	$\overline{A}$ to B	A to B
H	H	$\overline{B}$ to A	B to A
H	L	Isolation	Isolation
L	H	Latch A and B ($A = \overline{B}$)	Latch A and B ($A = B$)

This document contains information on a product under development. NSC reserves the right to change or discontinue this product without notice.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V_{CC}	7V
Input Voltage	
Dedicated Inputs	7V
I/O Ports	5.5V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS1242 DM54ALS1243A			DM74ALS1242 DM74ALS1243A			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			8			16	mA
T_A	Operating Free-Air Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free-air temperature (unless otherwise specified)

Symbol	Parameter	Conditions		DM54ALS1242 DM54ALS1243A			DM74ALS1242 DM74ALS1243A			Units
				Min	Typ	Max	Min	Typ	Max	
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2			−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = 4.5V	I_{OH} = −3 mA	2.4			2.4			V
			I_{OH} = Max	2			2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	I_{OL} = 54ALS (Max)		0.25	0.4		0.25	0.4	V
			I_{OL} = 74ALS (Max)		—	—		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_I = 7V (V_I = 5.5V for A or B Ports)				0.1			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_I = 2.7V				20			20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1			−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V, ALS1242 Active Outputs High			8	14		8	12	mA
		Active Outputs Low			10	17		10	15	mA
		Outputs TRI-STATE			9	16		9	14	mA
		V_{CC} = 5.5V, ALS1243 Active Outputs High			9			9		mA
		Active Outputs Low			10			10		mA
		Outputs TRI-STATE			11			11		mA

'ALS1242 Switching Characteristics

over recommended operating free-air temperature range (see Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R1 = 500Ω, R2 = 500Ω, T_A = Min to Max				Units
			54ALS1242		74ALS1242		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	A or B to B or A	2	14	2	12	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A or B to B or A	2	12	2	10	ns
t_{PZH}	Output Enable Time to High Level Output	$\overline{G}$AB to B	4	20	4	17	ns
t_{PZL}	Output Enable Time to Low Level Output	$\overline{G}$AB to B	5	23	5	21	ns
t_{PHZ}	Output Disable Time from High Level Output	$\overline{G}$AB to B	2	12	2	10	ns
t_{PLZ}	Output Disable Time from Low Level Output	$\overline{G}$AB to B	2	12	2	10	ns
t_{PZH}	Output Enable Time to High Level Output	GBA to A	5	23	5	20	ns
t_{PZL}	Output Enable Time to Low Level Output	GBA to A	6	25	6	23	ns
t_{PHZ}	Output Disable Time from High Level Output	GBA to A	2	12	2	10	ns
t_{PLZ}	Output Disable Time from Low Level Output	GBA to A	2	15	2	12	ns

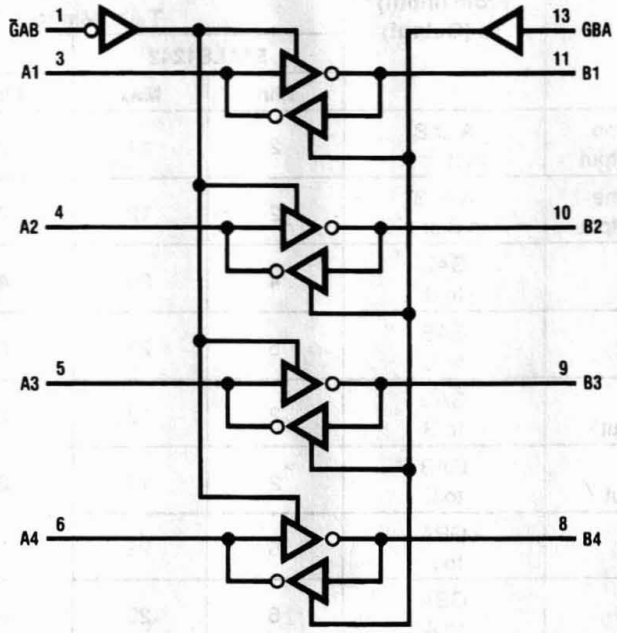
'ALS1243A Switching Characteristics

over recommended operating free-air temperature range (see Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R1 = 500Ω, R2 = 500Ω, T_A = Min to Max				Units
			54ALS1243A		74ALS1243A		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	A or B to B or A					ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A or B to B or A					ns
t_{PZH}	Output Enable Time to High Level Output	$\overline{G}$AB to B					ns
t_{PZL}	Output Enable Time to Low Level Output	$\overline{G}$AB to B					ns
t_{PHZ}	Output Disable Time from High Level Output	$\overline{G}$AB to B					ns
t_{PLZ}	Output Disable Time from Low Level Output	$\overline{G}$AB to B					ns
t_{PZH}	Output Enable Time to High Level Output	GBA to A					ns
t_{PZL}	Output Enable Time to Low Level Output	GBA to A					ns
t_{PHZ}	Output Disable Time from High Level Output	GBA to A					ns
t_{PLZ}	Output Disable Time from Low Level Output	GBA to A					ns

Logic Diagrams

DM54/74ALS1242B



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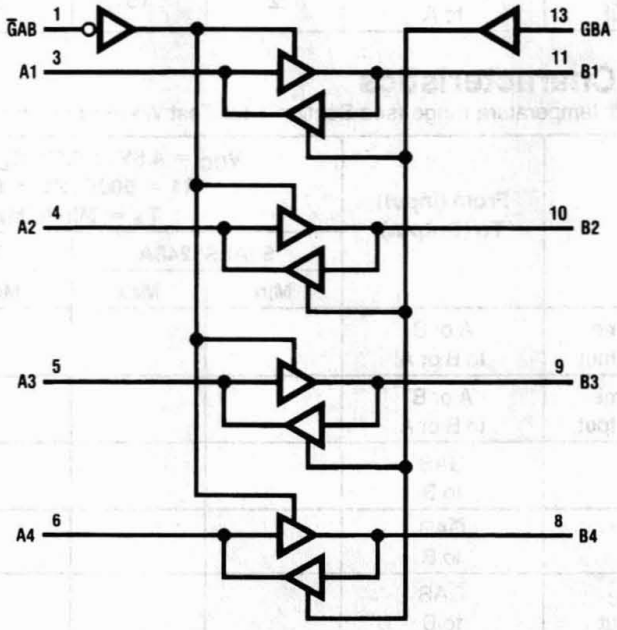
DM54/74ALS1243B



TL/F/6262–3

National Semiconductor Corporation

DM54ALS1244A/DM74ALS1244A Octal TRI-STATE® Bus Driver

General Description

This octal TRI-STATE bus driver is designed to provide the designer with flexibility in implementing a bus interface with memory, microprocessor, or communication systems, and is a low power dissipation version of the 'ALS244. The output TRI-STATE gating control is organized into two separate groups of four buffers, and both control inputs enable the respective outputs when set logic low. The TRI-STATE circuitry contains a feature that maintains the buffer outputs in TRI-STATE (high impedance state) during power supply ramp-up or ramp-down. This eliminates bus glitching problems that arise during power-up and power-down.

Features

- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Switching response specified into 500Ω and 50 pF load
- Switching response specifications guaranteed over full temperature and V_{CC} supply range
- PNP input design reduces input loading
- Low power dissipation version of the DM54/74ALS244A
- Low level drive current: 54ALS = 8 mA, 74ALS = 16 mA

Connection Diagram

Dual-In-Line Package

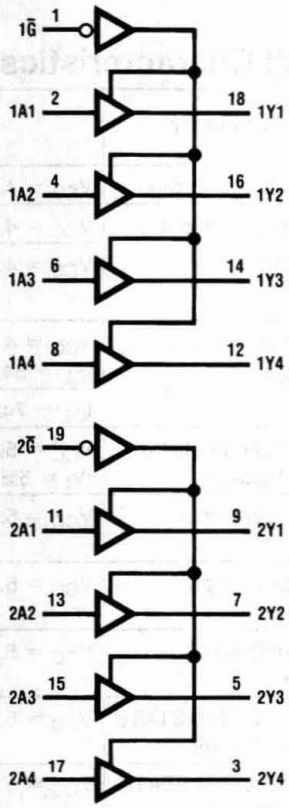
TL/F/6263–1

Top View

Order Number DM54ALS1244AJ, DM74ALS1244AWM or DM74ALS1244AN

See NS Package Number J20A, M20B or N20A

Logic Diagram



TL/F/6263–2

Function Table

Enable Input $1\overline{G}$ or $2\overline{G}$	Data Buffer Outputs
L	Active
H	TRI-STATE

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V_{CC}	7V
Input Voltage	7V
Voltage Applied to Disabled Output	5.5V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS1244A			DM74ALS1244A			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			8			16	mA
T_A	Operating Free-Air Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free-air temperature (unless otherwise specified)

Symbol	Parameter	Conditions		DM54ALS1244A			DM74ALS1244A			Units
				Min	Typ	Max	Min	Typ	Max	
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = 4.5V	I_{OH} = −3 mA	2.4			2.4			V
			I_{OH} = Max	2			2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 54ALS (Max)			0.25	0.4		0.25	0.4	V
		I_{OL} = 74ALS (Max)			—	—		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_I = 7V (V_I = 5.5V for A or B Ports)				0.1			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_I = 2.7V				20			20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.1			−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	−30		−112	mA
I_{OZH}	High Level TRI-STATE Output Current	V_{CC} = 5.5V, V_O = 2.7V				20			20	μA
I_{OZL}	Low Level TRI-STATE Output Current	V_{CC} = 5.5V, V_O = 0.4V				−20			−20	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs High			6	15		6	11	mA
		Outputs Low			10	20		10	17	mA
		Outputs TRI-STATE			11	25		11	20	mA

Switching Characteristics over recommended operating free-air temperature range

Symbol	Parameter	From (Input)	To (Output)	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R1 = 500Ω, R2 = 500Ω, T_A = Min to Max				Units
				54ALS1244A		74ALS1244A		
				Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	A	Y	3	21	3	14	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			3	16	3	14	ns
t_{PZH}	Output Enable Time to High Level Output	$\overline{G}$	Y	6	28	6	22	ns
t_{PZL}	Output Enable Time to Low Level Output			6	26	6	22	ns
t_{PHZ}	Output Disable Time from High Level Output	$\overline{G}$	Y	2	15	2	10	ns
t_{PLZ}	Output Disable Time from Low Level Output			3	25	3	13	ns

National Semiconductor Corporation

DM54ALS1245A/DM74ALS1245A TRI-STATE® Bus Transceivers

General Description

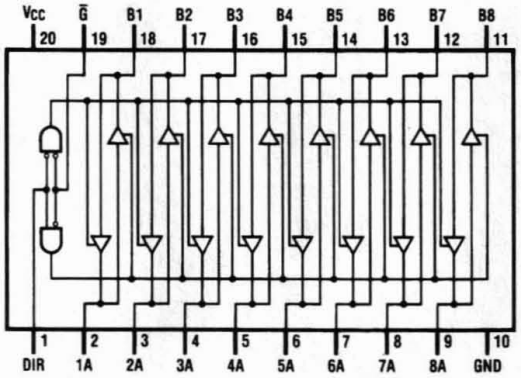
This advanced low power Schottky device contains 8 pairs of TRI-STATE logic elements configured as octal bus transceivers. This circuit is designed for use in memory, microprocessor systems and in asynchronous bidirectional data buses. Two way communication between buses is controlled by the (DIR) input. Data either transmits from the A bus to the B bus or from the B bus to the A bus. Both the driver and receiver outputs can be disabled via the ($\overline{G}$) enable input which causes outputs to enter the high impedance mode, so that the buses are effectively isolated. The TRI-STATE circuitry also contains a protection feature that prevents the buffer from glitching the bus during power-up or power-down.

Features

- Low power version of ALS245A
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Low output impedance to drive terminated transmission lines to 133Ω
- Switching response specified into 500Ω/50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range

Connection Diagram

Dual-In-Line Package



TL/F/8438–1

Order Number DM54ALS1245AJ, DM74ALS1245AWM or DM74ALS1245AN
See NS Package Number J20A, M20B or N20A

Function Table

Control Inputs		Operation
$\overline{G}$	DIR	
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	Hi-Z

L = Low Logic Level, H = High Logic Level

X = Either Low or High Logic Level

Hi-Z = High Impedance (off) State

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V_{CC}	7V
Input Voltage	
Control Inputs	7V
I/O Ports	5.5V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

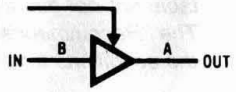
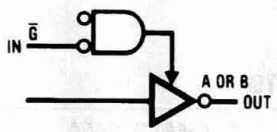
Symbol	Parameter	DM54ALS1245A			DM74ALS1245A			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			8			16	mA
T_A	Operating Free Air Temperature Range	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		DM54ALS1245A			DM74ALS1245A			Units
				Min	Typ	Max	Min	Typ	Max	
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18 mA				−1.5			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, I_{OH} = −3 mA		2.4	3.2		2.4	3.2		V
		V_{CC} = 4.5V, I_{OH} = Max		2	2.3		2	2.3		V
		I_{OH} = −0.4 mA, V_{OL} = 4.5V to 5.5V		V_{CC} − 2			V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	I_{OL} = 8 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 16 mA					0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IN} = 7V (V_{IN} = 5.5V for A or B Ports)				0.1			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IN} = 2.7V				20			20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V				−0.1			−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		21	33		21	30	mA
			Outputs Low		23	36		23	33	mA
			TRI-STATE		25	40		25	36	mA

Switching Characteristics over recommended operating free air temperature range (Notes 1 and 2)

Symbol	Parameter	Circuit Configuration	DM54ALS1245A		DM74ALS1245A		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		2	19	2	13	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		2	15	2	13	ns
t_{PZL}	Output Enable Time to Low Level Output		8	29	8	25	ns
t_{PZH}	Output Enable Time to High Level Output		8	30	8	25	ns
t_{PLZ}	Output Disable Time from Low Level Output		3	30	3	18	ns
t_{PHZ}	Output Disable Time from High Level Output		2	14	2	12	ns

Note 1: See Section 1 for test waveforms and output load.

Note 2: Switching characteristic conditions are V_{CC} = 4.5V to 5.5V, R_L = 500Ω, C_L = 50 pF.

National Semiconductor Corporation

PRELIMINARY

DM54ALS1645A/DM74ALS1645A Octal TRI-STATE® Bus Transceivers

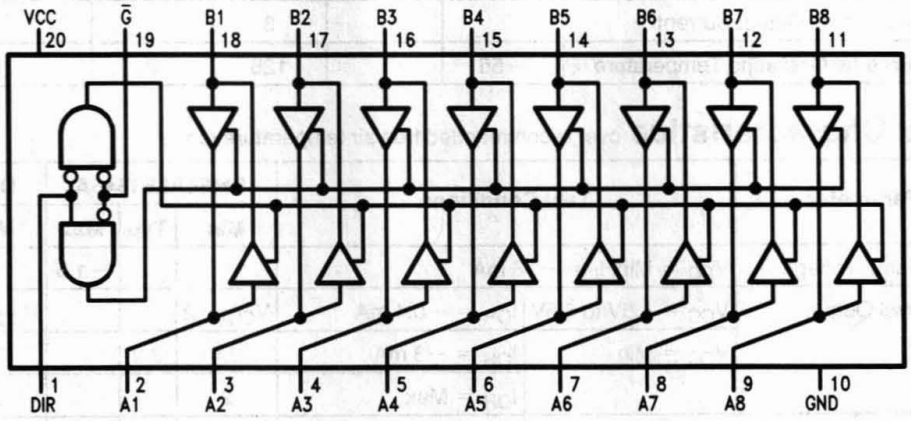
General Description

This device contains eight pairs of TRI-STATE logic elements configured as octal bus transceivers. This device is designed for use in memory, microprocessor systems and in asynchronous bidirectional data buses. Two way communication between buses is controlled by the direction (DIR) input. Data either transmits from the A bus to the B bus or from the B bus to the A bus. Both the driver and receiver outputs can be disabled by the enable (G) input which causes outputs to enter the high impedance mode, so that the buses are effectively isolated.

Features

- Low power version of the ALS645A
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- PNP input design reduces input loading
- Low output impedance to drive terminated transmission lines to 133Ω
- Switching specifications guaranteed over the full temperature and V_{CC} range

Connection Diagram



TL/F/9164–1

Order Number DM54ALS1645AJ, DM74ALS1645AWM or DM74ALS1645AN
See NS Package Number J20A, M20A or N20A

Function Table

Control Inputs		Operation
$\overline{G}$	DIR	
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	Hi-Z

L = Low Logic Level
H = High Logic Level
X = Don't Care (Either Low or High Logic Level)
Hi-Z = High Impedance

2

This document contains information on a product under development. NSC reserves the right to change or discontinue this product without notice.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	
Control Inputs	7V
I/O Ports	5.5V
Operating Free-Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS1645A			DM74ALS1645A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			8			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended free air temperature range

Symbol	Parameter	Test Conditions		DM54ALS1645A			DM74ALS1645A			Units
				Min	Typ	Max	Min	Typ	Max	
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = Min	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
			I_{OH} = Max	2			2			
V_{OL}	Low Level Output Voltage	V_{CC} = Min	I_{OL} = 8 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 16 mA					0.35	0.5	
I_I	Input Current at Max Input Voltage	V_{CC} = Max	I/O Ports, V_I = 5.5V			100			100	μA
			Control Inputs, V_I = 7V			100			100	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V (Note 1)				20			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V (Note 1)				−100			−100	μA
I_O	Output Drive Current	V_{CC} = Max, V_O = 2.25V		−30		−112	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = Max			25	40		25	36	mA

Note 1: For I/O ports, the parameters I_{IH} and I_{IL} include the off-state currents. (I_{OZH}, I_{OZL})

Switching Characteristics over recommended operating free air temperature range

Symbol	Parameter	Conditions	From (Input) To (Output)	DM54ALS1645A		DM74ALS1645A		Units
				Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V, R_1 = 500Ω, R_2 = 500Ω, C_L = 50 pF	A or B to B or A	2	15	2	13	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		A or B to B or A	2	15	2	13	ns
t_{PZH}	Output Enable Time to High Level Output		$\overline{G}$ to A or B	8	28	8	25	ns
t_{PZL}	Output Enable Time to Low Level Output		$\overline{G}$ to A or B	8	28	8	25	ns
t_{PHZ}	Output Disable Time from High Level Output		$\overline{G}$ to A or B	2	14	2	12	ns
t_{PLZ}	Output Disable Time from Low Level Output		$\overline{G}$ to A or B	3	22	3	18	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

PRELIMINARY

DM54ALS2541/DM74ALS2541 Octal Buffers and MOS Line Drivers with TRI-STATE® Outputs

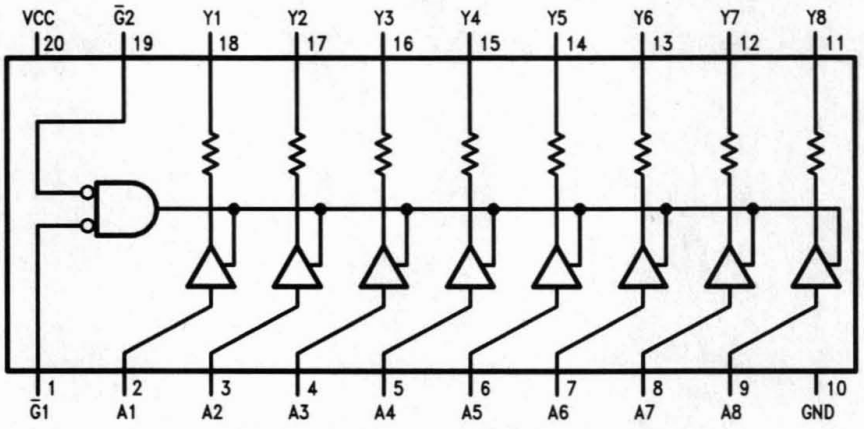
General Description

These octal buffers and line drivers are designed to have the performance of the 'ALS240 series and, at the same time, offer a pinout with inputs and outputs on opposite sides of the package. This arrangement of input/outputs enhances printed circuit board layout. These drivers are designed to drive the capacitive inputs of MOS devices. The outputs have 25Ω resistors in series, thus external components are not required. The TRI-STATE control gate is a 2-input NOR such that if either $\overline{G}1$ or $\overline{G}2$ is high, all eight outputs are in the high impedance state.

Features

- Advanced oxide-isolated ion-implanted Schottky TTL process
- Switching performance is guaranteed over full temperature and V_{CC} supply range
- Data Flow-Thru Pinout (All inputs on opposite side from outputs)
- P-N-P Inputs reduce DC loading
- Outputs have 25Ω series resistors thus no external resistors are required

Connection Diagram



TL/F/9165–1

Order Number DM54ALS2541J or DM74ALS2541WM, N
See NS Package Number J20A, M20B or N20A

Function Table

Input			Output
$\overline{G}1$	$\overline{G}2$	A	Y
H	X	X	Hi-Z
X	H	X	Hi-Z
L	L	L	L
L	L	H	H

H = High Logic Level, L = Low Logic Level
X = Don't Care (Either high or low logic level)
Hi-Z = High Impedance (Off) State

This document contains information on a product under development. NSC reserves the right to change or discontinue this product without notice.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Voltage Applied to a Disabled TRI-STATE Output	5.5V
Operating Free-Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS2541			DM74ALS2541			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			12			12	mA
T_A	Operating Free Air Temperature Range	−55		125	0		70	°C

Electrical Characteristics over recommended free air temperature range

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V, I_{OH} = −0.4 mA		V_{CC} − 2			mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min	I_{OL} = 1 mA		0.15	0.5	
			I_{OL} = 12 mA		0.35	0.8	
I_{OZH}	High Level TRI-STATE Output Current	V_{CC} = Max, V_O = 2.7V				20	μA
I_{OZL}	Low Level TRI-STATE Output Current	V_{CC} = Max, V_O = 0.4V				−20	μA
I_{OH}	High Level Output Current	V_{CC} = Min, V_O = 2V		−15			mA
I_{OL}	Low Level Output Current	V_{CC} = Min, V_O = 2V		30			mA
I_I	Input Current @ Maximum Input Voltage	V_{CC} = Max, V_I = 7V				100	μA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−100	μA
I_O	Output Drive Current	V_{CC} = Max, V_O = 2.25V		−15		−70	mA
I_{CC}	Supply Current	V_{CC} = Max	Outputs High		6	14	mA
			Outputs Low		15	25	
			Outputs Disabled		13.5	22	

Switching Characteristics over recommended operating free air temperature range

Symbol	Parameter	Conditions	From (Input) To (Output)	DM54ALS2541		DM74ALS2541		Units
				Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V, $R_1 = R_2 = 500\Omega$ (Note 1) C_L = 50 pF	A to Y	2	17	2	15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		A to Y	2	14	2	12	ns
t_{PZH}	Output Enable Time to High Level Output		$\overline{G}$ to Y	5	18	5	15	ns
t_{PZL}	Output Enable Time to Low Level Output		$\overline{G}$ to Y	8	24	8	20	ns
t_{PHZ}	Output Disable Time from High Level Output		$\overline{G}$ to Y	1	12	1	10	ns
t_{PLZ}	Output Disable Time from Low Level Output		$\overline{G}$ to Y	2	14	2	12	ns

Note 1: See Section 1 for output load and test waveforms.

National Semiconductor Corporation

PRELIMINARY

DM54ALS2645A/DM74ALS2645A Octal TRI-STATE® Transceivers

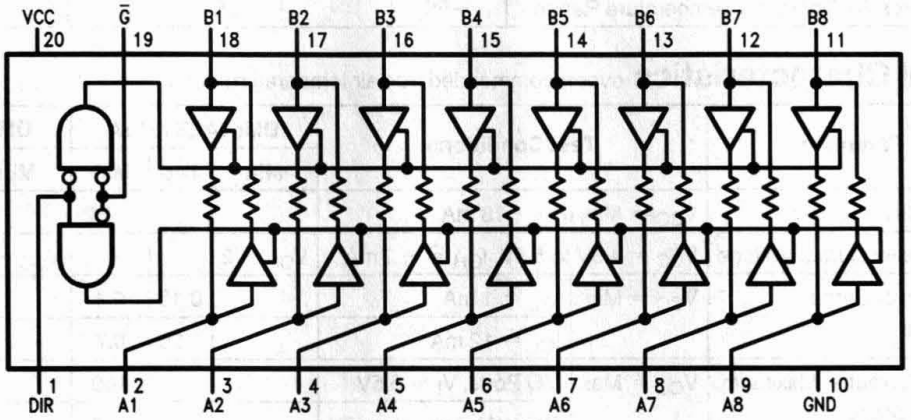
General Description

This octal bus transceiver is designed for asynchronous two way communication between data buses. Data is transmitted either from the A bus to the B bus or from the B bus to the A bus depending on the logic level of the direction control (DIR) input. The device can be disabled via the enable input (G) which causes outputs to enter the high impedance mode so the buses are effectively isolated.

Features

- Advanced oxide-isolated, ion implanted Schottky TTL process
- Switching specification guaranteed over the full temperature and V_{CC} range
- PNP inputs to reduce input loading
- I/O ports have 25Ω series resistors so no external resistors are required

Connection Diagram



TL/F/9168–1

Order Number DM54ALS2645AJ, DM74ALS2645AWM or DM74ALS2645AN
See NS Package Number J20A, M20B or N20A

Function Table

Control Inputs		Operation
$\overline{G}$	DIR	
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	High Impedance

L = Low Logic Level, H = High Logic Level

X = Don't Care (Either Low or High Logic Level)

This document contains information on a product under development. NSC reserves the right to change or discontinue this product without notice.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	
Control Inputs	7V
I/O Ports	5.5V
Storage Temperature Range	−65°C to +150°C

ESD rating is to be determined.

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS2645A			DM74ALS2645A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
T_A	Free Air Operating Temperature Range	−55		125	0		70	°C

Electrical Characteristics over recommended free air temperature range

Symbol	Parameter	Test Conditions		DM54ALS2645A			DM74ALS2645A			Units
				Min	Typ	Max	Min	Typ	Max	
V_{IK}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2			−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V, I_{OH} = −2 mA		V_{CC} − 2			V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min	I_{OL} = 1 mA		0.15	0.4		0.15	0.4	V
			I_{OL} = 12 mA		0.35	0.7		0.35	0.7	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	I/O Ports, V_I = 5.5V			100			100	μA
			Control Inputs, V_I = 7V			100			100	
I_{IH}	High Level Input Current (Note 1)	V_{CC} = Max, V_I = 2.7V	Control Inputs			20			20	μA
			I/O Ports			70			70	
I_{IL}	Low Level Input Current (Note 1)	V_{CC} = Max, V_I = 0.4V	Control Inputs			−500			−500	μA
			I/O Ports			−750			−750	
I_O	Output Drive Current	V_{CC} = Max, V_O = 2.25V		−50		−150	−50		−150	mA
I_{CC}	Supply Current	V_{CC} = Max	Outputs High		58	95		58	95	mA
			Outputs Low		95	155		95	155	
			Outputs Disabled		73	119		73	119	

Note 1: For I/O ports, I_{IH} and I_{IL} parameters include the TRI-STATE output currents (I_{OZL} and I_{OZH}).

Switching Characteristics over recommended operating free air temperature range

Symbol	Parameter	Conditions	From (Input) To (Output)	DM54ALS2645A		DM74ALS2645A		Units
				Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V $R_1 = R_2 = 500\Omega$, C_L = 50 pF (Note 1)	A or B to B or A	1	12	1	10	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		A or B to B or A	1	11	1	9.5	ns
t_{PZH}	Output Enable Time to High Level Output		$\overline{G}$ to A or B	1	13	1	11.5	ns
t_{PZL}	Output Enable Time to Low Level Output		$\overline{G}$ to A or B	1	13	1	10.5	ns
t_{PHZ}	Output Disable Time from High Level Output		$\overline{G}$ to A or B	1	9	1	8	ns
t_{PLZ}	Output DisableTime from Low Level Output		$\overline{G}$ to A or B	1	13	1	12	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

PRELIMINARY

DM54ALS5245/DM74ALS5245 Octal TRI-STATE® Transceivers

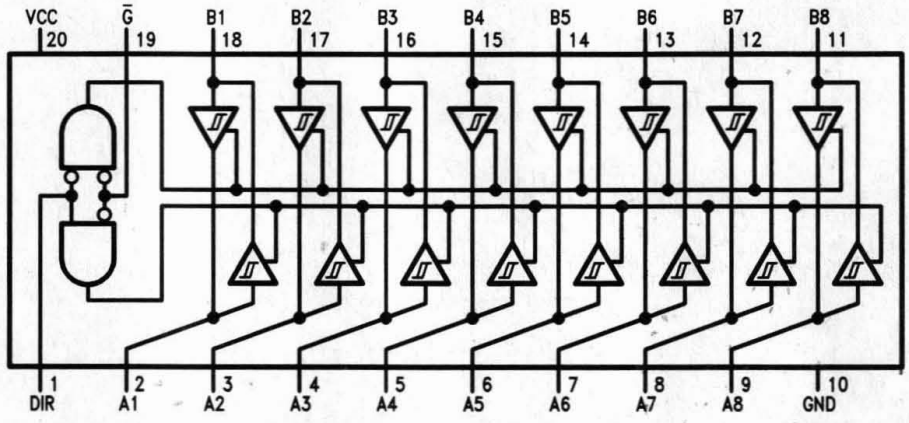
General Description

This octal bus transceiver is designed for asynchronous two-way communication between data buses. The inputs include hystersis which provides improved noise rejection. Data is transmitted either from the A bus to the B bus or from the B bus to the A bus depending on the logic level of the direction control (DIR) input. The device can be disabled via the enable input ($\overline{G}$) which causes the outputs to enter the high impedance mode so the buses are effectively isolated.

Features

- Advanced oxide-isolated, ion implanted Schottky TTL process
- Switching specification guaranteed over the full temperature and V_{CC} range
- PNP inputs to reduce input loading
- Input Hystersis to improve noise margin

Connection Diagram



TL/F/9175–1

Order Number DM54ALS5245J, DM74ALS5245WM or DM74ALS5245N
See NS Package Number J20A, M20B or N20A

Function Table

Control Inputs		Operation
$\overline{G}$	DIR	
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	High Impedance

L = Low Logic Level, H = High Logic Level
X = Don't Care (Either Low or High Logic Level)

This document contains information on a product under development. NSC reserves the right to change or discontinue this product without notice.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	
Control Inputs	7V
I/O Ports	5.5V
Operating Free-Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS5245			DM74ALS5245			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature Range	−55		125	0		70	°C

Electrical Characteristics over recommended free air temperature range

Symbol	Parameter	Test Conditions		DM54ALS5245			DM74ALS5245			Units
				Min	Typ	Max	Min	Typ	Max	
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5			−1.5	V
H_{YS}	Hystersis ($V_{T+} - V_{T-}$)	V_{CC} = Min		0.2	0.4		0.2	0.4		V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = Min	I_{OH} = 3 mA	2.4	3.2		2.4	3.2		
			I_{OH} = Max	2			2			
V_{OL}	Low Level Output Voltage	V_{CC} = Min	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	I/O Ports, V_I = 5.5V			100			100	μA
			Control Inputs, V_I = 7V			100			100	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V (Note 1)				20			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V (Note 1)				−100			−100	μA
I_O	Output Drive Current	V_{CC} = Max, V_O = 2.25V		−30		−112	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = Max	Outputs High		30	48		30	45	mA
			Outputs Low		36	60		36	55	
			Outputs Disabled		38	63		38	58	

Note 1: For I/O ports, I_{IH} and I_{IL} parameters include the TRI-STATE output currents (I_{OZL} and I_{OZH}).

Switching Characteristics over recommended operating free air temperature range

Symbol	Parameter	Conditions	From (Input) To (Output)	DM54ALS5245		DM74ALS5245		Units
				Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V, $R_1 = R_2 = 500\Omega$, C_L = 50 pF (Note 1)	A or B to B or A	3	15	3	10	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		A or B to B or A	3	13	3	10	ns
t_{PZH}	Output Enable Time to High Level Output		$\overline{G}$ to A or B	5	25	5	20	ns
t_{PZL}	Output Enable Time to Low Level Output		$\overline{G}$ to A or B	5	25	5	20	ns
t_{PHZ}	Output Disable Time from High Level Output		$\overline{G}$ to A or B	2	12	2	10	ns
t_{PLZ}	Output DisableTime from Low Level Output		$\overline{G}$ to A or B	4	18	4	15	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

PRELIMINARY

DM54ALS5620/DM74ALS5620 Octal TRI-STATE® Transceivers

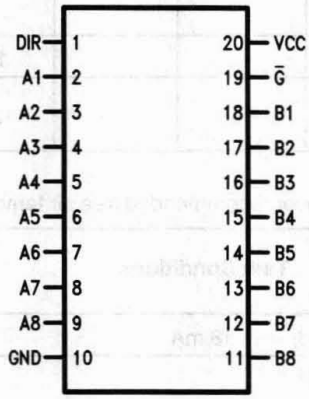
General Description

This octal bus transceiver is designed to have the performance of the 'ALS620 device with the addition of hystersis on the inputs. The input hystersis provides improved noise margin. Data is transmitted either from the A bus to the B bus or the B bus to the A bus depending on the logic level of the directon control input (DIR). The device can be disabled via the enable input (G) which causes the outputs to enter the high impedance mode so the busses are effectively isolated.

Features

- Advanced oxide-isolated, ion implanted Schottky TTL process
- Switching specification guaranteed over the full temperature and V_{CC} range
- PNP inputs to reduce input loading
- Hystersis on the inputs to improve noise rejection

Connection Diagram



TL/F/9166–1

Order Number DM54ALS5620J or DM74ALS5620WM, N
See NS Package Number J20A, M20B or N20A

Function Table

Control Inputs		Operation
$\overline{G}$BA	GAB	
L	X	$\overline{B}$ Data to A Bus
X	H	$\overline{A}$ Data to B Bus
H	L	High Impedance

L = Low Logic Level, H = High Logic Level
X = Don't Care (Either Low or High Logic Level)

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This document contains information on a product under development. NSC reserves the right to change or discontinue this product without notice.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	
Control Inputs	7V
I/O Ports	5.5V
Operating Free Air Temperature Range	
DM54ALS	−55°C to +125°C
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54ALS5620			DM74ALS5620			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Operating Free Air Temperature Range	−55		125	0		70	°C

Electrical Characteristics over recommended free air temperature range

Symbol	Parameter	Test Conditions		DM54ALS5620			DM54ALS5620			Units
				Min	Typ	Max	Min	Typ	Max	
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5			−1.5	V
HYS	Input Hystersis ($V_{T+} - V_{T-}$)	V_{CC} = Min		0.2			0.2			V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = Min	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
			I_{OH} = Max	2			2			
V_{OL}	Low Level Output Voltage	V_{CC} = Min	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max	I/O Ports, V_I = 5.5V			100			100	µA
			Control Inputs, V_I = 7V			100			100	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V (Note 1)				20			20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V (Note 1)				−100			−100	µA
I_O	Output Drive Current	V_{CC} = Max, V_O = 2.25V		−30		−112	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = Max	Outputs High		24	39		24	34	mA
			Outputs Low		25	49		31	44	
			Outputs Disabled		27	52		33	47	

Note 1: For I/O ports, I_{IH} and I_{IL} parameters include the TRI-STATE output currents (I_{OZL} and I_{OZH}).

Switching Characteristics over recommended operating free air temperature range

Symbol	Parameter	Conditions	From (Input) To (Output)	DM54ALS5620		DM74ALS5620		Units
				Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V, $R_1 = R_2 = 500\Omega$, C_L = 50 pF (Note 1)	A or B to B or A	2	12	2	10	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		A or B to B or A	2	12	2	10	ns
t_{PZH}	Output Enable Time to High Level Output		$\overline{G}$BA or GBA to A or B	3	23	3	17	ns
t_{PZL}	Output Enable Time to Low Level Output		$\overline{G}$BA or GBA to A or B	5	31	4	25	ns
t_{PHZ}	Output Disable Time from High Level Output		$\overline{G}$BA or GBA to A or B	2	14	3	12	ns
t_{PLZ}	Output DisableTime from Low Level Output		$\overline{G}$BA or GBA to A or B	3	22	4	18	ns

Note 1: See Section 1 for test waveforms and output load.

Section 3
Advanced Schottky

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National Semiconductor Corporation

DM74AS00 Quad 2-Input NAND Gates

General Description

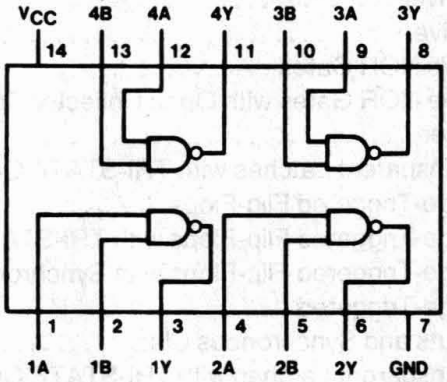
This device contains four independent gates, each of which performs the logic NAND function.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky, low power Schottky, and advanced low power Schottky TTL counterpart
- Improved AC performance over Schottky, low power Schottky, and advanced low power Schottky counterparts

Connection Diagram

Dual-In-Line Package



TL/F/6105–1

Order Number DM74AS00M or DM74AS00N
See NS Package Number M14A or N14A

Function Table

$$Y = \overline{AB}$$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level

L = Low Logic Level

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−2	mA
I_{OL}	Low Level Output Current			20	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2 mA V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 20 mA			0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		2.2	3.2	mA
			Outputs Low		10.8	17.4	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	1	4.5	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		1	4	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM74AS02 Quad 2-Input NOR Gates

General Description

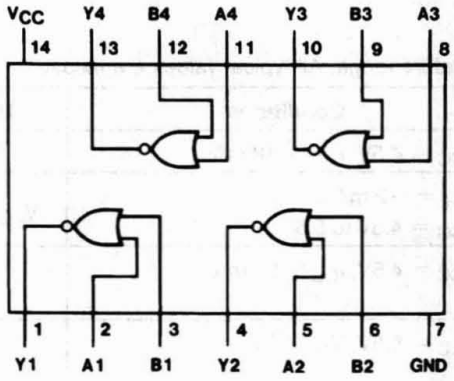
This device contains four independent gates, each of which performs the logic NOR function.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky, low power Schottky, and advanced low power Schottky TTL counterpart
- Improved AC performance over Schottky, low power Schottky and advanced low power Schottky counterparts

Connection Diagram

Dual-In-Line Package



TL/F/6272–1

Order Number DM74AS02M, N
See NS Package Number M14A or N14A

Function Table

$$Y = \overline{AB}$$

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−2	mA
I_{OL}	Low Level Output Current			20	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2 mA, V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 20 mA			0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		3.7	5.9	mA
			Outputs Low		12.5	20.1	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V, R_L = 500Ω, C_L = 50 pF	1	4.5	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		1	4.5	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM74AS04 Hex Inverters

General Description

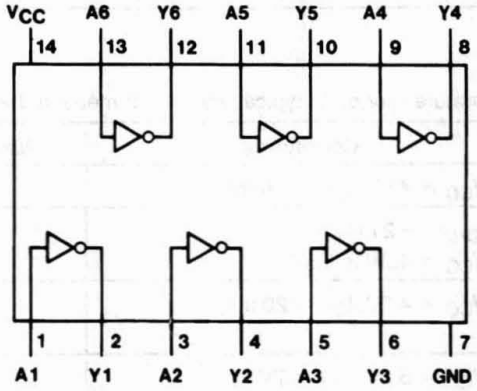
This device contains six independent gates, each of which performs the logic INVERT function.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky and low power Schottky TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts

Connection Diagram

Dual-In-Line Package



TL/F/6273–1

Order Number DM74AS04M, N
See NS Package Number M14A or N14A

Function Table

$Y = \overline{A}$

Input A	Output Y
L	H
H	L

H = High Logic Level

L = Low Logic Level

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−2	mA
I_{OL}	Low Level Output Current			20	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = − 2mA V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V I_{OL} = 20 mA			0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		3	4.8	mA
			Outputs Low		14	26.3	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	1	5	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		1	4	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM74AS08 Quad 2-Input AND Gate

General Description

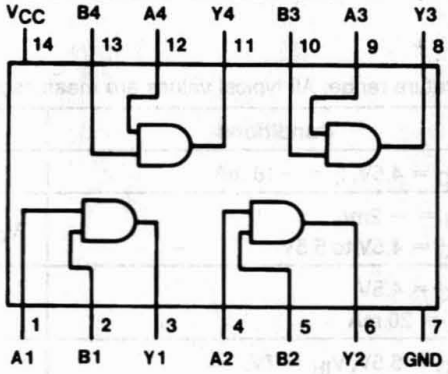
This device contains four independent gates, each of which performs the logic AND function.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky, low power Schottky, and advanced low power Schottky TTL counterpart
- Improved AC performance over Schottky, low power Schottky and advanced low power Schottky counterparts

Connection Diagram

Dual-In-Line Package



TL/F/6106–1

Order Number DM74AS08M or DM74AS08N
See NS Package Number M14A or N14A

Function Table

$Y = AB$

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = High Logic Level

L = Low Logic Level

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−2	mA
I_{OL}	Low Level Output Current			20	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2 mA V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 20 mA			0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		5.8	9.3	mA
			Outputs Low		14.9	24	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	1	5.5	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		1	5.5	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM74AS10 Triple 3-Input NAND Gates

General Description

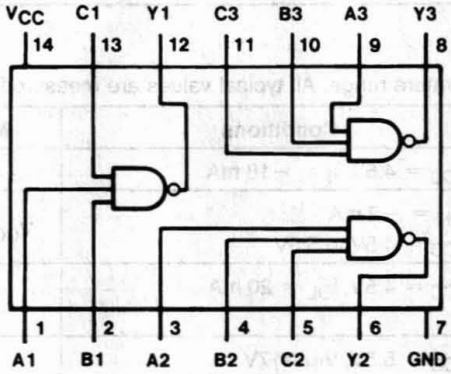
This device contains three independent gates, each of which performs the logic NAND function.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky, low power Schottky, and advanced low power Schottky TTL counterpart
- Improved AC performance over Schottky, low power Schottky, and advanced low power Schottky counterparts

Connection Diagram

Dual-In-Line Package



TL/F/6274–1

Order Number DM74AS10N
See NS Package Number N14A*

Function Table

$$Y = \overline{ABC}$$

Inputs			Output
A	B	C	Y
X	X	L	H
X	L	X	H
L	X	X	H
H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

*Contact your local NSC representative about surface mount (M) package availability.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−2	mA
I_{OL}	Low Level Output Current			20	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2 mA V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 20 mA			0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		1.5	2.4	mA
			Outputs Low		8.1	13	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	1	4.5	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		1	4.5	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM74AS11 Triple 3-Input AND Gates

General Description

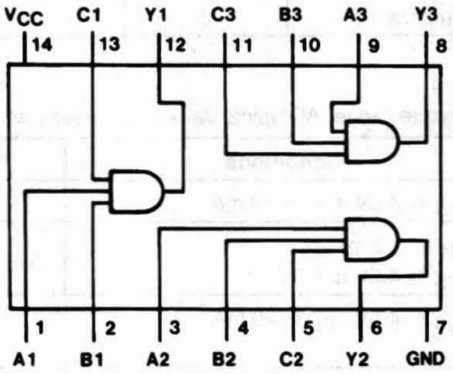
This device contains three independent gates each of which performs the logic AND function.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky, low power Schottky, and advanced low power Schottky TTL counterpart
- Improved AC performance over Schottky, low power Schottky, and advanced low power Schottky counterparts

Connection Diagram

Dual-In-Line Package



TL/F/6275–1

Order Number DM74AS11N
See NS Package Number N14A*

Function Table

$Y = ABC$

Inputs			Output
A	B	C	Y
X	X	L	L
X	L	X	L
L	X	X	L
H	H	H	H

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

*Contact your local NSC representative about surface mount (M) package availability.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−2	mA
I_{OL}	Low Level Output Current			20	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2 mA V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 20 mA			0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		4.3	7	mA
			Outputs Low		11.2	18	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	1	6	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		1	5.5	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM74AS20 Dual 4-Input NAND Gates

General Description

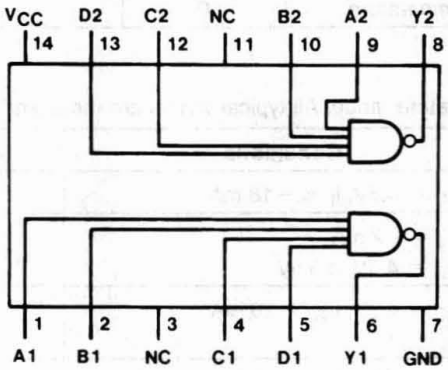
This device contains two independent gates, each of which performs the logic NAND function.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky, low power Schottky, and advanced low power Schottky TTL counterpart
- Improved AC performance over Schottky, low power Schottky, and advanced low power Schottky counterparts

Connection Diagram

Dual-In-Line Package



TL/F/6276–1

Order Number DM74AS20N
See NS Package Number N14A*

Function Table

$$Y = \overline{ABCD}$$

Inputs				Output
A	B	C	D	Y
X	X	X	L	H
X	X	L	X	H
X	L	X	X	H
L	X	X	X	H
H	H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

*Contact your local NSC representative about surface mount (M) package availability.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−2	mA
I_{OL}	Low Level Output Current			20	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2 mA V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 20 mA			0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		1.1	1.6	mA
			Outputs Low		6	8.7	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	1	5	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		1	4.5	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM74AS21 Dual 4-Input AND Gates

General Description

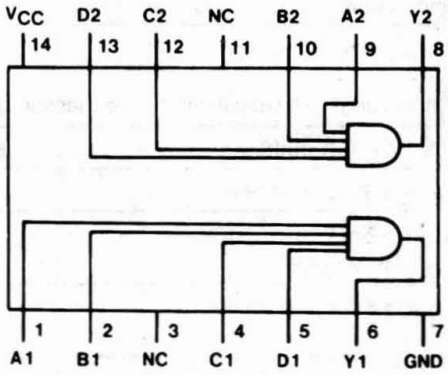
This device contains two independent 4-input gates, each of which performs the logic AND function.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky, low power Schottky, and advanced low power Schottky TTL counterpart
- Improved AC performance over Schottky, low power Schottky and advanced low power Schottky counterparts

Connection Diagram

Dual-In-Line Package



TL/F/6277–1

Order Number DM74AS21N
See NS Package Number N14A*

Function Table

Inputs				Output
A	B	C	D	Y
H	H	H	H	H
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

*Contact your local NSC representative about surface mount (M) package availability.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−2	mA
I_{OL}	Low Level Output Current			20	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2 mA, V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 20 mA			0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		2.9	4.6	mA
			Outputs Low		7.4	12	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V, R_L = 500Ω, C_L = 50 pF	1	6	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		1	6	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM74AS27 Triple 3-Input NOR Gates

General Description

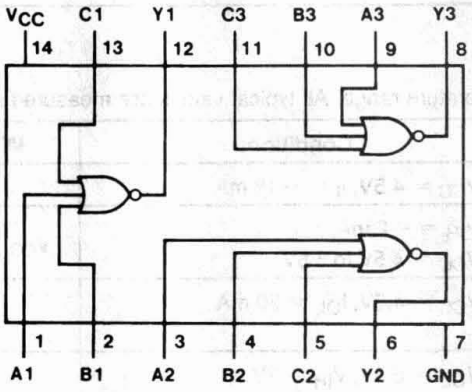
This device contains three independent 3-input gates, each of which performs the logic NOR function.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky, low power Schottky, and advanced low power Schottky TTL counterpart
- Improved AC performance over Schottky, low power Schottky, and advanced low power Schottky counterparts

Connection Diagram

Dual-In-Line Package



TL/F/6278–1

Order Number DM74AS27N
See NS Package Number N14A*

Function Table

$$Y = \overline{A + B + C}$$

Inputs			Output
A	B	C	Y
L	L	L	H
H	X	X	L
X	H	X	L
X	X	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

*Contact your local NSC representative about surface mount (M) package availability.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−2	mA
I_{OL}	Low Level Output Current			20	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2 mA V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 20 mA			0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		4	6.4	mA
			Outputs Low		10.6	17.1	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	1	5.5	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		1	4.5	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM74AS30 8 Input NAND Gate

General Description

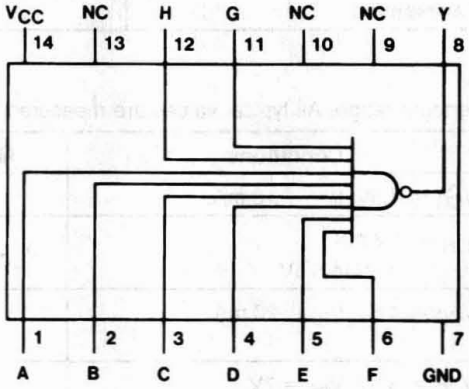
This device contains a single gate which performs the logic NAND function.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky, low power Schottky, and advanced low power Schottky TTL counterpart
- Improved AC performance over Schottky, low power Schottky, and advanced low power Schottky counterparts

Connection Diagram

Dual-In-Line Package



TL/F/6279–1

Order Number DM74AS30N
See NS Package Number N14A*

Function Table

$$Y = \overline{ABCDEFGH}$$

Inputs	Output
A thru H	Y
All inputs H	L
One or More Inputs L	H

H = High Logic Level
L = Low Logic Level

*Contact your local NSC representative about surface mount (M) package availability.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−2	mA
I_{OL}	Low Level Output Current			20	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2 mA V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 20 mA			0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		1	1.5	mA
			Outputs Low		3.4	4.9	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	1	5	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		1	4.5	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM74AS32 Quad 2-Input OR Gates

General Description

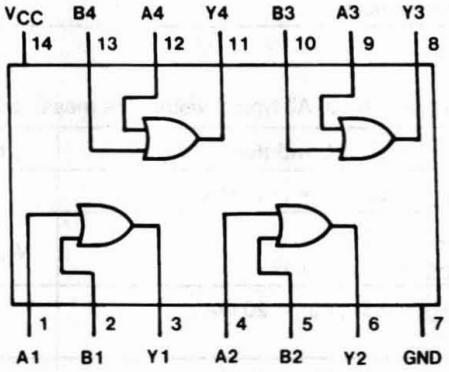
This device contains four independent gates, each of which performs the logic AND function.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky, low power Schottky, and advanced low power Schottky TTL counterpart
- Improved AC performance over Schottky, low power Schottky and advanced low power Schottky counterparts

Connection Diagram

Dual-In-Line Package



TL/F/6280–1

Order Number DM74AS32M or DM74AS32N
See NS Package Number M14A or N14A

Function Table

$Y = A + B$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

H = High Logic Level

L = Low Logic Level

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specifications.

Absolute Max
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7V
7V

0°C to +70°C
−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

d Operating Conditions

	Parameter	Min	Nom	Max	Units
	Supply Voltage	4.5	5	5.5	V
	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−2	mA
I_{OL}	Low Level Output Current			20	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V I_{OH} = −2 mA		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 20 mA			0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		7.3	12	mA
			Outputs Low		16.5	26.6	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	1	5.8	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		1	5.8	ns

Note 1: See Section 1 for test waveforms and output load.

3

National Semiconductor Corporation

DM74AS34 Hex Non-Inverter

General Description

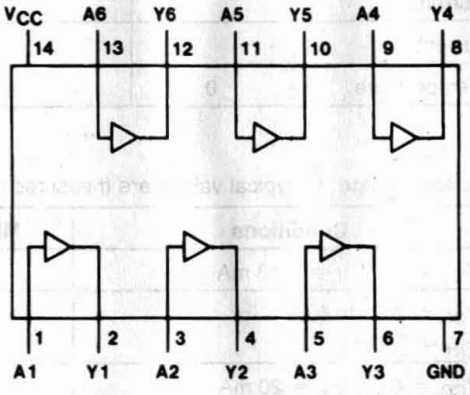
These devices contain six independent gates, each of which performs the logic identity function.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process

Connection Diagram

Dual-In-Line Package



TL/F/6281–1

Order Number DM74AS34N
See NS Package Number N14A*

Function Table

$Y = \overline{A}$

Input A	Output Y
H	H
L	L

H = High Logic Level
L = Low Logic Level

*Contact your local NSC representative about surface mount (M) package availability.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−2	mA
I_{OL}	Low Level Output Current			20	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V I_{OH} = −2 mA		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 20 mA			0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		7.4	12	mA
			Outputs Low		21.3	34.6	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	1	5.5	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		1	6	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM74AS74 Dual D Positive-Edge-Triggered Flip-Flops with Preset and Clear

General Description

The AS74 is a dual edge-triggered flip-flops. Each flip-flop has individual D, clock, clear and preset inputs, and also complementary Q and $\overline{Q}$ outputs.

Information at input D is transferred to the Q output on the positive going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. When the clock input is at either the high or low level, the D input signal has no effect.

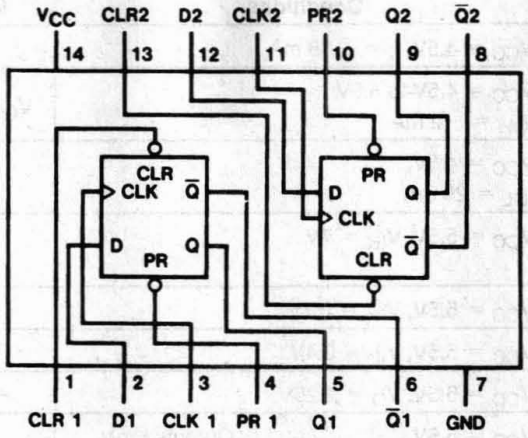
Asynchronous preset and clear inputs will set or clear Q output respectively upon the application of low level signal.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin-for-pin compatible with Schottky and LS TTL counterpart
- Improved AC performance over S74 at approximately half the power

Connection Diagram

Dual-In-Line Package



TL/F/6282–1

Order Number DM74AS74M, N
See NS Package Number M14A or N14A

Function Table

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

L = Low State, H = High State, X = Don't Care

↑ = Positive Edge Transition

Q_0 = Previous Condition of Q

* = This condition is nonstable; it will not persist when preset and clear inputs return to their inactive (high) level. The output levels in this condition are not guaranteed to meet the V_{OH} specification.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−2	mA
I_{OL}	Low Level Output Current				20	mA
f_{CLK}	Clock Frequency		0		105	MHz
$t_{W(CLK)}$	Width of Clock Pulse	High	4			ns
		Low	5.5			ns
t_W	Pulse Width Preset & Clear Low		4			ns
t_{SU}	Data Setup Time		4.5↑			ns
t_{SU}	PRE or CLR Setup-Time		2↑			ns
t_H	Data Hold Time		0↑			ns
T_A	Free Air Operating Temperature		0		70	°C

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

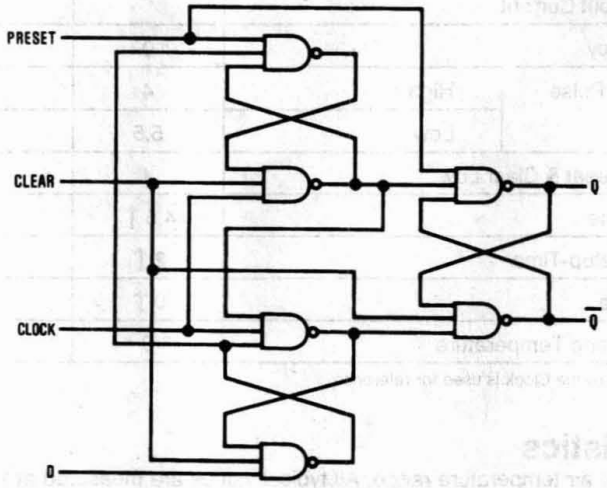
Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V, I_{OH} = −2 mA		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, V_{IH} = Max, I_{OL} = 20 mA			0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V	Clock, D			20	μA
			Preset, Clear			40	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V	Clock, D			−0.5	mA
			Preset, Clear			−1.8	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V			10.5	16	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From	To	Min	Max	Units
f_{MAX}	Maximum Clock Frequency	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF			105		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output		Preset or Clear	Q or $\overline{Q}$	3	7.5	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Preset or Clear	Q or $\overline{Q}$	3.5	10.5	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		Clock	Q or $\overline{Q}$	3.5	8	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Clock	Q or $\overline{Q}$	4.5	9	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6282–2

National Semiconductor Corporation

DM74AS86 Quad 2-Input Exclusive-OR Gates

General Description

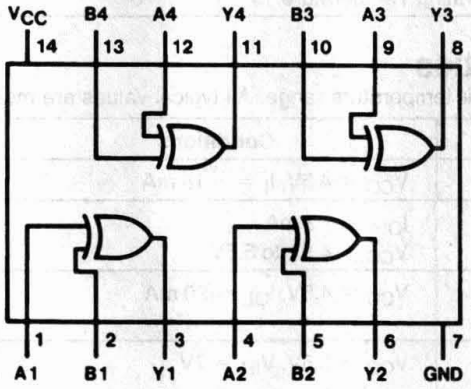
This device contains four independent gates, each of which performs the logic exclusive-OR function.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky, low power Schottky, and advanced low power Schottky TTL counterpart
- Improved AC performance over Schottky, low power Schottky, and advanced low power Schottky counterparts

Connection Diagram

Dual-In-Line Package



TL/F/6283–1

Order Number DM74AS86N
See NS Package Number N14A*

Function Table

$$Y = A \oplus B = \overline{A}B + A\overline{B}$$

Inputs		Outputs
A	B	
L	L	L
L	H	H
H	L	H
H	H	L

H = High Logic Level

L = Low Logic Level

*Contact your local NSC representative about surface mount (M) package availability.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−2	mA
I_{OL}	Low Level Output Current			20	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2 mA V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 20 mA			0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		12	16.5	mA
			Outputs Low		24	38	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output (Other Input Low)	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	2	6.5	ns
t_{PHL}	Propagation Delay Time High to Low Level Output (Other Input Low)		2	6.5	ns
t_{PLH}	Propagation Delay Time Low to High Level Output (Other Input High)		1	6	ns
t_{PHL}	Propagation Delay Time High to Low Level Output (Other Input High)		1	6	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM74AS109 Dual J-$\overline{K}$ Positive-Edge-Triggered Flip-Flops with Preset and Clear

General Description

The DM54AS109 is a dual edge-triggered flip-flop. Each flip-flop has individual J, $\overline{K}$, clock, clear and preset inputs, and also complementary Q and $\overline{Q}$ outputs.

Information at inputs J and $\overline{K}$ meeting the setup time requirements are transferred to the Q output on the positive going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. When the clock input is at either the high or low level, the J, $\overline{K}$ input signal has no effect.

Asynchronous preset and clear inputs will set or reset Q output respectively upon the application of low level signal.

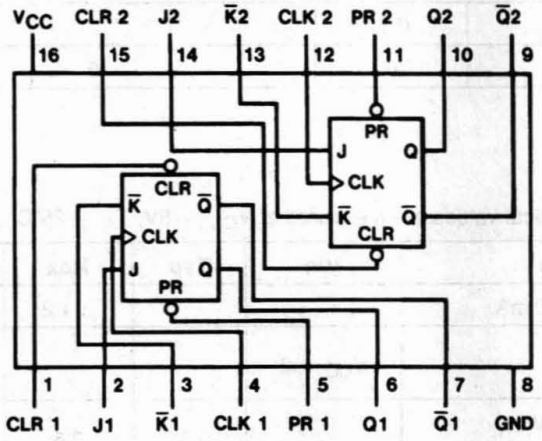
The J-$\overline{K}$ design allows operation as a D flip-flop by tying the J and $\overline{K}$ inputs together.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky and LS TTL counterpart
- Improved AC performance over S109 at approximately half the power

Connection Diagram

Dual-In-Line Package



TL/F/6284–1

Order Number DM74AS109N
See NS Package Number N16A*

Function Table

Inputs					Outputs	
PR	CLR	CK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

L = Low State, H = High State, X = Don't Care

↑ = Positive Edge Transition, Q_0 = Previous Condition of Q

*This condition is nonstable; it will not persist when preset and clear inputs return to their inactive (high) level. The output levels in this condition are not guaranteed to meet the V_{OH} specification.

*Contact your local NSC representative about surface mount (M) package availability.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−2	mA
I_{OL}	Low Level Output Current				20	mA
f_{CLK}	Clock Frequency		0		105	MHz
t_{WCLK}	Pulse Width	Clock High	4			ns
		Clock Low	5.5			ns
t_W	Pulse Width	Preset & Clear	4			ns
t_{SU}	Data Setup Time	J or $\overline{K}$	5.5 ↑			ns
		PRE or CLR Inactive	2 ↑			
t_H	Data Hold Time		0 ↑			ns
T_A	Free Air Operating Temperature		0		70	°C

The (↑) indicates the positive edge of the Clock is used for reference.

Electrical Characteristics

over recommended operating free-air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2 mA, V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, V_{IH} = 2V, I_{OL} = 20 mA			0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V	Clock, J, $\overline{K}$			20	μA
			Preset, Clear			40	
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V	Clock, J, $\overline{K}$			−0.5	mA
			Preset, Clear			−1.8	
I_O	Output Drive Current	V_O = 2.25V, V_{CC} = 5.5V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V (Note 1)			11.5	17	mA

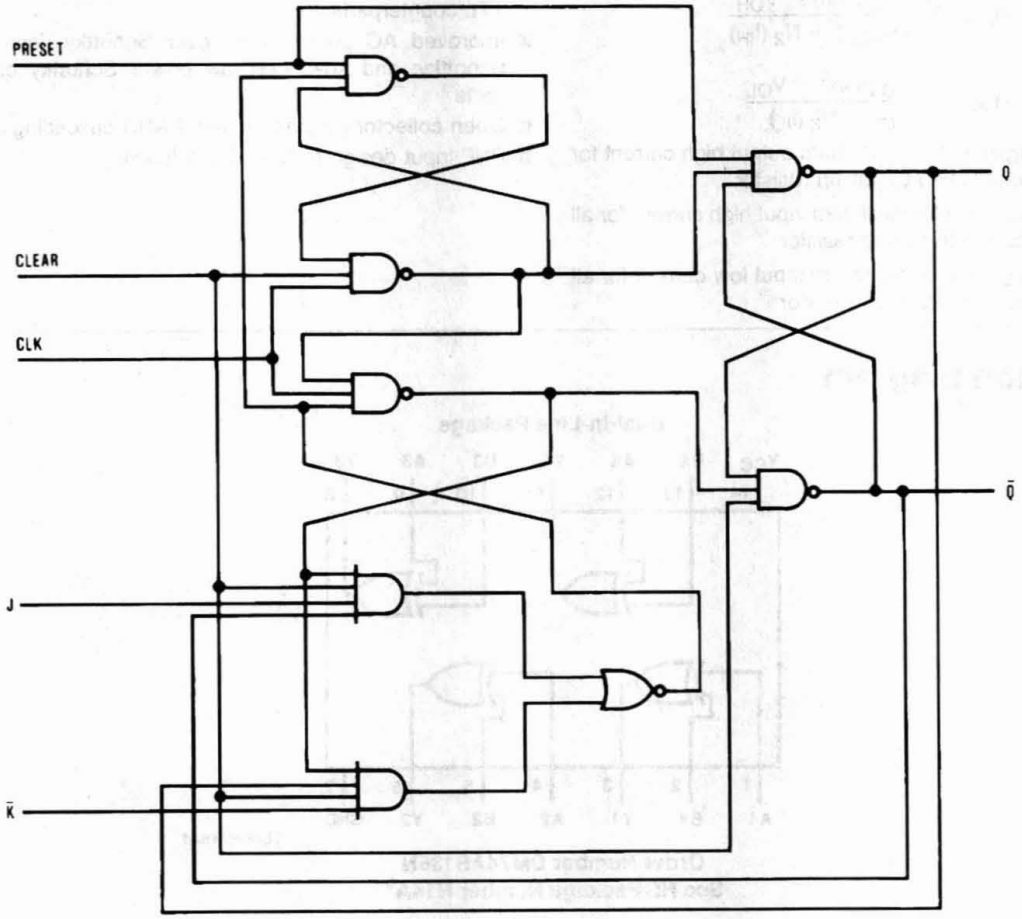
Note 1: I_{CC} is measured with J, $\overline{K}$, CLK and PR grounded, then with J, $\overline{K}$, CLK and CLR grounded.

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From	To	Min	Max	Units
f_{MAX}	Maximum Clock Frequency	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF			105		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output		Preset or Clear	Q or $\overline{Q}$	3	8	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Preset or Clear	Q or $\overline{Q}$	3.5	10.5	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		Clock	Q or $\overline{Q}$	3.5	9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Clock	Q or $\overline{Q}$	4.5	9	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6284–2

National Semiconductor Corporation

DM74AS136 Quad 2-Input Exclusive-OR Gates with Open-Collector Outputs

General Description

This device contains four independent gates, each of which performs the logic exclusive-OR function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

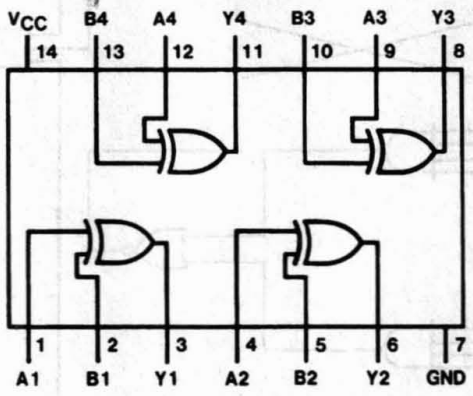
$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky, low power Schottky, and advanced low power Schottky TTL counterparts
- Improved AC performance over Schottky, low power Schottky, and advanced low power Schottky counterparts
- Open collector outputs for wired AND cascading
- PNP input design reduces input loading

Connection Diagram

Dual-In-Line Package



TL/F/6718–1

Order Number DM74AS136N
See NS Package Number N14A*

Function Table

$$Y = A \oplus B$$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = High Logic Level

L = Low Logic Level

*Contact your local NSC representative about surface mount (M) package availability.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Output Voltage (off-state)	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
V_{OH}	High Level Output Voltage			5.5	V
I_{OL}	Low Level Output Current			20	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max, V_{IH} = Min				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−0.5	mA
I_{CC}	Supply Current	V_{CC} = Max	Outputs High		13	18	mA
			Outputs Low		28	41	

Switching Characteristics

over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	DM74AS136		Units
			Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Other Input Low V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	5	45	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		1	8	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Other Input Low V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	5	45	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		1	9	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM74AS157/DM74AS158
Quad 1 of 2 Line Data Selectors/Multiplexers

General Description

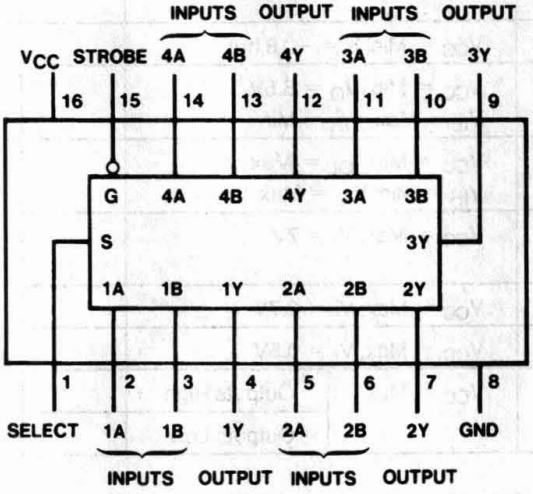
These data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The AS157 presents true data whereas the AS158 presents inverted data to minimize propagation delay time.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky, low power Schottky, and advanced low power Schottky TTL counterpart
- Improved AC performance over Schottky, low power Schottky, and advanced low power Schottky counterparts
- Expand any data input point
- Multiplex dual data buses
- General four functions of two variables (one variable is common)
- Source programmable counters

Connection Diagram

Dual-In-Line Package



TL/F/6290–1

Order Number DM74AS157N
or DM74AS158N
See NS Package Number N16A*

Function Table

Inputs				Output Y	
Strobe	Select	A	B	AS157	AS158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = High Level, L = Low Level, X = Don't Care

*Contact your local NSC representative about surface mount (M) package availability.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM74AS157, 158			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−2	mA
I_{OL}	Low Level Output Current			20	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V, I_{OH} = −2 mA		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 20 mA			0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V	Select			0.2	mA
			All Others			0.1	
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V	Select			40	μA
			All Others			20	
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V	Select			−1	mA
			All Others			−0.5	
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	'AS157		17.5	28	mA
			'AS158		15.6	22.5	mA

'AS157 Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From (Input)	To (Output)	DM74AS157		Units
					Min	Max	
t_{PLH}	Propagation Delay Time, Low to High Level Output	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R_L = 500Ω	Data	Y	1	6	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output		Data	Y	1	5.5	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output		Strobe	Y	2	10.5	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output		Strobe	Y	2	7.5	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output		Select	Y	2	11	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output		Select	Y	2	10	ns

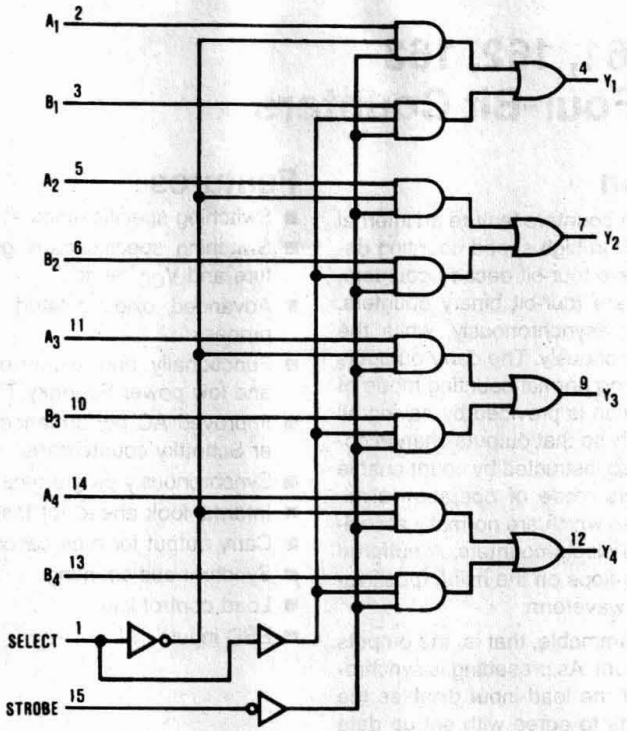
'AS158 Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From (Input)	To (Output)	DM74AS158		Units
					Min	Max	
t_{PLH}	Propagation Delay Time, Low to High Level Output	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R_L = 500Ω	Data	Y	1	5	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output		Data	Y	1	4.5	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output		Strobe	Y	2	6.5	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output		Strobe	Y	2	10	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output		Select	Y	2	9.5	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output		Select	Y	2	10.5	ns

Note 1: See Section 1 for test waveforms and output load.

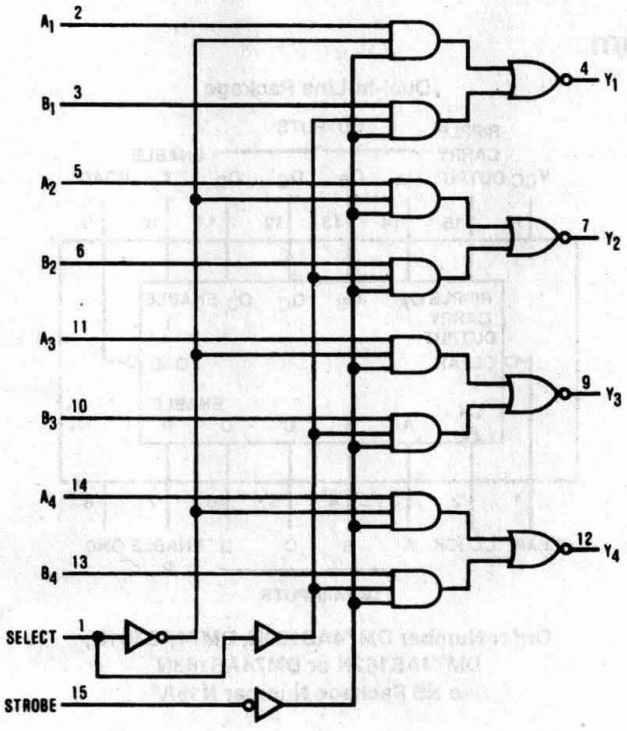
Logic Diagrams

AS157



TL/F/6290–2

AS158



TL/F/6290–3

National Semiconductor Corporation

DM74AS160, 161, 162, 163 Synchronous Four-Bit Counters

General Description

These synchronous presettable counters feature an internal carry look ahead for application in high speed counting designs. The AS160 and AS162 are four-bit decade counters, while the AS161 and AS163 are four-bit binary counters. The AS160 and AS161 clear asynchronously, while the AS162 and AS163 clear synchronously. The carry output is decoded to prevent spikes during normal counting mode of operation. Synchronous operation is provided by having all flip-flops clocked simultaneously so that outputs change coincident with each other when so instructed by count enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

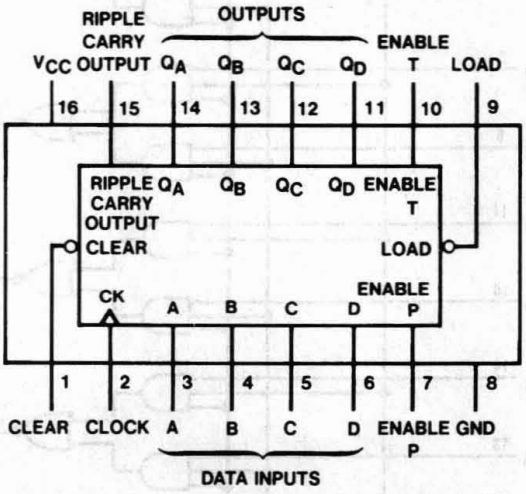
These counters are fully programmable, that is, the outputs may each be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with set up data after the next clock pulse regardless of the levels of enable input. Low to high transitions at the load input are perfectly acceptable regardless of the logic levels on the clock or enable inputs. (Continued)

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin-for-pin compatible with Schottky and low power Schottky TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts
- Synchronously programmable
- Internal look ahead for fast counting
- Carry output for n-bit cascading
- Synchronous counting
- Load control line
- ESD inputs

Connection Diagram

Dual-In-Line Package



TL/F/6291–1

Order Number DM74AS160N, DM74AS161N, DM74AS162N or DM74AS163N
See NS Package Number N16A*

*Contact your local NSC representative about surface mount (M) package availability.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter			DM74AS160 thru 163			Units
				Min	Nom	Max	
V_{CC}	Supply Voltage			4.5	5	5.5	V
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
I_{OH}	High Level Output Current					−2	mA
I_{OL}	Low Level Output Current					20	mA
f_{CLK}	Clock Frequency			0		75	MHz
t_{SU}	t_{setup}, Set-Up Time	Data; A, B, C, D		8			ns
		En P, En T		8			ns
		Load		8			ns
		Clear (Only for 162 & 163)	Low	12			ns
			High	9			
	Set-up 1 (Only for 160 & 161)	Clear		8			ns
t_H	t_{hold}, Hold Time	Data; A, B, C, D		0			ns
		En P, En T		0			ns
		Load		0			ns
		Clear (Only for 162 & 163)		0			ns
	Hold 0 (Only for 160 & 161)	Clear		0			ns
t_{WCLK}	Width of Clock Pulse			6.7			ns
t_{WCLR}	Width of Clear Pulse, ('AS160, 'AS161 Low)			8			ns

Electrical Characteristics over recommended operating free air temperature range

All typical values are measured at V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2 mA, V_{CC} = 4.5 to 5.5V		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 20 mA			0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V	Load			0.3	mA
			ENT			0.2	
			Others			0.1	
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V	Load			60	μA
			ENT			40	
			Others			20	
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V	Load			−0.5	mA
			ENT			−1	
			Others			0.5	
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V			35	53	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From	To	DM74AS160 thru 163		Units
					Min	Max	
f_{MAX}	Max. Clock Freq.	V_{CC} = 4.5V to 5.5V, R_L = 500Ω, C_L = 50 pF			75		MHz
t_{PHL}	Propagation Delay Time High to Low Level Output		Clock	Ripple Carry	2	12.5	ns
t_{PLH}	Propagation Delay Time Low to High Level Output with Load High		Clock	Ripple Carry	1	8	ns
t_{PLH}	Propagation Delay Time Low to High Level Output with Load Low		Clock	Ripple Carry	3	16.5	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		Clock	Any Q	1	7	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Clock	Any Q	2	13	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		En T	Ripple Carry	1.5	9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		En T	Ripple Carry	1	8.5	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Clear (AS160, AS161)	Any Q	2	13	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Clear (AS160, AS161)	Ripple Carry	2	12.5	ns

Note 1: See Section 1 for test waveforms and output load.

General Description (Continued)

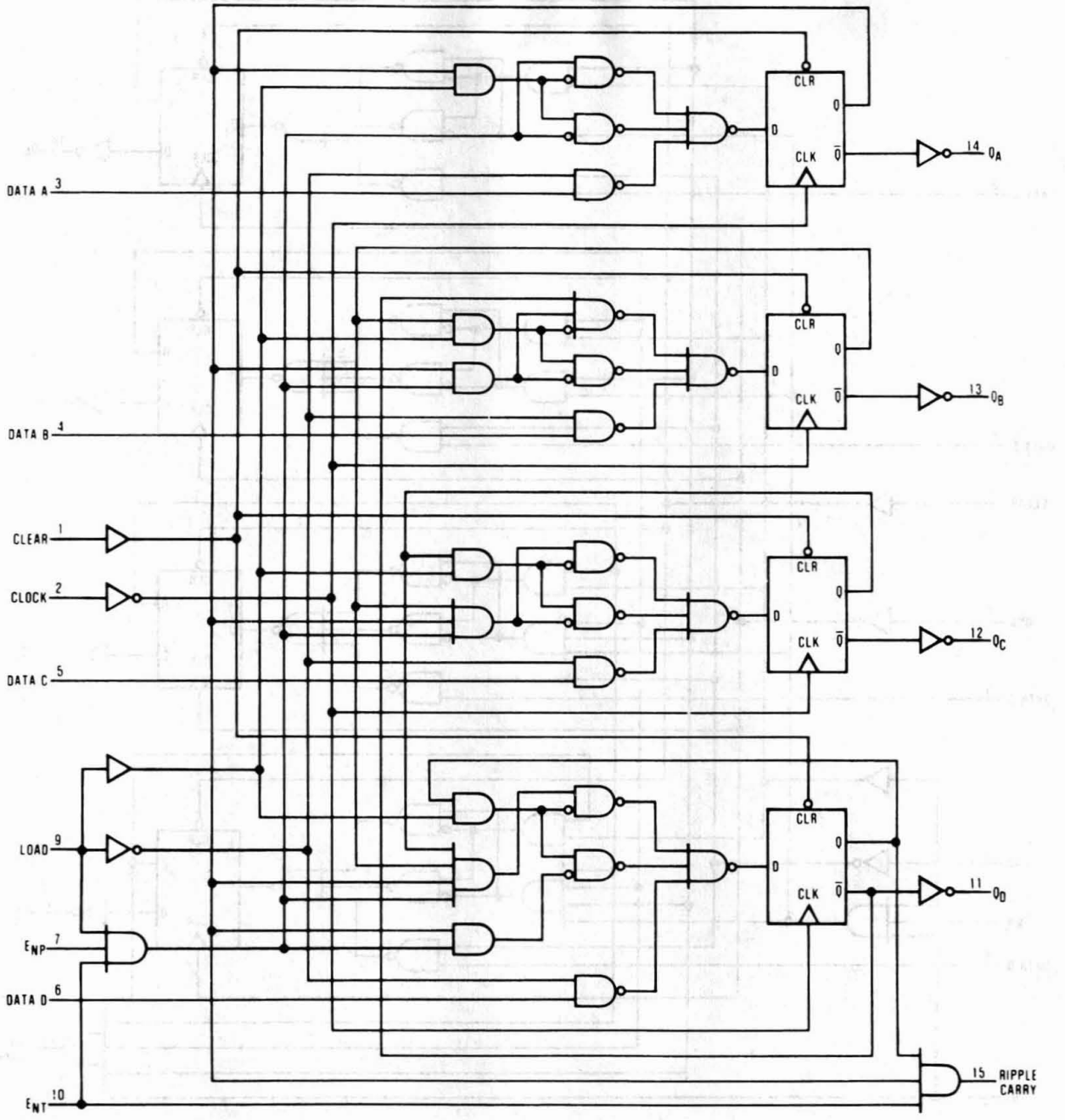
The AS160 and AS161 clear function is asynchronous. A low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of clock, load or enable inputs. These two counters are provided with a clear on power-up feature. The AS162 and AS163 clear function is synchronous; and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of enable inputs. This synchronous clear allows the count length to be modified easily, as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to all low outputs. Low to high transitions at the clear input of the AS162 and AS163 are also permissible regardless of the levels of logic on the clock, enable or load inputs.

The carry look ahead circuitry provides for cascading counters for n bit synchronous application without additional gating. Instrumental in accomplishing this function are two count-enable inputs (P and T) and a ripple carry output. Both count-enable inputs must be high to count. The T input is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high level output pulse with a duration approximately equal to the high level portion of QA output. This high level overflow ripple carry pulse can be used to enable successive cascaded stages. High to low level transitions at the enable P or T inputs of the AS160 through AS163, may occur regardless of the logic level on the clock.

The AS160 through SA163 feature a fully independent clock circuit. Changes made to control inputs (enable P or T, or load) that will modify the operating mode will have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading or counting) will be dictated solely by the conditions meeting the stable set-up and hold times.

Logic Diagrams

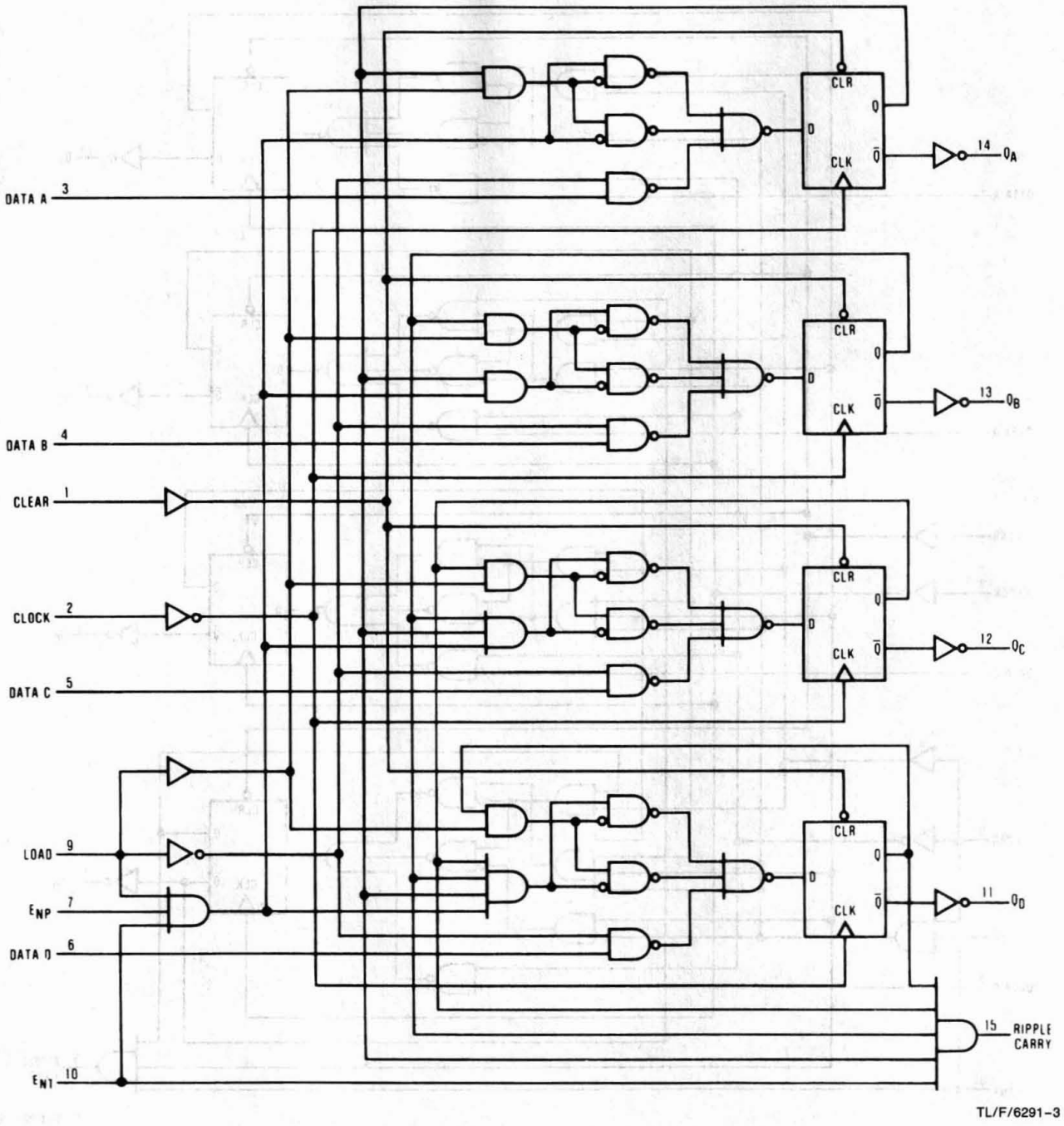
AS160



TL/F/6291–2

Logic Diagrams (Continued)

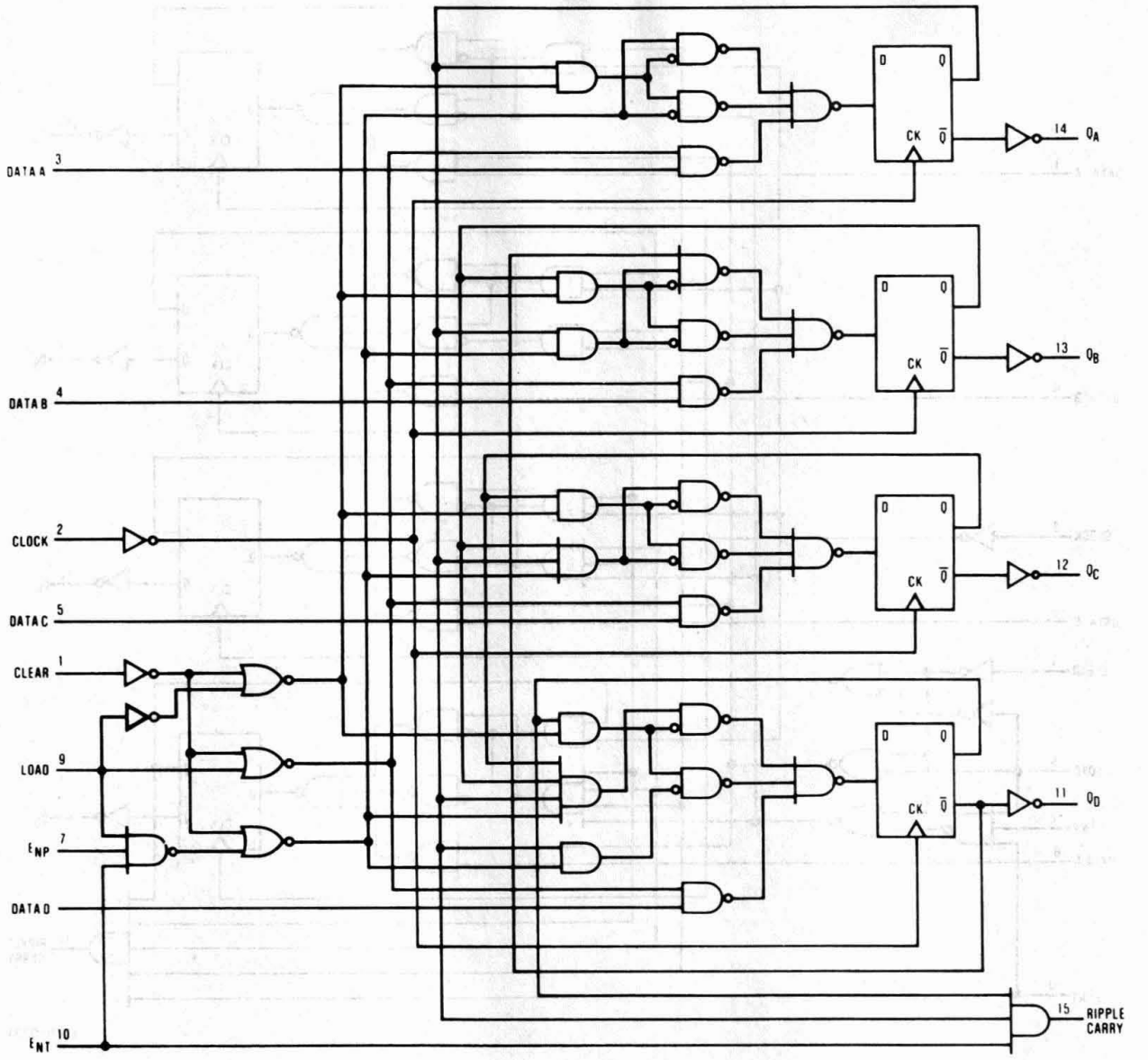
AS161



TL/F/6291–3

Logic Diagrams (Continued)

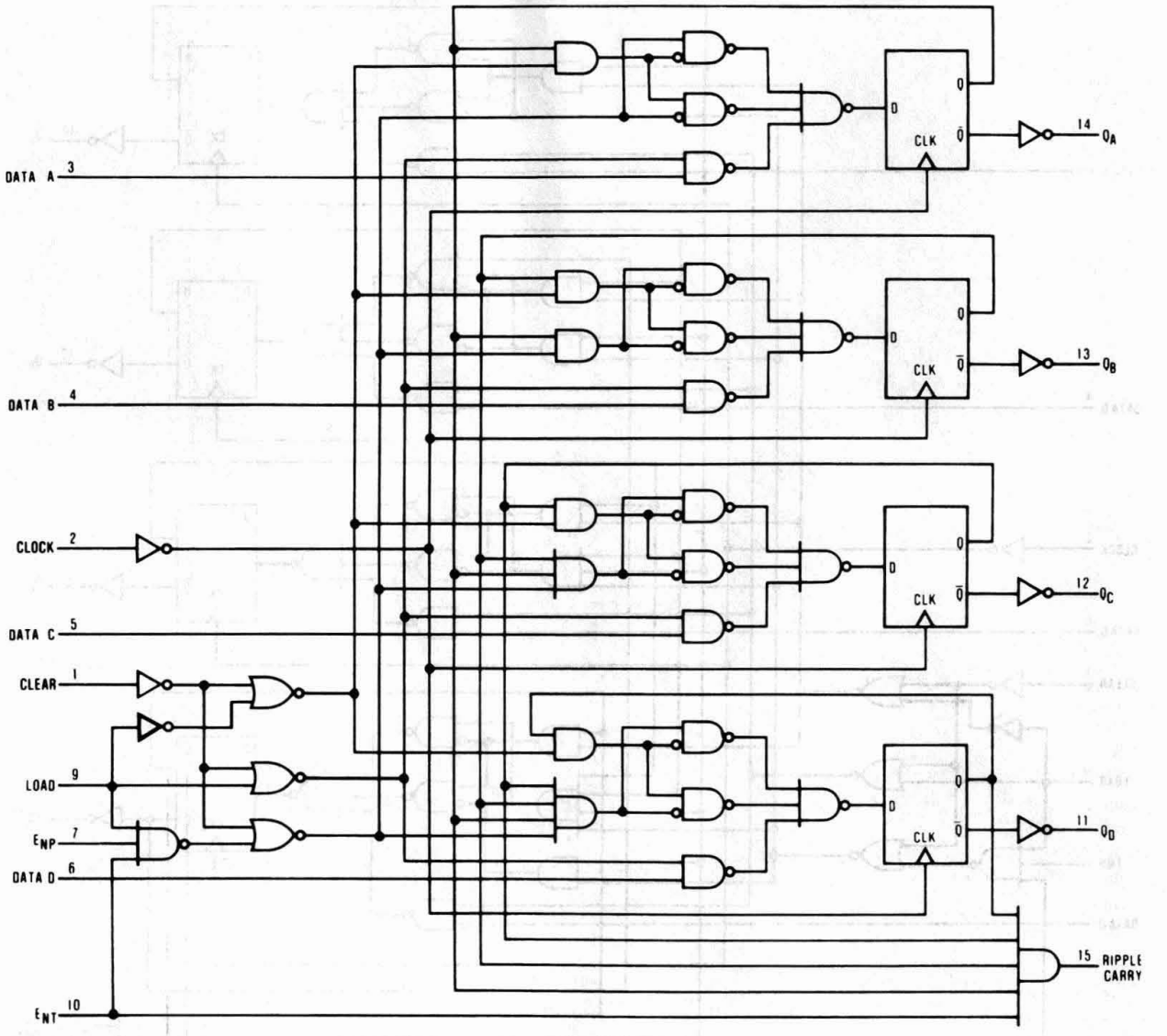
AS162



TL/F/6291–4

Logic Diagrams (Continued)

AS163



TL/F/6291–5

National Semiconductor Corporation

DM74AS168A, 169A
Synchronous Four Bit Up/Down Counters

General Description

These synchronous presettable counters feature an internal carry look ahead for cascading in high speed counting applications. The AS168 is a four-bit decade up/down counter and the AS169 is a four-bit binary up/down counter. The carry output is decoded to prevent spikes during normal mode of counting operation. Synchronous operation is provided so that outputs change coincident with each other when so instructed by count enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive going) edge of clock input waveform.

These counters are fully programmable; that is, the outputs may each be preset either high or low. The load input circuitry allows loading with carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry permits cascading counters for n-bit synchronous applications without additional gating. Both count enable inputs ($\overline{P}$ and $\overline{T}$) must be low to count. The direction of the count is determined by the level of the up/down input. When the input is high, the counter counts up; when low, it counts down. Input T is fed forward to enable the carry outputs. The carry output thus enabled will produce a low level output pulse with a duration approximately equal to the high portion of the QA output when counting up, and approximately equal to the low portion of the QA output when counting down. This low level overflow carry pulse can be used to enable successively cascaded stages. Transitions at the enable $\overline{P}$ or $\overline{T}$ inputs are allowed regardless of the level of the clock input.

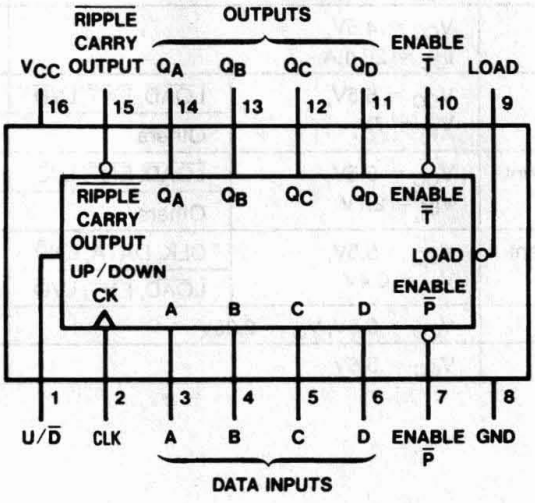
The control functions for these counters are fully synchronous. Changes at control inputs (enable $\overline{P}$, enable $\overline{T}$, load, up/down) which modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

Features

- Switching Specifications at 50 pF
- Switching Specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin-for-pin compatible with Schottky and low power Schottky TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts
- Synchronously programmable
- Internal look ahead for fast counting
- Carry output for n-bit cascading
- Synchronous counting
- Load control line
- ESD inputs

Connection Diagram

Dual-In-Line Package



TL/F/6292–1

Order Number DM74AS168AN or DM74AS169AN
See NS Package Number N16A*

*Contact your local NSC representative about surface mount (M) package availability.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−2	mA
I_{OL}	Low Level Output Current				20	mA
f_{CLK}	Clock Frequency		0		75	MHz
t_{SU}	t_{setup}, Set-up Time	Data; A, B, C, D	8			ns
		En $\overline{P}$, En $\overline{T}$	8			ns
		Load	8			ns
		U/$\overline{D}$	11			ns
t_H	t_{hold}, Hold Time	Data; A, B, C, D	0			ns
		En $\overline{P}$, En $\overline{T}$	0			ns
		Load	0			ns
		U/$\overline{D}$	0			ns
t_{WCLK}	Width of Clock Pulse		6.7			ns
t_A	Free Air Operating Temperature		0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2 mA, V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 20 mA			0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V	$\overline{LOAD}$, $\overline{ENT}$, U/$\overline{D}$			0.2	mA
			Others			0.1	
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V	$\overline{LOAD}$, $\overline{ENT}$, U/$\overline{D}$			40	μA
			Others			20	
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V	CLK, DATA, $\overline{ENP}$			−0.5	mA
			$\overline{LOAD}$, $\overline{ENT}$, U/$\overline{D}$			−1	
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V			46	63	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

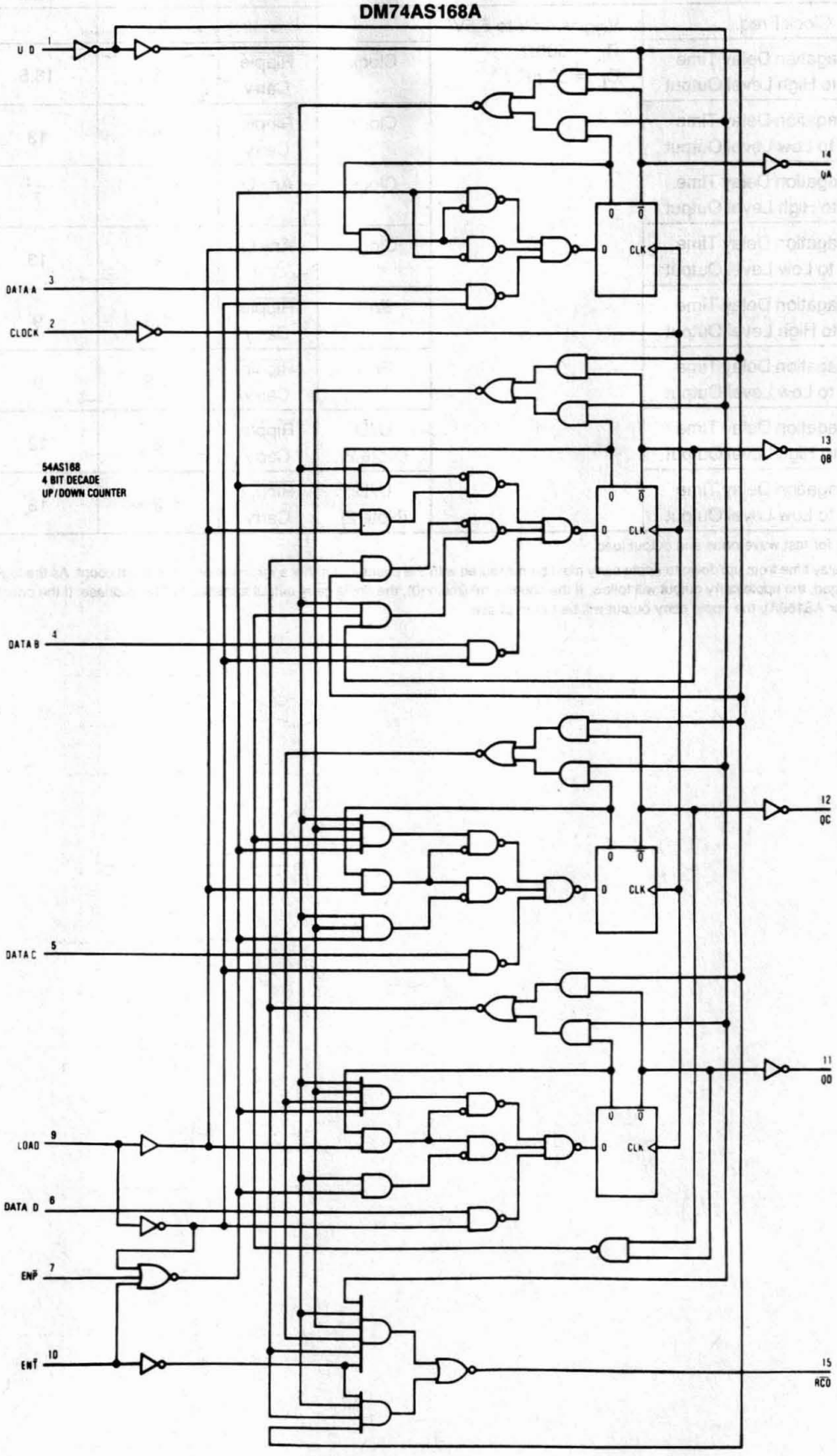
Symbol	Parameter	Conditions	From	To	Min	Max	Units
f_{MAX}	Max. Clock Freq.	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF			75		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output		Clock	$\overline{\text{Ripple}}$ Carry	3	16.5	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Clock	$\overline{\text{Ripple}}$ Carry	2	13	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		Clock	Any Q	1	7	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Clock	Any Q	2	13	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		En T	$\overline{\text{Ripple}}$ Carry	1.5	9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		En T	$\overline{\text{Ripple}}$ Carry	1.5	9	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		U/$\overline{\text{D}}$ (Note 2)	$\overline{\text{Ripple}}$ Carry	2	12	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		U/$\overline{\text{D}}$ (Note 2)	$\overline{\text{Ripple}}$ Carry	2	13	ns

Note 1: See Section 1 for test waveforms and output load.

Note 2: Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0), the ripple carry output transition will be in phase. If the count is maximum (9 for AS168A or 15 for AS169A), the ripple carry output will be out of phase.

Logic Diagrams

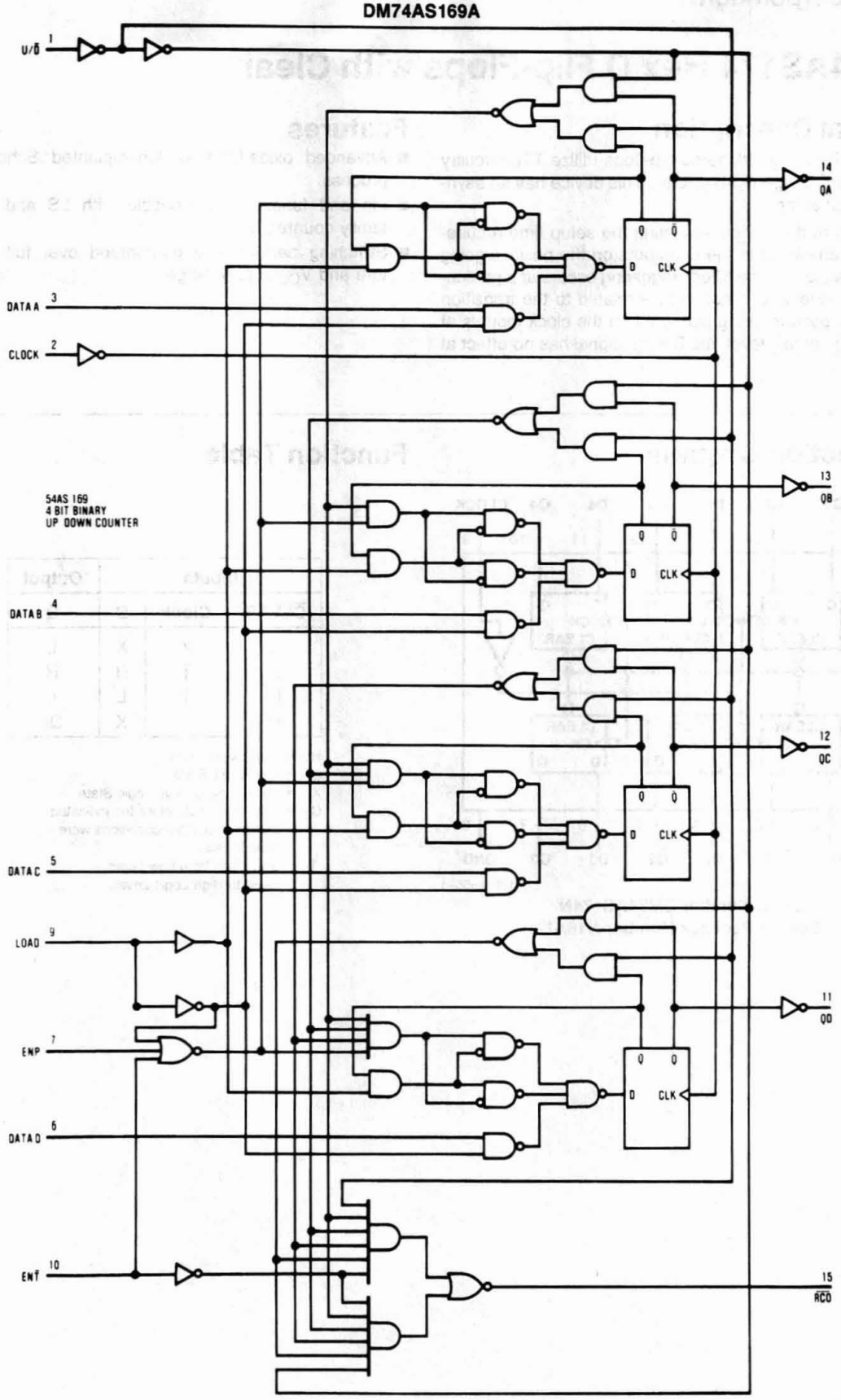
DM74AS168A



TL/F/6292–2

Logic Diagrams (Continued)

DM74AS169A



TL/F/6292–3

National Semiconductor Corporation

DM74AS174 Hex D Flip-Flops with Clear

General Description

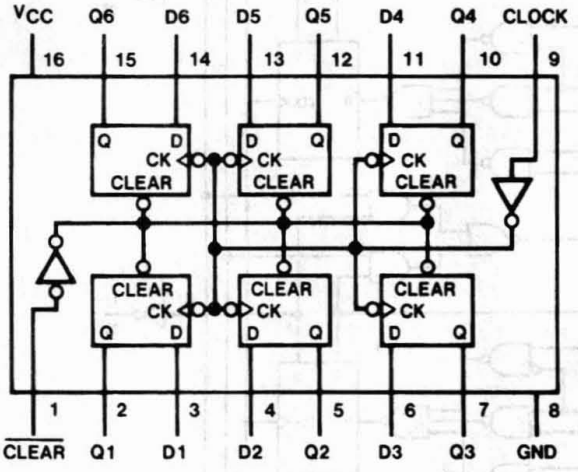
These positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. This device has an asynchronous clear input.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either a high or low level, the D input signal has no effect at the output.

Features

- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Pin and functional compatible with LS and Schottky family counterpart
- Switching performance guaranteed over full temperature and V_{CC} supply range

Connection Diagram


VCC Q6 D6 D5 Q5 D4 Q4 CLOCK
16 15 14 13 12 11 10 9
Q D CK CLEAR
D Q CK CLEAR
D Q CK CLEAR
CLEAR CK Q D
CLEAR CK D Q
CLEAR CK D Q
1 2 3 4 5 6 7 8
CLEAR Q1 D1 D2 Q2 D3 Q3 GND

TL/F/8655–1

Order Number DM74AS174N
See NS Package Number N16A*

Function Table

Inputs			Output
$\overline{CLEAR}$	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

H = High Logic State
L = Low Logic State
X = Either Low or High Logic State
Q_0 = The level of Q before the indicated steady-state input conditions were established.
↑ = Transition from Low Logic Level to High Logic Level

*Contact your local NSC representative about surface mount (M) package availability.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−2	mA
I_{OL}	Low Level Output Current				20	mA
f_{CLOCK}	Clock Frequency		0		100	MHz
t_W	Pulse Width	Clock High	4			ns
		Clock Low	6			
		$\overline{CLEAR}$	5			
t_{Setup}	Setup Time	Data	4			ns
		$\overline{CLEAR}$ Inactive	6			
t_{HOLD}	Data Input Hold Time		1			ns
T_A	Operating Free Air Temperature Range		0		70	°C

Electrical Characteristics over recommended operating free air temperature range

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA			−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = Max, V_{CC} = 4.5 to 5.5V	V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = Max, V_{IH} = 2V		0.35	0.5	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = 5.5V, V_I = 7V			100	μA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_I = 2.7V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_I = 0.4V			−500	μA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V (Note 2)		30	45	mA

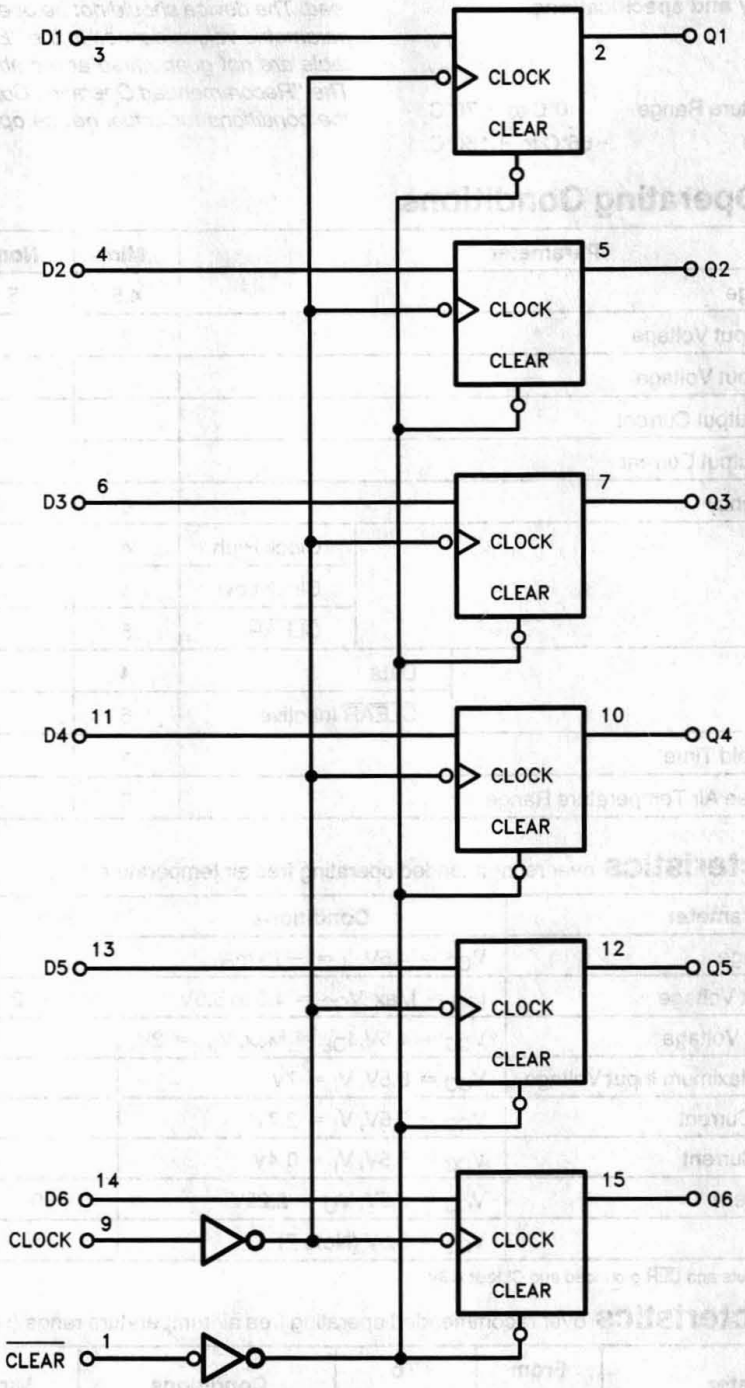
Note 2: I_{CC} is measured with D inputs and $\overline{CLR}$ grounded and CLK at 4.5V.

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	From (Input)	To (Output)	Conditions	Min	Max	Units
f_{MAX}	Maximum Clock Frequency			V_{CC} = 4.5V to 5.5V, C_L = 50 pF, T_A = Min to Max, R_L = 500Ω	100		MHz
t_{PHL}	Propagation Delay Time High to Low Level Output	$\overline{CLEAR}$	Q		5	14	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock	Q		3.5	8	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock	Q		4.5	10	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/8655–2

National Semiconductor Corporation

DM74AS175A Quad D Flip-Flops with Clear

General Description

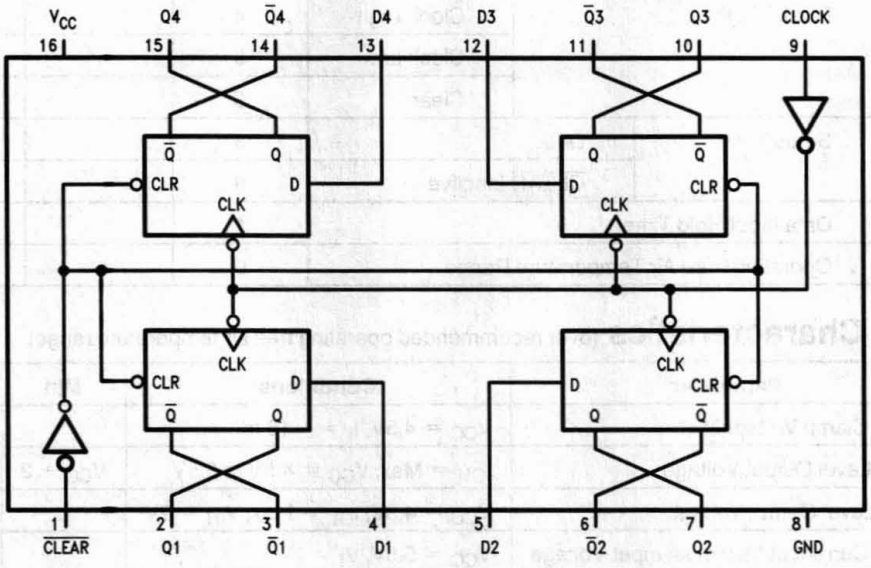
These positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. This device has an asynchronous clear input.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either a high or low level, the D input signal has no effect at the output.

Features

- Advanced Oxide-Isolated Ion-Implanted Schottky TTL process
- Pin and Functional compatible with LS and Schottky family counterpart
- Switching performance guaranteed over full temperature and V_{CC} supply range

Connection Diagram



TL/F/8656–1

Order Number DM74AS175AN
See NS Package Number N16A*

Function Table

Inputs			Outputs	
$\overline{CLEAR}$	Clock	D	Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

H = High Logic State

L = Low Logic State

Q_0 = The level of Q before the indicated steady-state input conditions were established.

↑ = Transition from Low Logic Level to High Logic Level

*Contact your local NSC representative about surface mount (M) package availability.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temp. Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−2	mA
I_{OL}	Low Level Output Current				20	mA
f_{CLOCK}	Clock Frequency		0		100	MHz
t_W	Pulse Width	Clock High	4			ns
		Clock Low	5			
		Clear	5			
t_{Setup}	Setup Time	Data	3			ns
		$\overline{\text{CLEAR}}$ Inactive	6			
t_{HOLD}	Data Input Hold Time		1			ns
T_A	Operating Free Air Temperature Range		0		70	°C

Electrical Characteristics (over recommended operating free air temperature range)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA			−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = Max, V_{CC} = 4.5V to 5.5V	V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = Max, V_{IH} = 2V		0.35	0.5	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = 5.5V, V_I = 7V			100	μA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_I = 2.7V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_I = 0.4V			−500	μA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V (Note 1)		22.5	34	mA

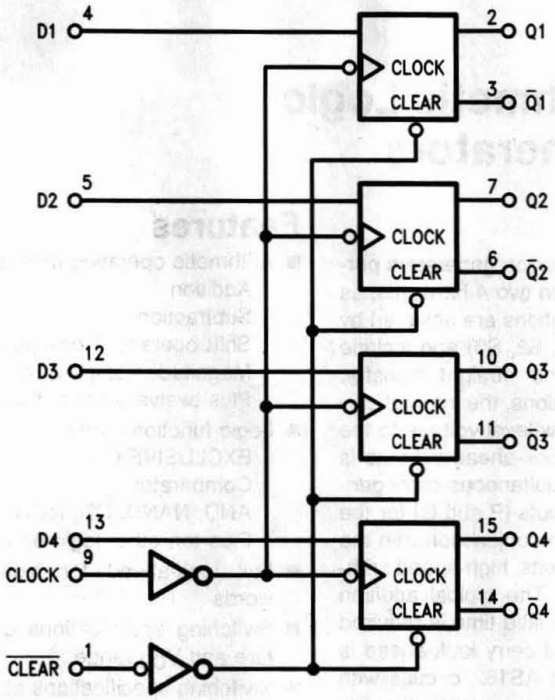
Note 1: I_{CC} is measured with D inputs and CLEAR grounded, and clock at 4.5V.

Switching Characteristics over recommended operating free air temperature range (Note 2)

Symbol	Parameter	From (Input)	To (Output)	Conditions	Min	Max	Units
f_{MAX}	Maximum Clock Frequency			V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R_L = 500Ω, T_A = Min to Max	100		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	$\overline{\text{CLEAR}}$	$\overline{Q}$		4	9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	$\overline{\text{CLEAR}}$	Q		4.5	13	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock	Q or $\overline{Q}$		4	7.5	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock	Q or $\overline{Q}$		4	10	ns

Note 2: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/8656–2

National Semiconductor Corporation

DM74AS181B Arithmetic Logic Unit/Function Generators

General Description

These arithmetic logic units (ALU)/function generators perform 16 binary arithmetic operations on two 4-bit words, as shown in Tables I and II. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (P and G) for the four bits in the package. When used in conjunction with the DM74AS182 full carry look-ahead circuits, high-speed arithmetic operations can be performed. The typical addition times shown in Table III illustrate how little time is required for addition of longer words, when full carry look-ahead is employed. The method of cascading AS182 circuits with these ALU's to provide multi-level full carry look-ahead is illustrated under typical applications data for the DM74AS182.

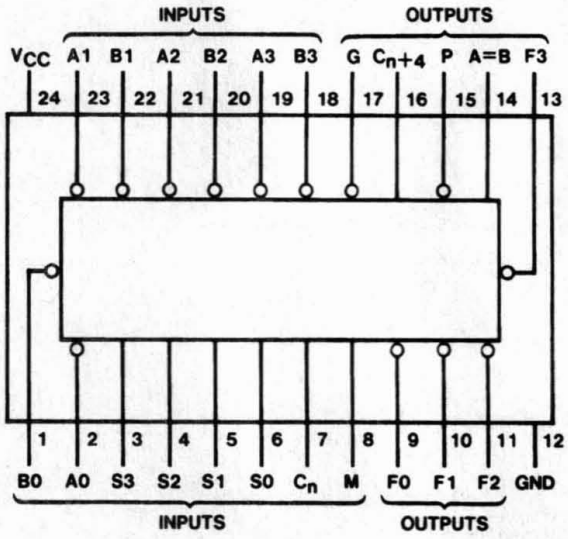
(Continued)

Features

- Arithmetic operating modes:
  - Addition
  - Subtraction
  - Shift operand A one position
  - Magnitude comparison
  - Plus twelve other arithmetic operations
- Logic function modes:
  - EXCLUSIVE-OR
  - Comparator
  - AND, NAND, OR, NOR
  - Plus ten other logic operations
- Full look-ahead for high-speed operations on long words
- Switching specifications guaranteed over full temperature and V_{CC} range
- Switching specifications at 500Ω/50 pF
- Advanced oxide-isolated, ion-implanted Schottky TTL process

Connection Diagram

Dual-In-Line Package


INPUTS
OUTPUTS
VCC A1 B1 A2 B2 A3 B3 G Cn+4 P A=B F3
24 23 22 21 20 19 18 17 16 15 14 13
1 2 3 4 5 6 7 8 9 10 11 12
B0 A0 S3 S2 S1 S0 Cn M F0 F1 F2 GND
INPUTS
OUTPUTS

TL/F/6295–1

Order Number DM74AS181BN, NT
See NS Package Number N24A or N24C

Pin Designations

Designation	Pin Nos.	Function
A3, A2, A1, A0	19, 21, 23, 2	Word A Inputs
B3, B2, B1, B0	18, 20, 22, 1	Word B Inputs
S3, S2, S1, S0	3, 4, 5, 6	Function-Select Inputs
C_n	7	Inv. Carry Input
M	8	Mode Control Input
F3, F2, F1, F0	13, 11, 10, 9	Function Outputs
A = B	14	Comparator Output
$\overline{P}$	15	Carry Propagate Output
C_n+4	16	Inv. Carry Output
$\overline{G}$	17	Carry Generate Output
V_{CC}	24	Supply Voltage
GND	12	Ground

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Off-State Output Voltage (A = B only)	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current	All Outputs Except A = B and $\overline{G}$			−2	mA
		$\overline{G}$			−3	
I_{OL}	Low Level Output Current	All Outputs Except $\overline{G}$			20	mA
		$\overline{G}$			48	
V_{OH}	High Level Output Voltage, (A = B Only)				5.5	V
T_A	Free Air Operating Temperature		0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2 mA	Any Output Except A = B	V_{CC} − 2			V
		I_{OH} = −3 mA	$\overline{G}$	2.4	3.4		
I_{OH}	High Level Output Current (A = B)	V_{CC} = 4.5V, V_{OH} = 5.5V				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 20 mA	Any Output Except $\overline{G}$		0.3	0.5	V
		I_{OL} = 48 mA	$\overline{G}$		0.4	0.5	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_{IH} = 7V	Mode			0.1	mA
			Any A or B			0.3	
			S			0.4	
			Carry			0.6	
I_{IH}	High Level Input Current	V_{CC} = Max, V_{IH} = 2.7V	Mode Input			20	μA
			Any S Input			80	
			Any A or B Input			60	
			Carry Input			120	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V	Mode Input			−0.5	mA
			Any S Input			−2	
			Any A or B Input			−1.5	
			Carry Input			−2.5	
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V			70	104	mA

3

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions (Note 2)	From (Input)	To (Output)	Min	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		C_n	C_{n+4}	2	9	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	9	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 4.5V S1 = S2 = 0V ($\overline{SUM}$ mode)	Any A or B	C_{n+4}	2	12	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	12	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 0V S1 = S2 = 4.5V ($\overline{DIFF}$ mode)	Any A or B	C_{n+4}	2	16	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	16	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V ($\overline{SUM}$ or $\overline{DIFF}$ mode)	C_n	Any F	3	9	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				3	9	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 4.5V S1 = S2 = 0V ($\overline{SUM}$ mode)	Any A or B	G	2	7	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	7	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 0V S1 = S2 = 4.5V ($\overline{DIFF}$ mode)	Any A or B	G	2	9	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	9	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 4.5V S1 = S2 = 0V ($\overline{SUM}$ mode)	Any A or B	P	2	8	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	8	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 0V S1 = S2 = 4.5V ($\overline{DIFF}$ mode)	Any A or B	P	2	10	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	10	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 4.5V S1 = S2 = 0V ($\overline{SUM}$ mode)	A_i or B_i	F_i	2	8	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	8	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 0V S1 = S2 = 4.5V ($\overline{DIFF}$ mode)	A_i or B_i	F_i	2	10	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	10	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 4.5V (logic mode)	A_i or B_i	F_i	2	11	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	11	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 0V S1 = S2 = 4.5V ($\overline{DIFF}$ mode)	Any A or B	A = B	4	21	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				4	21	

Note 1: See Section 1 for test waveforms and output load.

Note 2: V_{CC} = 4.5V to 5.5V, C_L = 50 pF (15 pF for A = B), R_L = 500Ω (280Ω for A = B).

Dynamic Parameter Measurement Information

Logic Mode Test Table
Function Inputs: S1 = S2 = M = 4.5V, S0 = S3 = 0V

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH} t_{PHL}	A_i	B_i	None	None	Remaining A and B, C_n	F_i	Out-of-Phase
t_{PLH} t_{PHL}	B_i	A_i	None	None	Remaining A and B, C_n	F_i	Out-of-Phase

$\overline{\text{SUM}}$ Mode Test Table
Function Inputs: S0 = S3 = 4.5V, S1 = S2 = M = 0V

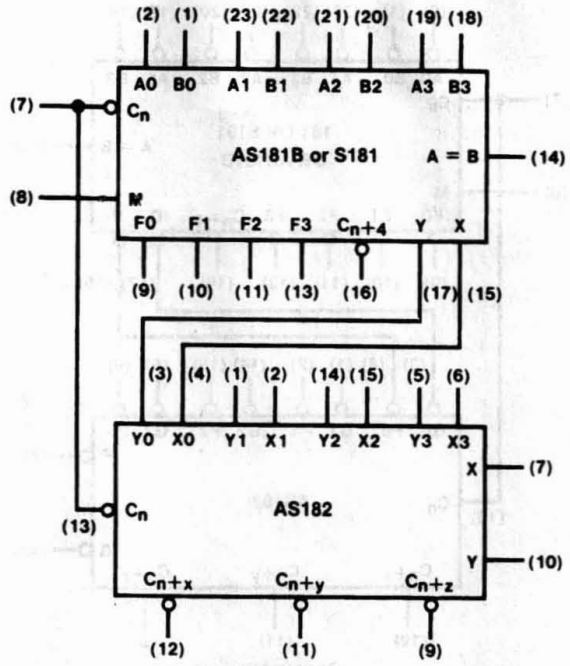
Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH} t_{PHL}	A_i	B_i	None	Remaining A and B	C_n	F_i	In-Phase
t_{PLH} t_{PHL}	B_i	A_i	None	Remaining A and B	C_n	F_i	In-Phase
t_{PLH} t_{PHL}	A_i	B_i	None	None	Remaining A and B, C_n	P	In-Phase
t_{PLH} t_{PHL}	B_i	A_i	None	None	Remaining A and B, C_n	P	In-Phase
t_{PLH} t_{PHL}	A_i	None	B_i	Remaining B	Remaining A, C_n	G	In-Phase
t_{PLH} t_{PHL}	B_i	None	A_i	Remaining B	Remaining A, C_n	G	In-Phase
t_{PLH} t_{PHL}	C_n	None	None	All A	All B	Any F or C_n+4	In-Phase
t_{PLH} t_{PHL}	A_i	None	B_i	Remaining B	Remaining A, C_n	C_n+4	Out-of-Phase
t_{PLH} t_{PHL}	B_i	None	A_i	Remaining B	Remaining A, C_n	C_n+4	Out-of-Phase

Dynamic Parameter Measurement Information (Continued)

$\overline{\text{DIFF}}$ Mode Test Table
Function Inputs: S1 = S2 = 4.5V, S0 = S3 = M = 0V

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH} / t_{PHL}	A_i	None	B_i	Remaining A	Remaining B, C_n	F_i	In-Phase
t_{PLH} / t_{PHL}	B_i	A_i	None	Remaining A	Remaining B, C_n	F_i	Out-of-Phase
t_{PLH} / t_{PHL}	A_i	None	B_i	None	Remaining A and B, C_n	P	In-Phase
t_{PLH} / t_{PHL}	B_i	A_i	None	None	Remaining A and B, C_n	P	Out-of-Phase
t_{PLH} / t_{PHL}	A_i	B_i	None	None	Remaining A and B, C_n	G	In-Phase
t_{PLH} / t_{PHL}	B_i	None	A_i	None	Remaining A and B, C_n	G	Out-of-Phase
t_{PLH} / t_{PHL}	A_i	None	B_i	Remaining A	Remaining B, C_n	A = B	In-Phase
t_{PLH} / t_{PHL}	B_i	A_i	None	Remaining A	Remaining B, C_n	A = B	Out-of-Phase
t_{PLH} / t_{PHL}	C_n	None	None	All A and B	None	C_n+4 or any F	In-Phase
t_{PLH} / t_{PHL}	A_i	B_i	None	None	Remaining A, B, C_n	C_n+4	Out-of-Phase
t_{PLH} / t_{PHL}	B_i	None	A_i	None	Remaining A, B, C_n	C_n+4	In-Phase

General Description (Continued)



TL/F/6295–2

FIGURE 1

TABLE I

Selection				Active High Data		
				M = H	M = L; Arithmetic Operations	
S3	S2	S1	S0	Logic Functions	C_n = H (no carry)	C_n = L (with carry)
L	L	L	L	F = $\overline{A}$	F = A	F = A Plus 1
L	L	L	H	F = $\overline{A + B}$	F = A + B	F = (A + B) Plus 1
L	L	H	L	F = $\overline{AB}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) Plus 1
L	L	H	H	F = 0	F = Minus 1 (2's Compl)	F = Zero
L	H	L	L	F = $\overline{AB}$	F = A Plus A$\overline{B}$	F = A Plus A$\overline{B}$ Plus 1
L	H	L	H	F = $\overline{B}$	F = (A + B) Plus A$\overline{B}$	F = (A + B) Plus A$\overline{B}$ Plus 1
L	H	H	L	F = A ⊕ B	F = A Minus B Minus 1	F = A Minus B
L	H	H	H	F = A$\overline{B}$	F = A$\overline{B}$ Minus 1	F = A$\overline{B}$
H	L	L	L	F = $\overline{A}$ + B	F = A Plus AB	F = A Plus AB Plus 1
H	L	L	H	F = $\overline{A \oplus B}$	F = A Plus B	F = A Plus B Plus 1
H	L	H	L	F = B	F = (A + $\overline{B}$) Plus AB	F = (A + $\overline{B}$) Plus AB Plus 1
H	L	H	H	F = AB	F = AB Minus 1	F = AB
H	H	L	L	F = 1	F = A Plus A*	F = A Plus A Plus 1
H	H	L	H	F = A + $\overline{B}$	F = (A + B) Plus A	F = (A + B) Plus A Plus 1
H	H	H	L	F = A + B	F = (A + $\overline{B}$) Plus A	F = (A + $\overline{B}$) Plus A Plus 1
H	H	H	H	F = A	F = A Minus 1	F = A

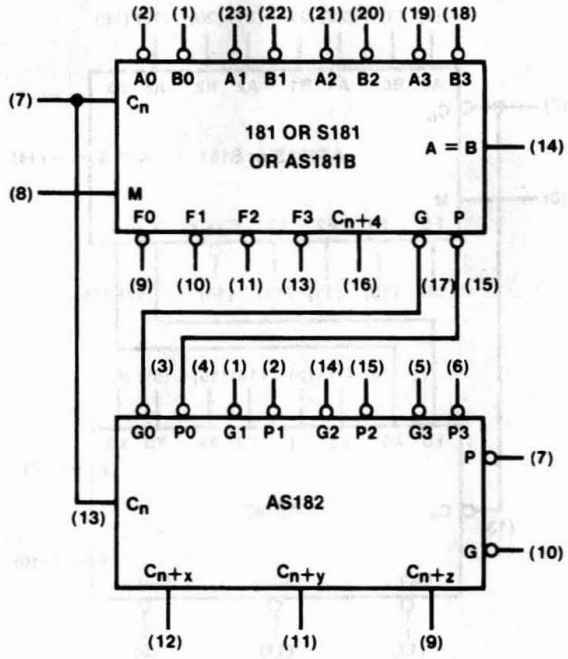
*Each bit is shifted to the next more significant position.

Input C_n	Output C_n+4	Active-High Data *(Figure 1)*
H	H	A ≤ B
H	L	A > B
L	H	A < B
L	L	A ≥ B

Pin Number	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-High Data (Table I)	A0	B0	A1	B1	A2	B2	A3	B3	F0	F1	F2	F3	$\overline{C}_n$	$\overline{C}_n+4$	X	Y

3

General Description (Continued)



TL/F/6295–3

FIGURE 2

TABLE II

Selection				Active Low Data		
				M = H	M = L; Arithmetic Operations	
S3	S2	S1	S0	Logic Functions	C_n = L (no carry)	C_n = H (with carry)
L	L	L	L	F = $\overline{A}$	F = A Minus 1	F = A
L	L	L	H	F = $\overline{AB}$	F = AB Minus 1	F = AB
L	L	H	L	F = $\overline{A}$ + B	F = A$\overline{B}$ Minus 1	F = A$\overline{B}$
L	L	H	H	F = 1	F = Minus 1 (2's Compl)	F = Zero
L	H	L	L	F = $\overline{A + B}$	F = A Plus (A + $\overline{B}$)	F = A Plus (A + $\overline{B}$) Plus 1
L	H	L	H	F = $\overline{B}$	F = AB Plus (A + B)	F = AB Plus (A + $\overline{B}$) Plus 1
L	H	H	L	F = $\overline{A \oplus B}$	F = A Minus B Minus 1	F = A Minus B
L	H	H	H	F = A + $\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) Plus 1
H	L	L	L	F = $\overline{A}$B	F = A Plus (A + B)	F = A Plus (A + B) Plus 1
H	L	L	H	F = A ⊕ B	F = A Plus B	F = A Plus B Plus 1
H	L	H	L	F = B	F = A$\overline{B}$ Plus (A + B)	F = A$\overline{B}$ Plus (A + B) Plus 1
H	L	H	H	F = A + B	F = A + B	F = (A + B) Plus 1
H	H	L	L	F = 0	F = A Plus A*	F = A Plus A Plus 1
H	H	L	H	F = A$\overline{B}$	F = AB Plus A	F = AB Plus A Plus 1
H	H	H	L	F = AB	F = A$\overline{B}$ Plus A	F = A$\overline{B}$ Plus A Plus 1
H	H	H	H	F = A	F = A	F = A Plus 1

*Each bit is shifted to the next more significant position.

Input C_n	Output C_{n+4}	Active-Low Data *(Figure 2)*
H	H	A ≥ B
H	L	A < B
L	H	A > B
L	L	A ≤ B

Pin Number	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-Low Data (Table II)	$\overline{A}$0	$\overline{B}$0	$\overline{A}$1	$\overline{B}$1	$\overline{A}$2	$\overline{B}$2	$\overline{A}$3	$\overline{B}$3	$\overline{F}$0	$\overline{F}$1	$\overline{F}$2	$\overline{F}$3	C_n	C_{n+4}	$\overline{P}$	$\overline{G}$

General Description (Continued)

If high speed is not important, a ripple-carry input (C_n) and a ripple-carry output (C_n+4) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

These circuits will accommodate active-high or active-low data, if the pin designations are interpreted as shown below.

Subtraction is accomplished by 1's complement addition, where the 1's complement of the subtrahend is generated internally. The resultant output is A—B—1, which requires an end-around or forced carry to provide A—B.

The AS181B can also be utilized as a comparator. The A = B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A = B). The ALU should be in the subtract mode with C_n = H when performing this comparison. The A = B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_n+4) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the function select inputs S3, S2, S1, S0 at L, H, H, L, respectively.

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables I and II and include exclusive-OR, NAND, AND, NOR, and OR functions.

ALU SIGNAL DESIGNATIONS

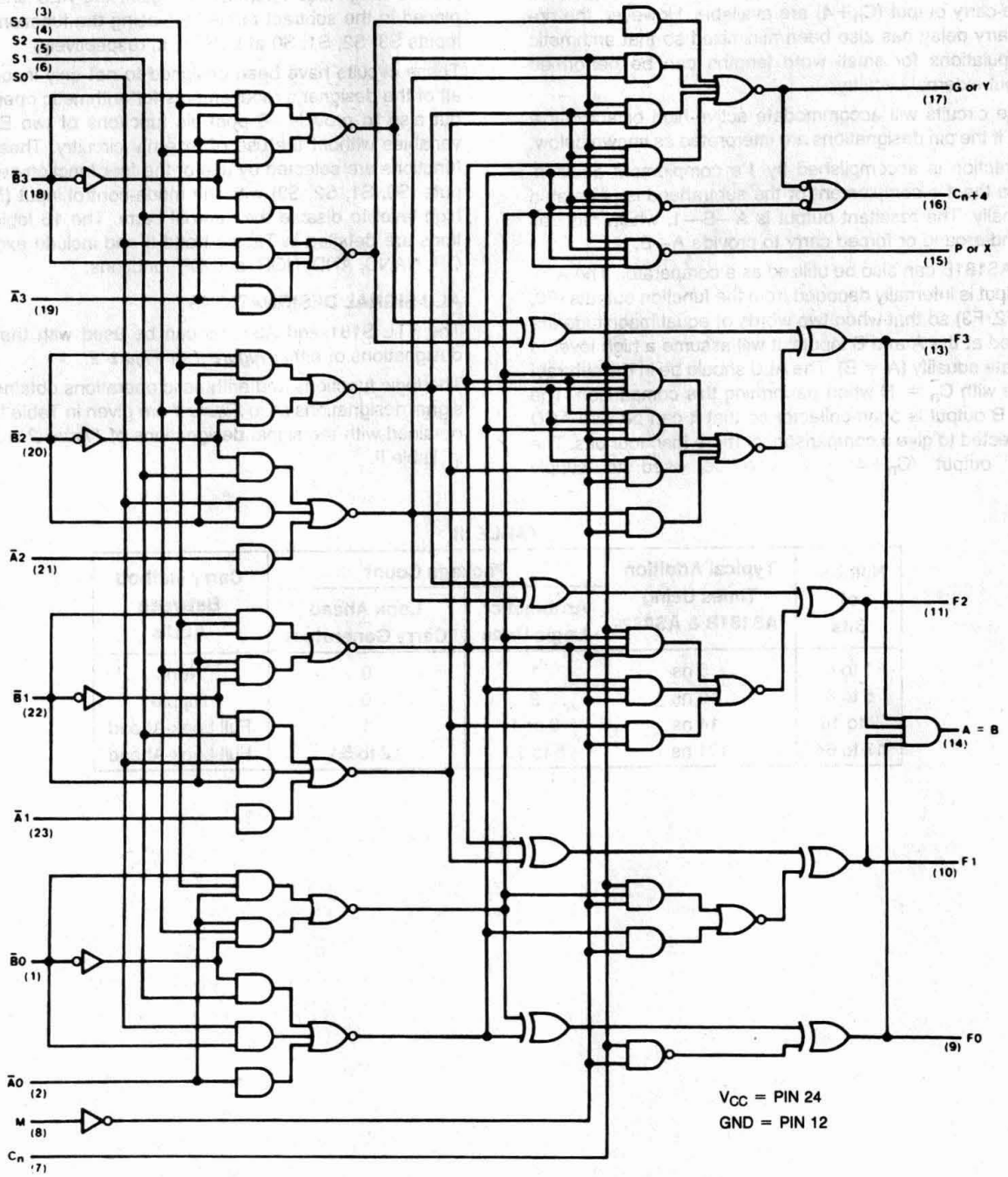
The TTL S181 and AS181B can be used with the signal designations of either *Figure 1* or *Figure 2*.

The logic functions and arithmetic operations obtained with signal designations as in *Figure 1* are given in Table I; those obtained with the signal designations of *Figure 2* are given in Table II.

TABLE III

Number of Bits	Typical Addition Times Using AS181B & AS882	Package Count		Carry Method Between ALU's
		Arithmetic/ Logic Units	Look Ahead Carry Generators	
1 to 4	5 ns	1	0	None
5 to 8	10 ns	2	0	Ripple
9 to 16	14 ns	3 or 4	1	Full Look-Ahead
17 to 64	101 ns	5 to 16	2 to 5	Full Look-Ahead

Logic Diagram



TL/F/6295–4

National Semiconductor Corporation

DM74AS182 Look-Ahead Carry Generators

General Description

These circuits are high-speed, look-ahead carry generators, capable of anticipating a carry across four binary adders or groups of adders. They are cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as shown in the pin designation table.

When used in conjunction with the AS181B arithmetic logic unit, these generators provide high-speed carry look-ahead capability for any word length. Each AS182 generates the look-ahead (anticipated carry) across a group of four ALUs and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits. The method of cascading circuits to perform multi-level look-ahead is illustrated under typical application data.

Carry input and output of the ALUs are in their true form, and the carry propagate (P) and carry generate (G) are in negated form; therefore, the carry functions (inputs, outputs, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connection to the ALU. Reinterpretations of carry functions, as explained on the 181 data sheet are also applicable to and compatible with the look-ahead generator. Positive logic equations for the AS182 are:

$$C_{n+x} = G0 + P0\ C_n$$

$$C_{n+y} = G1 + P1\ G0 + P1\ P0\ C_n$$

$$C_{n+z} = G2 + P2\ G1 + P2\ P1\ G0 + P2\ P1\ P0\ C_n$$

$$\overline{G} = \overline{G3 + P3 \cdot G2 + P3 \cdot P2 \cdot G1 + P3 \cdot P2 \cdot P1 \cdot G0}$$

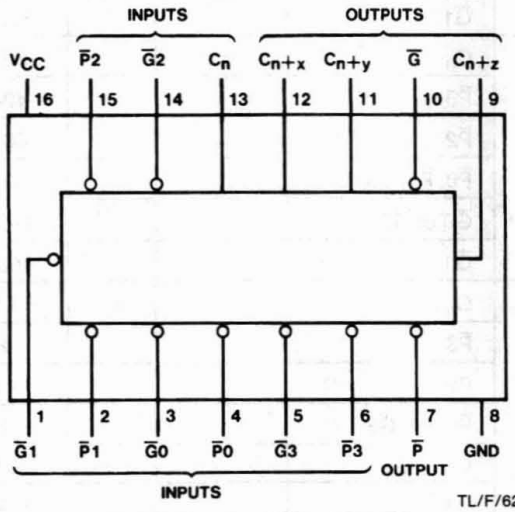
$$\overline{P} = \overline{P3\ P2\ P1\ P0}$$

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Offers carry functions in a compatible form for direct connection to the ALU
- Cascadable to perform look-ahead across n-bit adders
- PNP inputs reduce input loading
- Improved AC performance over Schottky at reduced power consumption

Connection Diagram

Dual-In-Line Package



TL/F/6296–1

Order Number DM74AS182N
See NS Package Number N16A*

Pin Designations

Designation	Pin Nos.	Function
$\overline{G0}, \overline{G1}, \overline{G2}, \overline{G3}$	3, 1, 14, 5	Active Low Carry Generate Inputs
$\overline{P0}, \overline{P1}, \overline{P2}, \overline{P3}$	4, 2, 15, 6	Active Low Carry Propagate Inputs
C_n	13	Carry Input
$C_{n+x}, C_{n+y}, C_{n+z}$	12, 11, 9	Carry Outputs
$\overline{G}$	10	Active Low Carry Generate Output
$\overline{P}$	7	Active Low Carry Propagate Output
V_{CC}	16	Supply Voltage
GND	8	Ground

*Contact your local NSC representative about surface mount (M) package availability.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−2	mA
I_{OL}	Low Level Output Current			20	mA
T_A	Free Air Operating Temperature Range	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2 mA		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 20 mA			0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V	$\overline{P}3$			200	μA
			C_n, $\overline{P}2$			300	
			$\overline{P}0$, $\overline{P}1$, $\overline{G}3$			400	
			$\overline{G}0$, $\overline{G}2$			700	
			$\overline{G}1$			800	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	C_n			60	μA
			$\overline{P}3$			40	
			$\overline{P}2$			60	
			$\overline{P}0$, $\overline{P}1$, $\overline{G}3$			80	
			$\overline{G}0$ or $\overline{G}2$			140	
			$\overline{G}1$			160	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	C_n			−1.5	mA
			$\overline{P}3$			−1	
			$\overline{P}2$			−1.5	
			$\overline{P}0$, $\overline{P}1$, $\overline{G}3$			−2	
			$\overline{G}0$ or $\overline{G}2$			−3.5	
			$\overline{G}1$			−4	
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High (1)		16	25	mA
			Outputs Low (2)		23	36	

Note 1: I_{CCH} is measured with all outputs open, inputs P3 and G3 at 4.5V, and all other inputs grounded.

Note 2: I_{CCL} is measured with all outputs open, inputs G0, G1, and G2 at 4.5V, and all other inputs grounded.

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	From (Input)	To (Output)	Conditions	Min	Max	25°C, 5V Max	Units
t_{PLH}	Propagation Delay Time, Low to High Level Output	$\overline{G}0$, $\overline{G}1$, $\overline{G}2$, $\overline{G}3$, $\overline{P}0$, $\overline{P}1$, $\overline{P}2$, or $\overline{P}3$	C_{n+x}, C_{n+y}, or C_{n+z}	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R_L = 500Ω	3	10.5	9.5	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output				2	6	6	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	$\overline{G}0$, $\overline{G}1$, $\overline{G}2$, $\overline{G}3$, $\overline{P}1$, $\overline{P}2$, or $\overline{P}3$	$\overline{G}$		3	12	11	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output				2	8	7.5	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	$\overline{P}0$, $\overline{P}1$, $\overline{P}2$, or $\overline{P}3$	$\overline{P}$		2	7.5	7	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output				2	6	5.5	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	C_n	C_{n+x}, C_{n+y}, or C_{n+z}		3	10	9	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output				3	9.5	9	ns

Note 1: See Section 1 for test waveforms and output load.

Function Tables

Inputs							Output
$\overline{G}3$	$\overline{G}2$	$\overline{G}1$	$\overline{G}0$	$\overline{P}3$	$\overline{P}2$	$\overline{P}1$	$\overline{G}$
L	X	X	X	X	X	X	L
X	L	X	X	L	X	X	L
X	X	L	X	L	L	X	L
X	X	X	L	L	L	L	L
All Other Combinations							H

Inputs				Output
$\overline{P}3$	$\overline{P}2$	$\overline{P}1$	$\overline{P}0$	$\overline{P}$
L	L	L	L	L
All Other Combinations				H

Inputs							Output
$\overline{G}2$	$\overline{G}1$	$\overline{G}0$	$\overline{P}2$	$\overline{P}1$	$\overline{P}0$	C_n	C_{n+z}
L	X	X	X	X	X	X	H
X	L	X	L	X	X	X	H
X	X	L	L	L	X	X	H
X	X	X	L	L	L	H	H
All Other Combinations							L

Inputs			Output
$\overline{G}0$	$\overline{P}0$	C_n	C_{n+x}
L	X	X	H
X	L	H	H
All Other Combinations			L

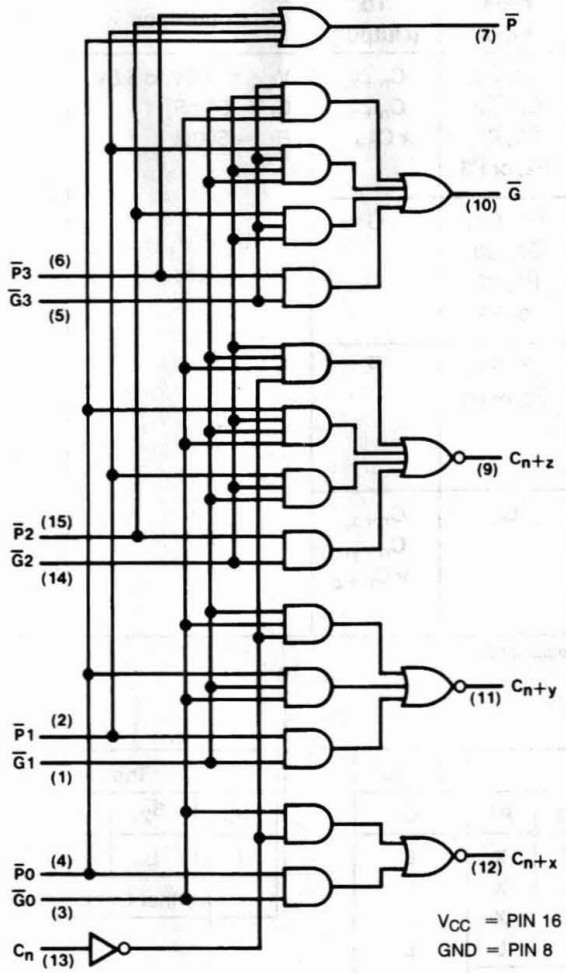
Inputs					Output
$\overline{G}1$	$\overline{G}0$	$\overline{P}1$	$\overline{P}0$	C_n	C_{n+y}
L	X	X	X	X	H
X	L	L	X	X	H
X	X	L	L	H	H
All Other Combinations					L

H = High level, L = Low level, X = irrelevant

Any inputs not shown in a given table are irrelevant with respect to that output.

3

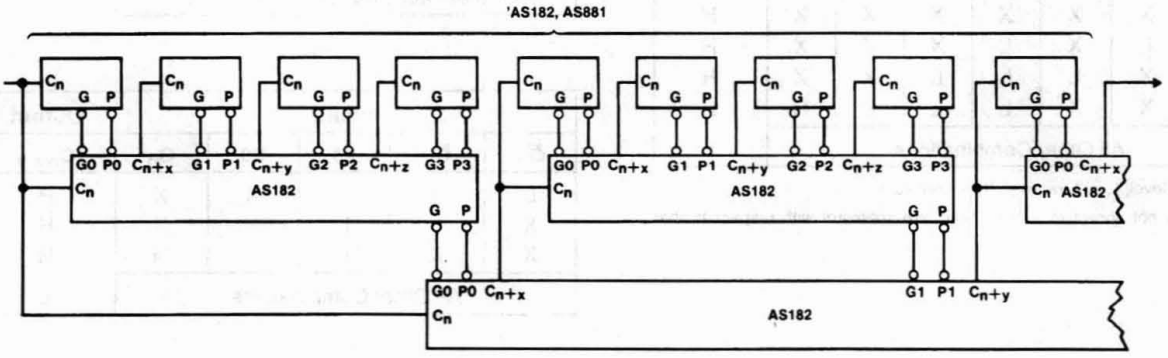
Logic Diagram



TL/F/6296–2

Typical Application

64-Bit ALU, Full-Carry Look-Ahead in Three Levels



A and B inputs and F outputs of AS181B are not shown.

TL/F/6296–3

National Semiconductor Corporation

DM74AS230/DM74AS231 TRI-STATE® Bus Drivers/Receivers

General Description

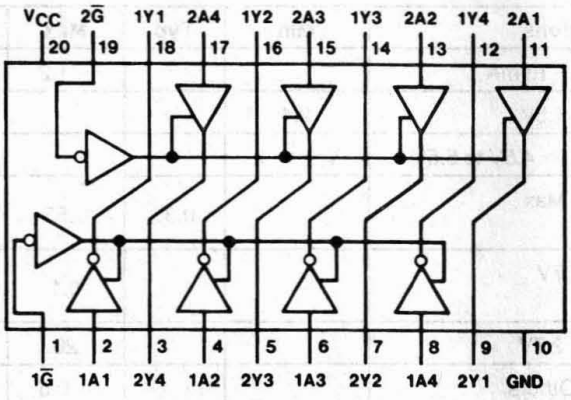
This family of Advanced Schottky TRI-STATE Bus circuits are designed to provide either bidirectional or unidirectional buffer interface in Memory, Microprocessor, and Communication Systems. The output characteristics of the circuits have low impedance sufficient to drive terminated transmission lines down to 133 ohms. The input characteristics of the circuits likewise have a high impedance so it will not significantly load the transmission line. The package contains eight TRI-STATE buffers organized with four buffers having a common TRI-STATE enable gate. The AS230 is organized as 4 bit buffers inverting and 4 bit buffers non inverting. The AS231 is organized as two 4 bit wide inverting buffers with separate complementary output control buffers.

Features

- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Improved switching performance over low power Schottky counterpart
- Functional and pin compatible with low power Schottky counterpart
- Switching response specified into 500Ω and 50 pF
- Low level drive current 74AS = 48 mA
- Specified to interface with CMOS at $V_{OH} = V_{CC} - 2V$

Connection Diagrams

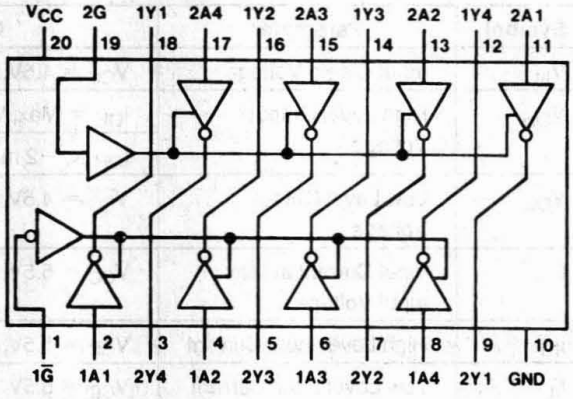
Dual-In-Line Package



TL/F/6297–1

Order Number DM74AS230N
See NS Package Number N20A*

Dual-In-Line Package



TL/F/6297–2

Order Number DM74AS231N
See NS Package Number N20A*

Function Tables

'AS230

Inputs		Outputs	
$\overline{G}$	A	1Y	2Y
L	L	H	L
L	H	L	H
H	X	Z	Z

'AS231

Inputs		Output
$1\overline{G}$	1A	1Y
L	L	H
L	H	L
H	X	Z

'AS231

Inputs		Output
2G	2A	2Y
H	L	H
H	H	L
L	X	Z

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
Z = High Impedance (off)

*Contact your local NSC representative about surface mount (M) package availability.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Voltage Applied to Disabled Output	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM74AS 230, 231			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−15	mA
I_{OL}	Low Level Output Current			−64	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = Max, V_{CC} = 4.5V		2.4			V
		I_{OH} = −2 mA, V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = Max			0.35	0.55	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IN} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IN} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V	Others			−0.5	mA
			AS230 2A Inputs			−1	
I_{OZH}	High Level TRI-STATE Output Current	V_{CC} = 5.5V, V_O = 2.7V				50	μA
I_{OZL}	Low Level TRI-STATE Output Current	V_{CC} = 5.5V, V_O = 0.4V				−50	μA
I_O	Output Drive Current	V_{CC} = 5.5V, V_{OUT} = 2.25V		−50		−150	mA
I_{CC}	74AS230 Supply Current	V_{CC} = 5.5V	Outputs High		16	25	mA
			Outputs Low		55	87	
			TRI-STATE		29	46	
I_{CC}	74AS231 Supply Current	V_{CC} = 5.5V	Outputs High		12	18	mA
			Outputs Low		52	82	
			TRI-STATE		25	39	

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	From (Input)	To (Output)	Conditions	DM74AS230		Units
					Min	Max	
t_{PLH}	Propagation Delay Time Low-to-High Level Output	1A	1Y	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	2.5	6.5	ns
t_{PHL}	Propagation Delay Time High-to-Low Level Output				2	5.7	
t_{PLH}	Propagation Delay Time Low-to-High Level Output	2A	2Y		2.5	6.2	ns
t_{PHL}	Propagation Delay Time High-to-Low Level Output				2	6.2	
t_{PZH}	Output Enable to High Level	$1\overline{G}$	1Y		2	6.4	ns
t_{PZL}	Output Enable to Low Level				2	8.5	
t_{PHZ}	Output Disable from High Level				2	5	
t_{PLZ}	Output Disable from Low Level				2	9.5	
t_{PZH}	Output Enable to High Level	$2\overline{G}$	2Y		2	9	ns
t_{PZL}	Output Enable to Low Level				2	7.5	
t_{PHZ}	Output Disable from High Level				2	6	
t_{PLZ}	Output Disable from Low Level				2	9	

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	From (Input)	To (Output)	Conditions	DM74AS231		Units
					Min	Max	
t_{PLH}	Propagation Delay Time Low-to-High Level Output	A	Y	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	2	6.5	ns
t_{PHL}	Propagation Delay Time High-to-Low Level Output				2	5.7	
t_{PZH}	Output Enable to High Level	$\overline{G}$	Y		2	6.4	ns
t_{PZL}	Output Enable to Low Level				2	8.5	
t_{PHZ}	Output Disable from High Level				2	5	
t_{PLZ}	Output Disable from Low Level				2	9.5	
t_{PZH}	Output Enable to High Level	G	Y		3	6	ns
t_{PZL}	Output Enable to Low Level				3	9	
t_{PHZ}	Output Disable from High Level				3	6	
t_{PLZ}	Output Disable from Low Level				3	7	

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM74AS240, 241, 242, 243, 244 TRI-STATE® Bus Drivers/Receivers

General Description

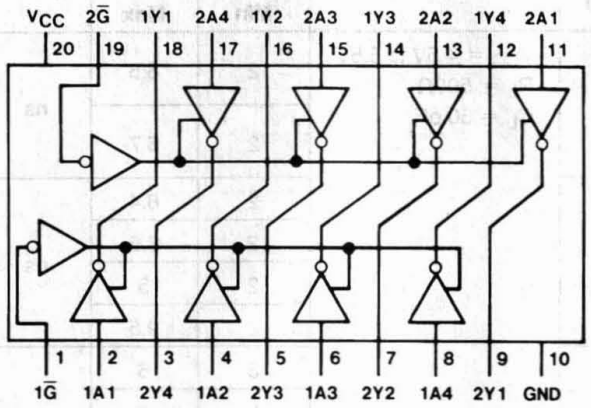
This family of Advance Schottky TRI-STATE Bus circuits are designed to provide either bidirectional or unidirectional buffer interface in Memory, Microprocessor, and Communication Systems. The output characteristics of the circuits have low impedance sufficient to drive terminated transmission lines down to 133 ohms. The input characteristics of the circuits likewise have a high impedance so it will not significantly load the transmission line. The package contains eight TRI-STATE buffers organized with four buffers having a common TRI-STATE enable gate. The AS240, 241 and 244 are eight wide in a 20 pin package, and may be used as a 4 wide bidirectional or eight wide unidirectional. The AS242 and 243 are organized four wide bidirectional in a 14 pin package. The buffer selection includes inverting and non-inverting, with enable or disable TRI-STATE control.

Features

- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Improved switching performance with less power dissipation compared with Schottky counterpart
- Functional and pin compatible with 54/74LS and Schottky counterpart
- Switching response specified into 500 ohm and 50 pF
- Specified to interface with CMOS at $V_{OH} = V_{CC} - 2V$

Connection Diagrams

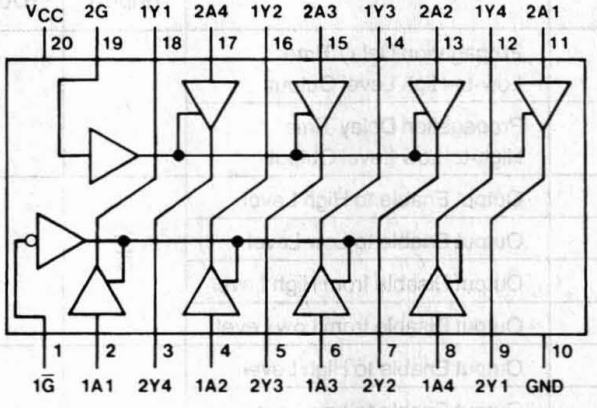
Dual-In-Line Package



TL/F/6298–1

Order Number DM74AS240N
See NS Package Number N20A*

Dual-In-Line Package



TL/F/6298–2

Order Number DM74AS241N
See NS Package Number N20A*

*Contact your local NSC representative about surface mount (M) package availability.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V_{CC}	7V
Input Voltage	7V
Voltage Applied to Disabled Output	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

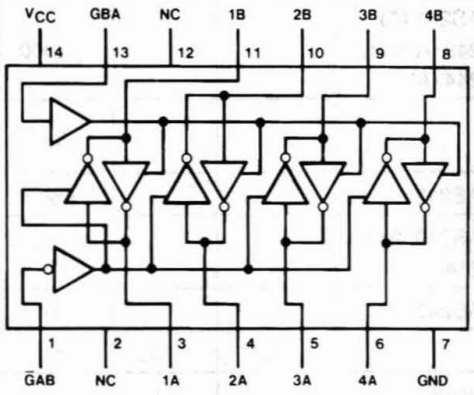
Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−15	mA
I_{OL}	Low Level Output Current			64	mA
T_A	Free Air Operating Temperature	0		70	°C

Connection Diagrams (Continued)

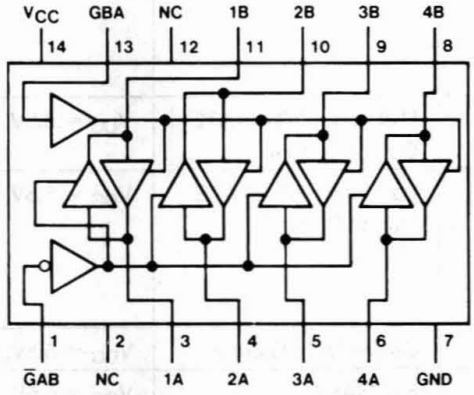
Dual-In-Line Package



TL/F/6298–3

Order Number DM74AS242N
See NS Package Number N14A*

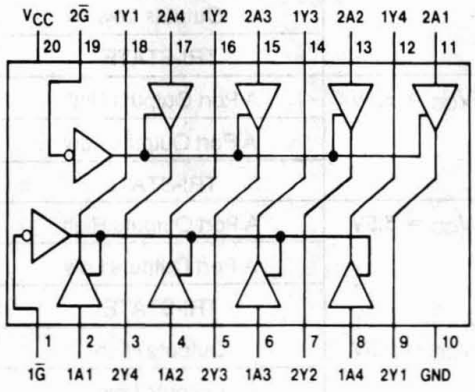
Dual-In-Line Package



TL/F/6298–4

Order Number DM74AS243N
See NS Package Number N14A*

Dual-In-Line Package



TL/F/6298–5

Order Number DM74AS244WM, N
See NS Package Number M20B or N20A

*Contact your local NSC representative about surface mount (M) package availability.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions			Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18 mA					−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, I_{OH} = −3 mA			2.4	3.2		V
		V_{CC} = 4.5V, I_{OH} = Max			2.4			
		I_{OH} = −2 mA, V_{CC} = 4.5V to 5.5V			V_{CC}−2			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = Max				0.35	0.55	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V	V_{IN} = 7V	Others			100	µA
			V_{IN} = 5.5V	For AS242, 243 (A or B)				
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IN} = 2.7V		AS242, 243 (A or B)			70	µA
				Others			20	
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V		AS240, 241 (G, $\overline{G}$), 242, 243 (Control Inputs), 244 ($\overline{G}$)			−500	µA
				AS241 (A), 243 (A or B), 244 (A)			−1000	
I_{OZH}	High Level TRI-STATE Output Current	V_{CC} = 5.5V, V= 2.7V					50	µA
I_{OZL}	Low Level TRI-STATE Output Current	V_{CC} = 5.5V, V = 0.4V		AS242			−500	µA
				AS240, 241, 244			−50	
				AS243			−1000	
I_O	Output Drive Current	V_{CC} = 5.5V, V_{OUT} = 2.25V			−50	−115	−150	mA
I_{CC}	54/74AS240 Supply Current	V_{CC} = 5.5V	Outputs High			11	17	mA
			Outputs Low			51	75	
			TRI-STATE			24	38	
I_{CC}	54/74AS241 Supply Current	V_{CC} = 5.5V	Outputs High			22	35	mA
			Outputs Low			61	90	
			TRI-STATE			35	56	
I_{CC}	54/74AS242 Supply Current	V_{CC} = 5.5V	A Port Outputs High			18	28	mA
			A Port Outputs Low			38	60	
			TRI-STATE			25	39	
I_{CC}	54/74AS243 Supply Current	V_{CC} = 5.5V	A Port Outputs High			28	44	mA
			A Port Outputs Low			47	74	
			TRI-STATE			35	56	
I_{CC}	54/74AS244 Supply Current	V_{CC} = 5.5V	Outputs High			22	34	mA
			Outputs Low			60	90	
			TRI-STATE			34	54	

'AS240 Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From (Input)	To (Output)	Min	Max	Units
t_{PLH}	Propagation Delay Time Low-to-High Level Output	V_{CC} = 4.5V to 5.5V $R_1 = R_2 = 500\Omega$ C_L = 50 pF	A	Y	2	6.5	ns
t_{PHL}	Propagation Delay Time High-to-Low Level Output		A	Y	2	5.7	ns
t_{PZL}	Output Enable to Low Level		$\overline{G}$	Y	2	9	ns
t_{PZH}	Output Enable to High Level		$\overline{G}$	Y	2	6.4	ns
t_{PLZ}	Output Disable from Low Level		$\overline{G}$	Y	2	9.5	ns
t_{PHZ}	Output Disable from High Level		$\overline{G}$	Y	2	5	ns

'AS241 Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From (Input)	To (Output)	Min	Max	Units
t_{PLH}	Propagation Delay Time Low-to-High Level Output	V_{CC} = 4.5V to 5.5V $R_1 = R_2 = 500\Omega$ C_L = 50 pF	A	Y	2	6.2	ns
t_{PHL}	Propagation Delay Time High-to-Low Level Output		A	Y	2	6.2	ns
t_{PZL}	Output Enable to Low Level		$1\overline{G}$	Y	2	7.5	ns
t_{PZH}	Output Enable to High Level		$1\overline{G}$	Y	2	9	ns
t_{PLZ}	Output Disable from Low Level		$1\overline{G}$	Y	2	9	ns
t_{PHZ}	Output Disable from High Level		$1\overline{G}$	Y	2	6	ns
t_{PZL}	Output Enable to Low Level		2G	Y	3	8.5	ns
t_{PZH}	Output Enable to High Level		2G	Y	3	10.5	ns
t_{PLZ}	Output Disable from Low Level		2G	Y	3	12	ns
t_{PHZ}	Output Disable from High Level		2G	Y	3	7	ns

'AS242 Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From (Input)	To (Output)	Min	Max	Units
t_{PLH}	Propagation Delay Time Low-to-High Level Output	V_{CC} = 4.5V to 5.5V $R_1 = R_2 = 500\Omega$ C_L = 50 pF	A or B	B or A	2	6.5	ns
t_{PHL}	Propagation Delay Time High-to-Low Level Output		A or B	B or A	2	5.7	ns
t_{PZL}	Output Enable to Low Level		GBA	A	3	8	ns
t_{PZH}	Output Enable to High Level		GBA	A	3	6	ns
t_{PLZ}	Output Disable from Low Level		GBA	A	3	10.5	ns
t_{PHZ}	Output Disable from High Level		GBA	A	3	6	ns
t_{PZL}	Output Enable to Low Level		$\overline{G}$AB	B	2	7.5	ns
t_{PZH}	Output Enable to High Level		$\overline{G}$AB	B	2	5.5	ns
t_{PLZ}	Output Disable from Low Level		$\overline{G}$AB	B	2	9.5	ns
t_{PHZ}	Output Disable from High Level		$\overline{G}$AB	B	2	6.5	ns

'AS243 Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From (Input)	To (Output)	Min	Max	Units
t_{PLH}	Propagation Delay Time Low-to-High Level Output	V_{CC} = 4.5V to 5.5V $R_1 = R_2 = 500\Omega$ C_L = 50 pF	A or B	B or A	3	7.5	ns
t_{PHL}	Propagation Delay Time High-to-Low Level Output		A or B	B or A	3	6.5	ns
t_{PZL}	Output Enable to Low Level		$\overline{G}$AB	B	2	7.5	ns
t_{PZH}	Output Enable to High Level		$\overline{G}$AB	B	2	9	ns
t_{PLZ}	Output Disable from Low Level		$\overline{G}$AB	B	2	9	ns
t_{PHZ}	Output Disable from High Level		$\overline{G}$AB	B	2	6.5	ns
t_{PZL}	Output Enable to Low Level		GBA	A	3	8.5	ns
t_{PZH}	Output Enable to High Level		GBA	A	3	10.5	ns
t_{PLZ}	Output Disable from Low Level		GBA	A	3	11	ns
t_{PHZ}	Output Disable from High Level		GBA	A	3	7	ns

'AS244 Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From (Input)	To (Output)	Min	Max	Units
t_{PLH}	Propagation Delay Time Low-to-High Level Output	V_{CC} = 4.5V to 5.5V $R_1 = R_2 = 500\Omega$ C_L = 50 pF	A	Y	2	6.2	ns
t_{PHL}	Propagation Delay Time High-to-Low Level Output		A	Y	2	6.2	ns
t_{PZL}	Output Enable to Low Level		$\overline{G}$	Y	2	7.5	ns
t_{PZH}	Output Enable to High Level		$\overline{G}$	Y	2	9	ns
t_{PLZ}	Output Disable from Low Level		$\overline{G}$	Y	2	9	ns
t_{PHZ}	Output Disable from High Level		$\overline{G}$	Y	2	6	ns

Note 1: See Section 1 for test waveforms and output load.

Function Tables

AS240

Inputs		Output
$\overline{G}$	A	Y
L	L	H
L	H	L
H	X	Z

AS241

Inputs				Outputs	
2G	$1\overline{G}$	1A	2A	1Y	2Y
X	L	L	X	L	
X	L	H	X	H	
X	H	X	X	Z	
H	X	X	L		L
H	X	X	H		H
L	X	X	X		Z

AS244

Inputs		Output
$\overline{G}$	A	Y
L	L	L
L	H	H
H	X	Z

L = Low Logic Level
H = High Logic Level
X = Either Low or High Logic Level
Z = High Impedance

AS242, AS243

INPUTS		'AS242	'AS243
$\overline{G}AB$	GBA		
L	L	$\overline{A}$ to B	A to B
H	H	$\overline{B}$ to A	B to A
H	L	Isolation	Isolation
L	H	Latch A and B ($A = \overline{B}$)	Latch A and B ($A = B$)

National Semiconductor Corporation

DM74AS245 Octal TRI-STATE® Bus Transceivers

General Description

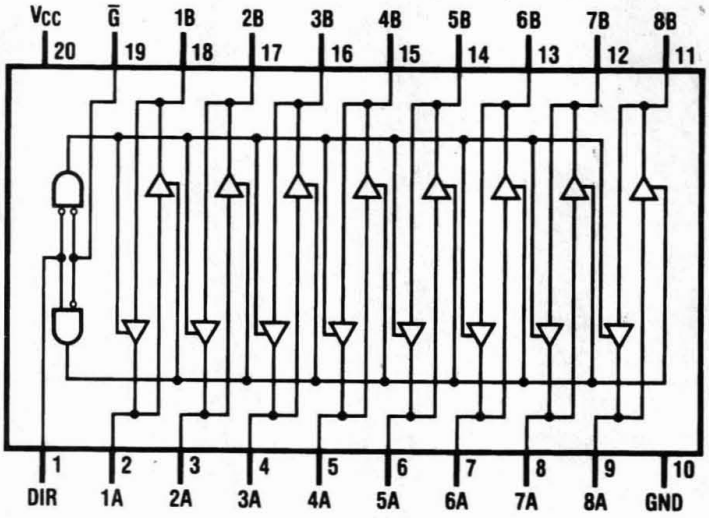
This advanced Schottky device contains 8 pairs of TRI-STATE logic elements configured as octal bus transceivers. These circuits are designed for use in memory, microprocessor systems and in asynchronous bidirectional data buses. Two way communication between buses is controlled by the (DIR) input. Data transmits either from the A bus to the B bus or from the B bus to the A bus. Both the driver and receiver outputs can be disabled via the ($\overline{G}$) enable input which causes outputs to enter the high impedance mode so that the buses are effectively isolated.

Features

- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Non-inverting logic output
- TRI-STATE outputs independently controlled on A and B buses
- Low output impedance to drive terminated transmission lines to 133Ω
- Switching response specified into 500Ω/50 pF
- Specified to interface with CMOS at $V_{OH} = V_{CC} - 2V$
- PNP inputs reduce input loading
- Switching specifications guaranteed over full temperature and V_{CC} range

Connection Diagram

Dual-In-Line Package



TL/F/6299–1

Order Number DM74AS245N
See NS Package Number N20A*

Function Table

Control Inputs		Operation
$\overline{G}$	DIR	
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	Hi-Z

*Contact your local NSC representative about surface mount (M) package availability.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V_{CC}	7V
Input Voltage	
Control Inputs	7V
I/O Ports	5.5V
Operating Free Air Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−15	mA
I_{OL}	Low Level Output Current			48	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics over recommended operating free air temperature range

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, I_{OH} = −3 mA		2.4	3.2		V
		V_{CC} = 4.5V, I_{OH} = −15 mA		2	2.3		
		I_{OH} = −2 mA, V_{CC} = 4.5V to 5.5V		V_{CC} − 2			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = Max			0.35	0.55	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IN} = 7V, (V_{IN} = 5.5V for A or B Ports)				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IN} = 2.7V	Control Inputs			20	μA
			A or B Ports			70	
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V	Control Inputs			−0.5	mA
			A or B Ports			−0.75	
I_O	Output Drive Current	V_{CC} = 5.5V, V_{OUT} = 2.25V		−50		−150	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Output High		62	97	mA
			Output Low		95	149	
			TRI-STATE		79	123	

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From	To	Min	Max	Units
t_{PLH}	Propagation Delay Time High-to-Low Level Output	V_{CC} = 4.5V to 5.5V, $R_1 = R_2$ = 500Ω, C_L = 50 pF	A or B	B or A	2	7.5	ns
t_{PHL}	Propagation Delay Time High-to-Low Level Output		A or B	B or A	2	7	ns
t_{PZL}	Output Enable Time to Low Level		$\overline{G}$	A or B	2	8.5	ns
t_{PZH}	Output Enable Time to High Level		$\overline{G}$	A or B	2	9	ns
t_{PLZ}	Output Disable Time from Low Level		$\overline{G}$	A or B	2	9.5	ns
t_{PHZ}	Output Disable Time from High Level		$\overline{G}$	A or B	2	5.5	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM74AS257/DM74AS258 TRI-STATE® Quad 1 of 2 Line Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four TRI-STATE outputs that can interface directly with data lines of bus-organized systems. A 4-bit word selected from one of two sources is routed to the four outputs. The AS257 presents true data whereas the AS258 presents inverted data to minimize propagation delay time.

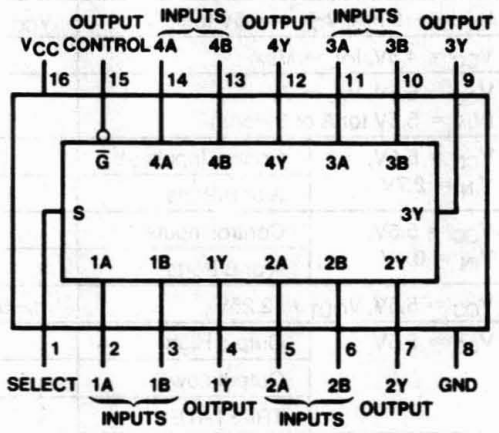
This TRI-STATE output feature means that n-bit (paralleled) data selectors with up to 300 sources can be implemented for data buses. It also permits the use of standard TTL registers for data retention throughout the system.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky, low power Schottky, and advanced low power Schottky TTL counterpart
- Improved AC performance over Schottky, low power Schottky, and advanced low power Schottky counterparts
- TRI-STATE buffer-type output drive bus lines directly
- Expand any data input point
- Multiplex dual data buses
- General four functions of two variables (one variable is common)
- Source programmable counters

Connection Diagram

Dual-In-Line Package



TL/F/6107–1

Order Number DM74AS257N or DM74AS258N
See NS Package Number N16A*

Function Table

Inputs				Output Y	
Output Control	Select	A	B	AS257	AS258
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = High Level, L = Low Level, X = Don't Care
Z = High Impedance (off)

*Contact your local NSC representative about surface mount (M) package availability.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V_{CC}	7V
Input Voltage	7V
Voltage Applied to Disabled Output	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−15	mA
I_{OL}	Low Level Output Current			48	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter		Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage		V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage		V_{CC} = 4.5V, I_{OH} = Max		2.4	3.2		V
			I_{OH} = −2 mA, V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage		V_{CC} = 4.5V, I_{OL} = Max			0.35	0.5	V
I_I	Input Current @ Max Input Voltage		V_{CC} = 5.5V, V_{IH} = 7V	A, B, $\overline{G}$			0.1	mA
				Select			0.2	
I_{IH}	High Level Input Current		V_{CC} = 5.5V, V_{IH} = 2.7V	A, B, $\overline{G}$			20	μA
				Select			40	
I_{IL}	Low Level Input Current		V_{CC} = 5.5V, V_{IL} = 0.4V	Select			−1	mA
				All Others			−0.5	
I_O	Output Drive Current		V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied		V_{CC} = 5.5V V_O = 2.7V				−50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied		V_{CC} = 5.5V V_O = 0.4V				−50	μA
I_{CCH}	Supply Current	AS257	V_{CC} = 5.5V Outputs Open	Outputs High		12.9	19.7	mA
		AS258				8.8	13.5	mA
I_{CCL}	Supply Current	AS257		Outputs Low		19	30.6	mA
		AS258				15.8	24.6	mA
I_{CCZ}	Supply Current	AS257		Outputs Disabled		19.7	31.9	mA
		AS258				15.5	25.2	mA

3

'AS257 Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	From	To	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time, Low to High Level Output	Data	Any Y	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R_L = 500Ω	1	5.5	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output				1	6	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	Select	Any Y		2	11	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output				2	10	ns
t_{PZH}	Output Enable Time to High Level	Output Control	Any Y		2	7.5	ns
t_{PZL}	Output Enable Time to Low Level				2	9.5	ns
t_{PHZ}	Output Disable Time, from High Level	Output Control	Any Y		1.5	6.5	ns
t_{PLZ}	Output Disable Time, from Low Level				2	7	ns

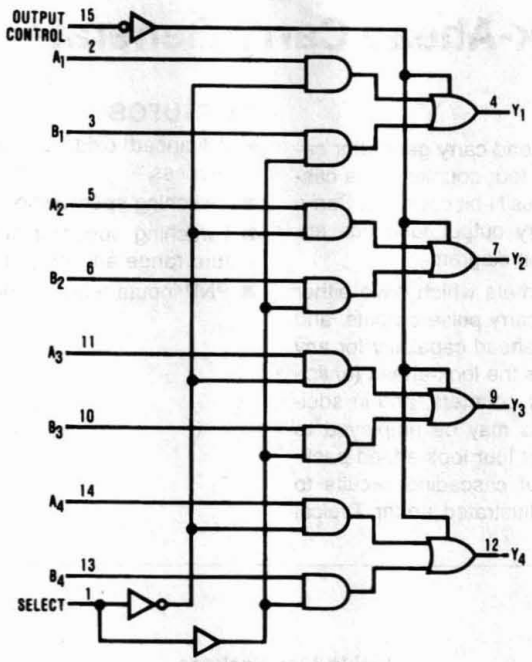
'AS258 Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	From	To	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time, Low to High Level Output	Data	Any Y	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R_L = 500Ω	1	5	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output				1	4	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	Select	Any Y		2	9.5	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output				2	10	ns
t_{PZH}	Output Enable Time to High Level	Output Control	Any Y		2	8	ns
t_{PZL}	Output Enable Time to Low Level				2	10	ns
t_{PHZ}	Output Disable Time, from High Level	Output Control	Any Y		1.5	6	ns
t_{PLZ}	Output Disable Time, from Low Level				2	6.5	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagrams

74AS257



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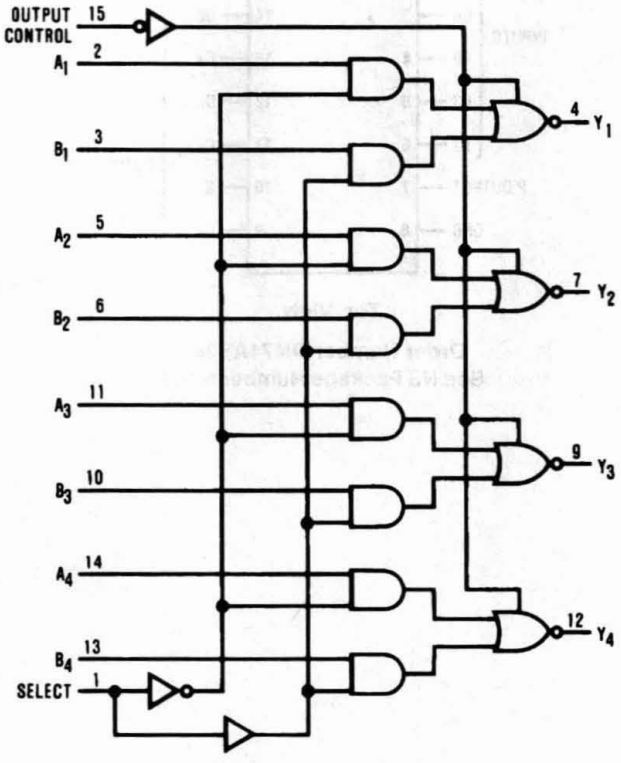
74AS258



TL/F/6107–3

3

National Semiconductor Corporation

DM74AS264 Look-Ahead Carry Generator

General Description

This circuit is a high speed, look-ahead carry generator capable of anticipating a carry across four counters. It is cascadable to perform look-ahead across N-bit counters. Carry, generator-carry and propagate-carry output functions are provided as shown in the connection diagram.

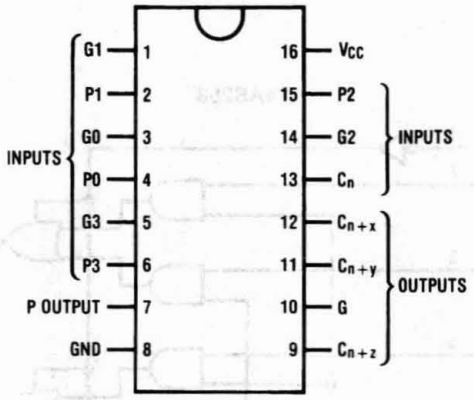
This circuit can accommodate counters which have either low level carry pulse or high level carry pulse outputs, and can provide high speed carry look-ahead capability for any word length. Each AS264 generates the look-ahead (anticipated carry) across a group of four counters, and in addition, other carry look-ahead circuits may be employed to anticipate a carry across sections of four look-ahead packages up to N bits. This method of cascading circuits to perform multi-level look-ahead is illustrated under Typical Applications.

Features

- Advanced oxide-isolated, ion implanted Schottky TTL process
- Switching specification at 50 pF
- Switching specifications guaranteed over full temperature range and V_{CC} range
- PNP inputs reduce input loading

Connection Diagram

Dual-In-Line Package



TL/F/6302–1

Top View

Order Number DM74AS264N
See NS Package Number N16A*

*Contact your local NSC representative about surface mount (M) package availability.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V_{CC}	7V
Input Voltage	7V
Operating Free Air Temperature	0°C to 70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−2	mA
I_{OL}	Low Level Output Current			20	mA
T_A	Operating Free-Air Temperature	0		70	°C

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise specified)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V, I_{OH} = −2 mA		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 20 mA			0.3	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_I = 7V	C_n			500	μA
			G0, G2			700	
			G1			800	
			G3, P0, P1			400	
			P2			300	
			P3			200	
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_I = 2.7V	C_n			100	μA
			G0, G2			140	
			G1			160	
			G3, P0, P1			80	
			P2			60	
			P3			40	
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_I = 0.4V	C_n			−2.5	mA
			G0, G2			−3.5	
			G1			−4	
			G3, P0, P1			−2	
			P3			−1	
			P2			−1.5	
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = 5.5V			26	38	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = 5.5V			28	43	mA

Note 1: All typicals are at V_{CC} = 5V and T_A = 25°C.

Switching Characteristics over recommended supply and temperature range (Note 1)

Symbol	Parameter	From (Input)	To (Output)	Conditions	Min	Max	25°C 5V Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	P or G	C_{n+x}, C_{n+y}, or C_{n+z}	C_L = 50 pF, R_L = 500Ω, V_{CC} = 4.5V to 5.5V	2	8	7.5	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	7	7	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	P or G	G		3	9.5	9	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				3	8.5	8	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	P	P		2	7.5	7	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	6.5	6	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_n	C_{n+x}, C_{n+y}, or C_{n+z}		3	9	8.5	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	8	7.5	ns

Note 1: See Section 1 for test waveforms and output load.

Function Tables

Logic Equations for the 'AS264 are:

Active High Carry Counters (C_n = H)

$$C_{n+x} = \overline{G0}$$
$$C_{n+y} = \overline{G0} \bullet \overline{G1}$$
$$C_{n+z} = \overline{G0} \bullet \overline{G1} \bullet \overline{G2}$$
$$\overline{G} = \overline{G0} \bullet \overline{G1} \bullet \overline{G2} \bullet \overline{G3}$$
$$\overline{P} = 0$$

Active Low Carry Counters (C_n = L)

$$C_{n+x} = \overline{P0}$$
$$C_{n+y} = \overline{P0} \bullet \overline{P1}$$
$$C_{n+z} = \overline{P0} \bullet \overline{P1} \bullet \overline{P2}$$
$$\overline{P} = \overline{P0} + \overline{P1} + \overline{P2} + \overline{P3}$$
$$G = \overline{P1}\,\overline{G3}\,\overline{G2}\,\overline{G1} + \overline{P2}\,\overline{G3}\,\overline{G2}\,\overline{G1} + \overline{P3}\,\overline{G3}$$

Inputs								Output
G3	G2	G1	G0	P3	P2	P1	P0	G
L	X	X	X	X	X	X	X	L
X	L	X	X	L	X	X	X	L
X	X	L	X	L	L	X	X	L
X	X	X	L	L	L	L	X	L
X	X	X	X	L	L	L	L	L
All Other Combinations								H

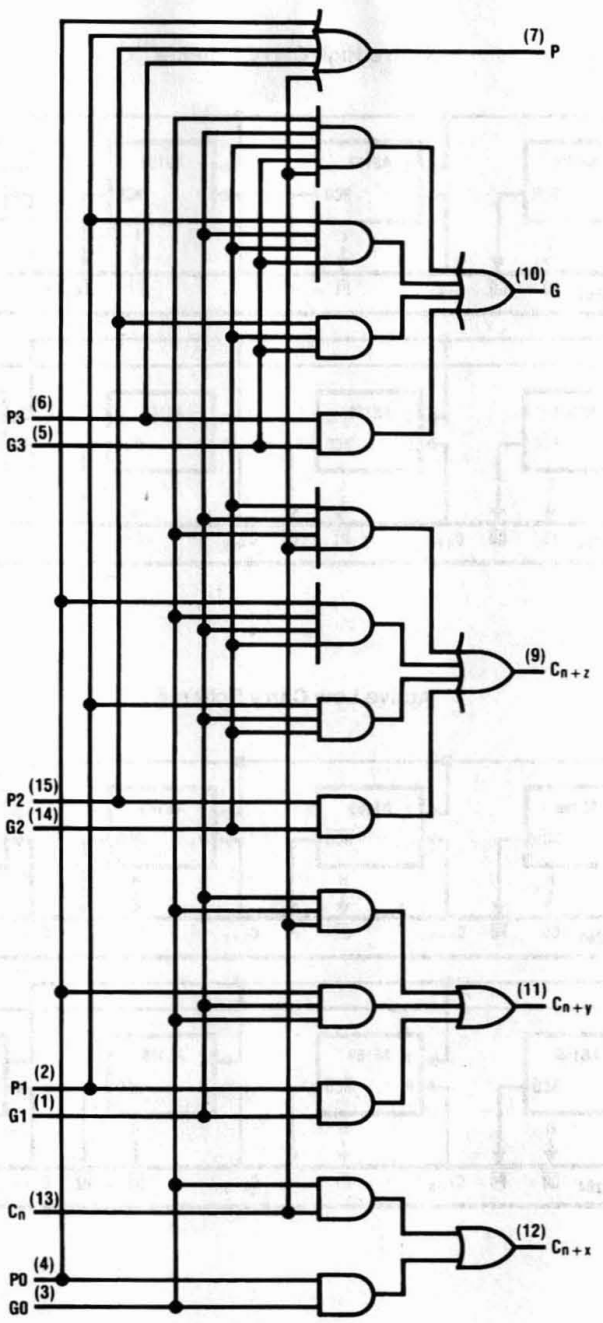
Inputs					Output
P3	P2	P1	P0	C_n	P
L	L	L	L	L	L
All Other Combinations					H

Inputs			Output
G1	G0	C_n	C_{n+y}
H	X	X	H
H	H	X	H
X	X	H	H
All Other Combinations			L

Inputs			Output
G0	P0	C_n	C_{n+x}
H	H	X	H
H	X	H	H
All Other Combinations			L

Inputs							Output
G2	G1	G0	P2	P1	P0	C_n	C_{n+z}
H	X	X	H	X	X	X	H
H	H	X	X	H	X	X	H
H	H	H	X	X	H	X	H
H	H	H	X	X	X	H	H
All Other Combinations							L

Logic Diagram



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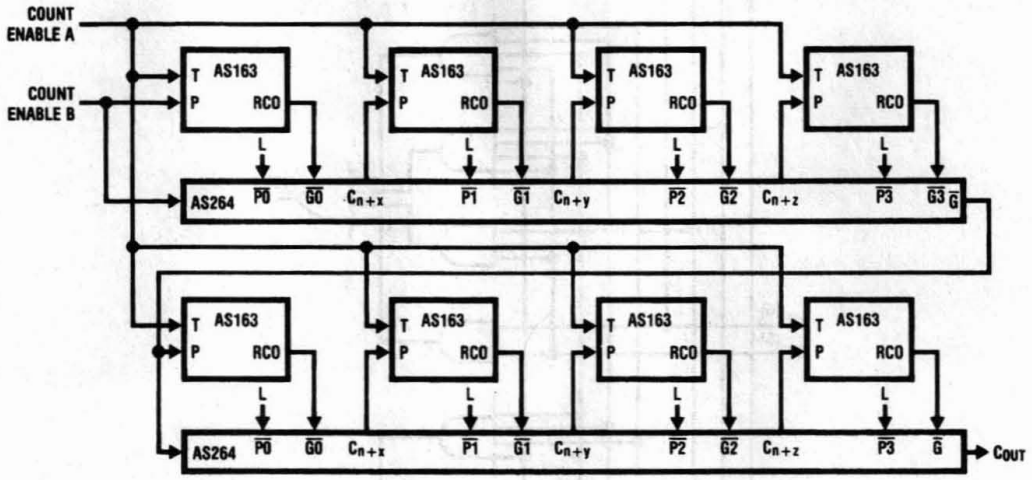
V_{CC} = pin 16
GND = pin 8

Typical Applications

Active High Carry Scheme



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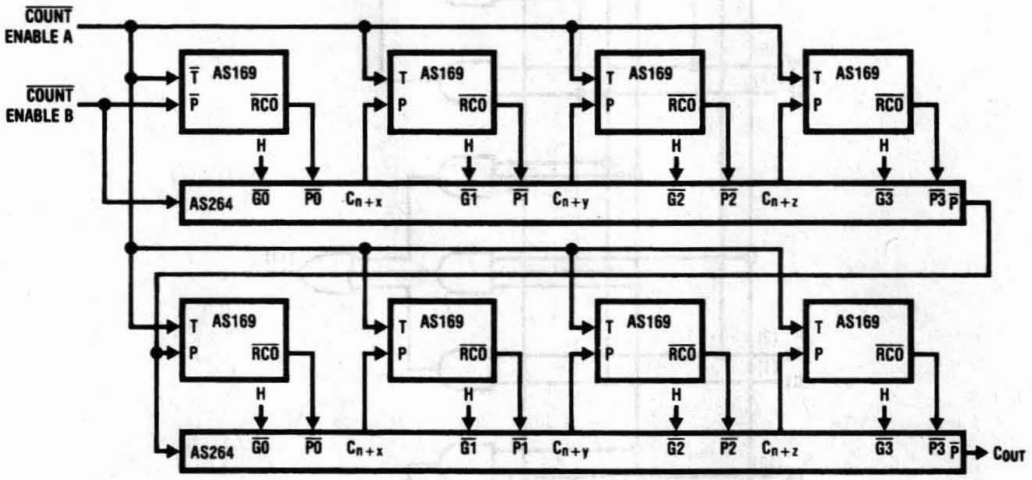
Active Low Carry Scheme



TL/F/6302–4

National Semiconductor Corporation

DM74AS280 9-Bit Parity Generator/Checker

General Description

These universal, 9-bit parity generators/checkers utilize advanced Schottky high performance circuitry and feature odd/even outputs to facilitate operation of either odd or even parity applications. The word length capability is easily expanded by cascading.

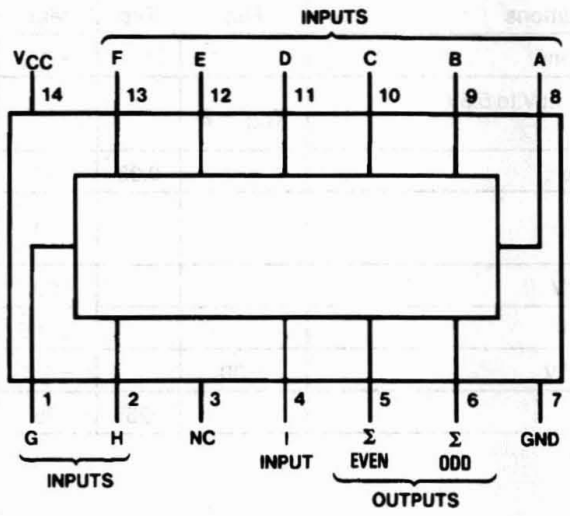
The AS280 can be used to upgrade the performance of most systems utilizing the '180 parity generator/checker. Although the AS280 is implemented without expander inputs, the corresponding function is provided by the availability of an input at pin 4 and no internal connection at pin 3. This permits the AS280 to be substituted for the '180 in existing designs to produce identical function even if 'AS280s are mixed with existing '180s.

Features

- Generates either odd or even parity for nine data lines
- Inputs are buffered to lower the drive requirements
- Can be used to upgrade existing systems using MSI parity circuits
- Cascadable for N-bits
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range

Connection Diagram

Dual-In-Line Package



TL/F/6303–1

Order Number DM74AS280M
or DM74AS280N
See NS Package Number M14A or N14A

Function Table

Number of Inputs (A thru I) that are High	Outputs	
	ΣEven	ΣOdd
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

L = Low State
H = High State

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−2	mA
I_{OL}	Low Level Output Current			20	mA
T_A	Free-Air Operating Temperature	0		70	°C

Electrical Characteristics

Over recommended free-air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

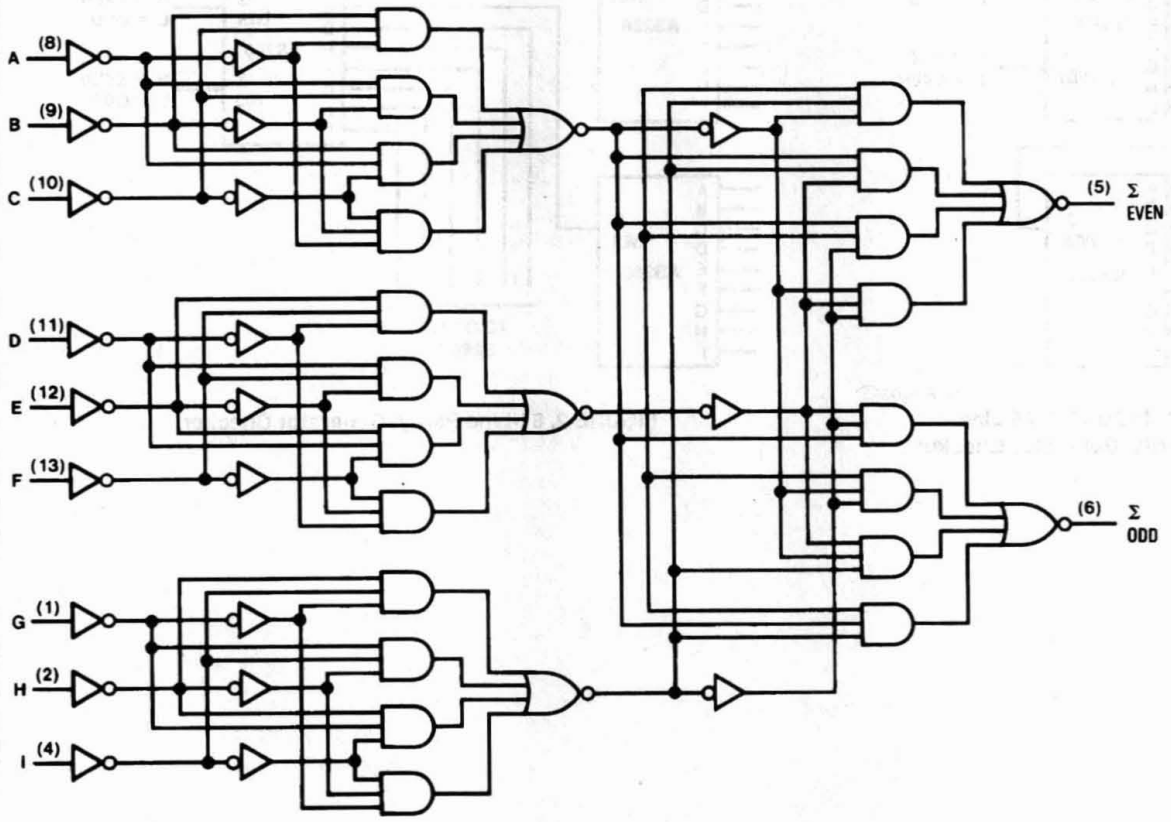
Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA			−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2 mA, V_{CC} = 4.5V to 5.5V	V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = Max		0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V			−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V	−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V		25	35	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From	To	Min	Max	Units
t_{PLH}	Propagation Delay Time, Low to High Level Output	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R_L = 500Ω	Data	ΣEven	3	12	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output				3	11	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output		Data	ΣOdd	3	12	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output				3	11.5	ns

Note 1: See section 1 for test waveforms and output load.

Logic Diagram



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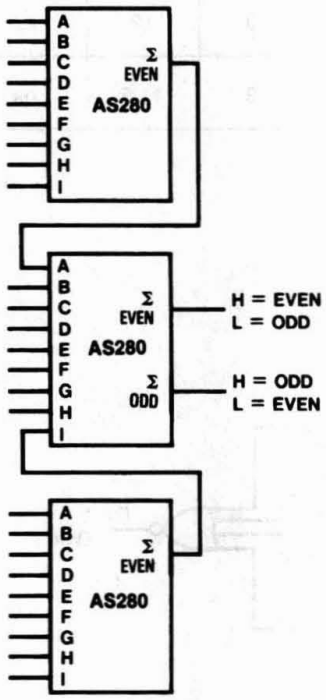
Typical Applications

Three AS280s can be used to implement a 25-line parity generator/checker.

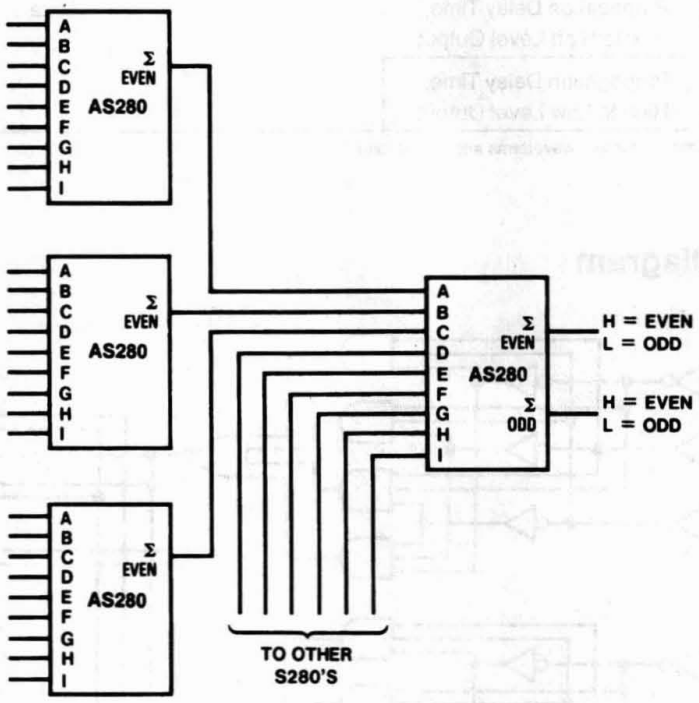
As an alternative, the outputs of two or three parity generators/checkers can be decoded with a 2-input (AS86) or 3-input (S135) exclusive-OR gate for 18 or 27-line parity applications.

Longer word lengths can be implemented by cascading AS280s. As shown in *Figure 2*, parity can be generated for word lengths up to 81 bits.



TL/F/6303–3

FIGURE 1. 25-Line Parity/Generator Checker



TL/F/6303–4

FIGURE 2. 81-Line Parity/Generator Checker

National Semiconductor Corporation

DM74AS282 Look-Ahead Carry Generator with Selectable Carry Inputs

General Description

This circuit is a high-speed, look-ahead carry generator capable of anticipating a carry across four binary adders or groups of adders. It is cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided.

When used in conjunction with the 'AS881 arithmetic logic unit, this generator provides high-speed carry look-ahead capability for any word length. Each 'AS282 generates the look-ahead (anticipated carry) across a group of four ALUs and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n bits. The method of cascading circuits to perform multi-level look-ahead is illustrated under Typical Applications.

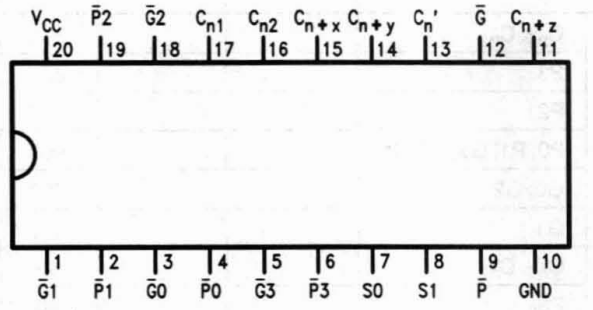
The carry functions (inputs, outputs, generate and propagate) of the look-ahead generator are implemented in compatible forms for direct connection to the 'AS881 ALU. The carry inputs are selectable in either active high or active low.

Features

- Selectable input version of 'AS182 allows double precision carry
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Switching specification at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- PNP inputs reduce input loading

Connection Diagram

Dual-In-Line Package



TL/F/6304–1

Top View

Order Number DM74AS282N
See NS Package Number N20A*

Logic Equations

$$C_{n+x} = G0 + P0\,C_n$$
$$C_{n+y} = G1 + P1\,G0 + P1\,P0\,C_n$$
$$C_{n+z} = G2 + P2\,G1 + P2\,P1\,G0 + P2\,P1\,P0\,C_n$$
$$\overline{G} = \overline{G3 + P3\,G2 + P3\,P2\,G1 + P3\,P2\,P1\,G0}$$
$$\overline{P} = \overline{P3\,P2\,P1\,P0}$$

Pin Designations

Designations	Function
$\overline{G}0, \overline{G}1, \overline{G}2, \overline{G}3$	Carry Generate Inputs
$\overline{P}0, \overline{P}1, \overline{P}2, \overline{P}3$	Carry Propagate Inputs
C_{nA}, C_{nB}	Carry Inputs
C_n'	Selected Carry
$C_{n+x}, C_{n+y}, C_{n+z}$	Carry Outputs
$\overline{G}$	Carry Generate Outputs
$\overline{P}$	Carry Propagate Outputs
S0, S1	Carry Select Inputs
V_{CC}	Supply Voltage
GND	Ground

*Contact your local NSC representative about surface mount (M) package availability.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V_{CC}	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−2	mA
I_{OL}	Low Level Output Current			20	mA
T_A	Operating Free-Air Temperature	0		70	°C

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise specified)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V, I_{OH} = −2 mA		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 20 mA			0.3	0.5	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = 5.5V, V_I = 7V	C_{n1}, C_{n2}			200	μA
			P3			200	
			P2			300	
			P0, P1, G3, S0, S1			400	
			G0, G2			700	
			G1			800	
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_I = 2.7V	C_{n1}, C_{n2}			40	μA
			P3			40	
			P2			60	
			P0, P1, G3, S0, S1			80	
			G0, G2			140	
			G1			160	
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_I = 0.4V	C_{n1}, C_{n2}			−1	mA
			P3			−1	
			P2			−1.5	
			P0, P1, G3, S0, S1			−2	
			G0, G2			−3.5	
			G1			−4	

Electrical Characteristics (Continued)

over recommended operating free-air temperature range (unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
I_O (Note 2)	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V	−30		−112	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = 5.5V		22	35	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = 5.5V		26	49	mA

Note 1: All typical values are at V_{CC} = 5V, T_A = 25°C.

Note 2: The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current I_{OS}.

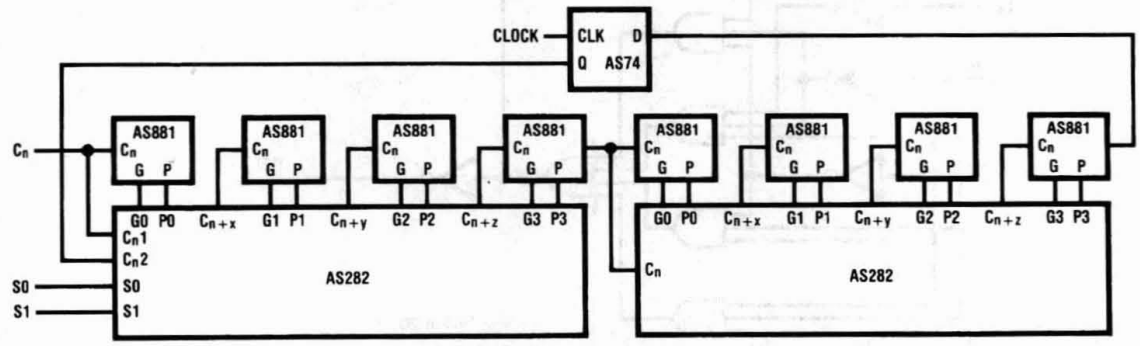
Switching Characteristics over recommended supply and temperature range (Note 3)

Symbol	Parameter	From (Input)	To (Output)	Conditions	Min	Max	25°C 5.0V Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	$\overline{P}$ or $\overline{G}$	$C_n + x$, $C_n + y$, or $C_n + z$	C_L = 50 pF, R_L = 500Ω V_{CC} = 4.5V to 5.5V	3	11	10	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	7	6.5	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	$\overline{P}$ or $\overline{G}$	$\overline{G}$		2	11	10	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	8	7	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	$\overline{P}$	$\overline{P}$		2	8	7	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	6	5.5	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_{n1} C_{n2}, S1, S0	$C_n + x$, $C_n + y$, or $C_n + z$		3	14	13	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				3	12	11	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_{n1}, C_{n2}, S1, S0	C_n'		3	12	11	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				3	11	10	ns

Note 3: See Section 1 for test waveforms and output load.

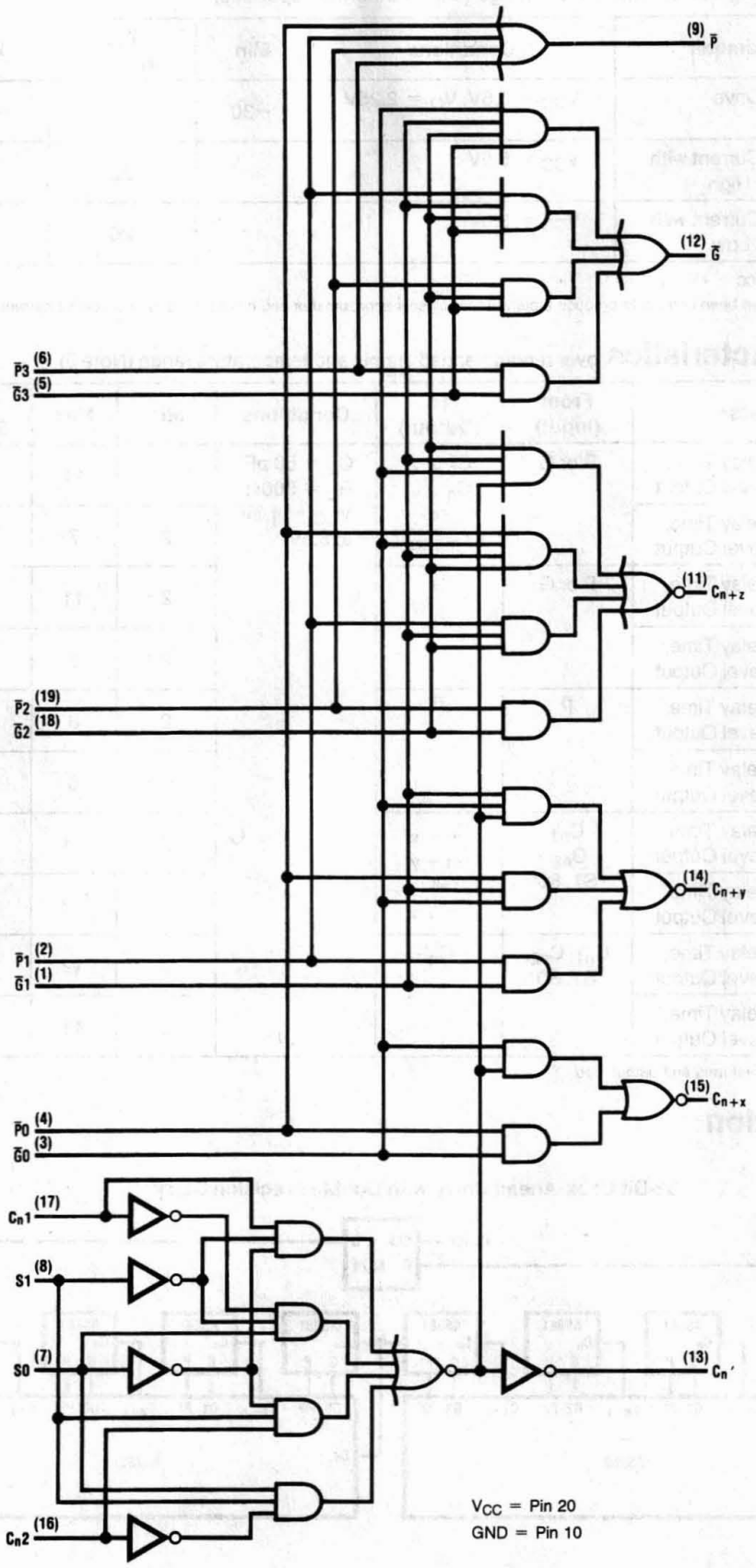
Typical Application

32-Bit Look-Ahead Carry with Double Precision Carry



TL/F/6304–2

Logic Diagram



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Function Tables

Function Table for $\overline{G}$ Output

Inputs							Output
$\overline{G}3$	$\overline{G}2$	$\overline{G}1$	$\overline{G}0$	$\overline{P}3$	$\overline{P}2$	$\overline{P}1$	$\overline{G}$
L	X	X	X	X	X	X	L
X	L	X	X	L	X	X	L
X	X	L	X	L	L	X	L
X	X	X	L	L	L	L	L
All Other Combinations							H

Function Table for $\overline{P}$ Output

Inputs				Output
$\overline{P}3$	$\overline{P}2$	$\overline{P}1$	$\overline{P}0$	$\overline{P}$
L	L	L	L	L
All Other Combinations				H

Function Table for C_n' Output

Inputs		Output
S1	S0	C_n'
L	L	C_{nA}
L	H	$\overline{C}_{nA}$
H	L	C_{nB}
H	H	$\overline{C}_{nB}$

H = High Level, L = Low Level, X = Irrelevant

Any inputs not shown in a given table are irrelevant with respect to that output.

Function Table for C_{n+x} Output

Inputs			Output
$\overline{G}0$	$\overline{P}0$	Cn′	C_{n+x}
L	X	X	H
X	L	H	H
All Other Combinations			L

Function Table C_{n+y} Output

Inputs					Output
$\overline{G}1$	$\overline{G}0$	$\overline{P}1$	$\overline{P}0$	$C_{n'}$	C_{n+y}
L	X	X	X	X	H
X	L	L	X	X	H
X	X	L	L	H	H
All Other Combinations					L

Function Table for C_{n+z} Output

Inputs							Output
$\overline{G}2$	$\overline{G}1$	$\overline{G}0$	$\overline{P}2$	$\overline{P}1$	$\overline{P}0$	$C_{n'}$	C_{n+z}
L	X	X	X	X	X	X	H
X	L	X	L	X	X	X	H
X	X	L	L	L	X	X	H
X	X	X	L	L	L	H	H
All Other Combinations							L

National Semiconductor Corporation

DM74AS286 9-Bit Parity Generator/Checker with Bus-Driver Parity I/O Port

General Description

These universal, 9-bit parity generators/checkers utilize advanced Schottky high performance circuitry and feature odd/even outputs to facilitate operation of either odd or even parity applications. The word length capability is easily expanded by cascading.

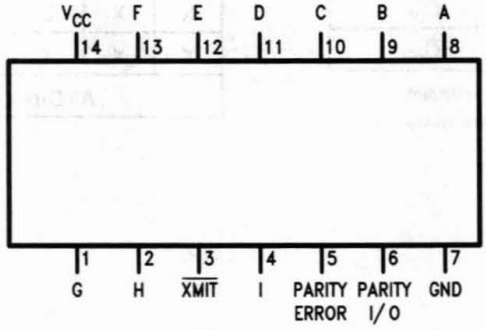
The 'AS286 can be used to upgrade the performance of most systems utilizing the 'AS180, 'AS280 parity generator/checker. Although the 'AS286 is implemented without expander inputs, the corresponding function is provided by the availability of an input pin $\overline{XMIT}$. $\overline{XMIT}$ is a control line which makes parity error output active and parity an input port when "high"; when "low", parity error output is inactive and parity becomes an output port. In addition, parity I/O control circuitry contains a feature to keep the I/O port in the TRI-STATE® during power up or down to prevent bus glitches.

Features

- PNP inputs to reduce bus loading
- Generates either odd or even parity for nine data lines
- Inputs are buffered to lower the drive requirements
- Can be used to upgrade existing systems using MSI parity circuits
- Cascadable for n-bits
- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- A parity I/O portable to drive bus

Connection Diagram

Dual-In-Line Package



TL/F/6305–1

Top View

Order Number DM74AS286N
See NS Package Number N14A*

Function Table

Number of Inputs (A thru I) that are High	Parity I/O		$\overline{XMIT}$	Parity Error	Mode of Operation
	Input	Output			
0, 2, 4, 6, 8	N/A	H	L	H	Parity Generator
1, 3, 5, 7, 9	N/A	L	L	H	
0, 2, 4, 6, 8	H	N/A	H	H	Parity Checker
0, 2, 4, 6, 8	L	N/A	H	L	
1, 3, 5, 7, 9	H	N/A	H	L	Parity Checker
1, 3, 5, 7, 9	L	N/A	H	H	

L = Low Logic Level
H = High Logic Level
N/A = Not Applicable

*Contact your local NSC representative about surface mount (M) package availability.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		Min	Typ	Max	Units
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current	Parity I/O			−15	mA
		Parity Error			−2	mA
I_{OL}	Low Level Output Current	Parity I/O			48	mA
		Parity Error			20	mA
T_A	Operating Free-Air Temperature		0		70	°C

Electrical Characteristics

over recommended free-air temperature range (Note 1). All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = Max, V_{CC} = 4.5V		2.4	3.2		V
		V_{CC} = 4.5V to 5.5V, I_{OH} = −2 mA		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = Max			0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V (V_I = 5.5V for Parity I/O)				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V (Note 1)	Others			20	μA
			Parity I/O			50	
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V (Note 1)				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_{OUT} = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V, Transmit Mode $\overline{XMIT}$ = Low				43	mA
		Receive Mode $\overline{XMIT}$ = High				50	mA

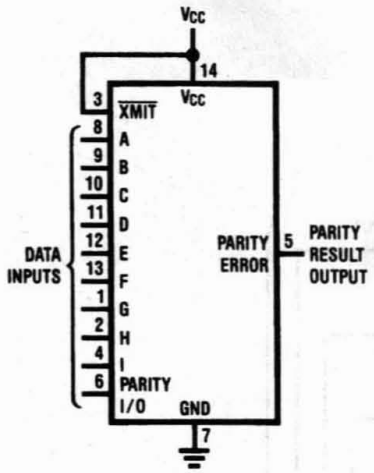
Note 1: For I/O ports, the parameters I_{IH} and I_{IL} include the off-state current, I_{OZH} and I_{OZL}.

Switching Characteristics over recommended supply and temperature range (Note 1)

Symbol	Parameter	From	To	Min	Max	Units
t_{PLH}	Propagation Delay Time from Low to High Level Output	Any Data Input	Parity I/O	3	15	ns
t_{PHL}	Propagation Delay Time from High to Low Level Output	Any Data Input	Parity I/O	3	14	ns
t_{PLH}	Propagation Delay Time from Low to High Level Output	Any Data Input	Parity Error	3	16.5	ns
t_{PHL}	Propagation Delay Time from High to Low Level Output	Any Data Input	Parity Error	3	16.5	ns
t_{PLH}	Propagation Delay Time from Low to High Level Output	Parity I/O	Parity Error	3	9	ns
t_{PHL}	Propagation Delay Time from High to Low Level Output	Parity I/O	Parity Error	3	9	ns
t_{PZL}	Output Enable Time to Low Level	$\overline{XMIT}$	Parity I/O	3	16	ns
t_{PLZ}	Output Disable Time from Low Level	$\overline{XMIT}$	Parity I/O	3	10	ns
t_{PZH}	Output Disable Time from High Level	$\overline{XMIT}$	Parity I/O	3	13	ns
t_{PHZ}	Output Enable Time to High Level	$\overline{XMIT}$	Parity I/O	3	11.5	ns

Note 1: See Section 1 for test waveforms and output load.

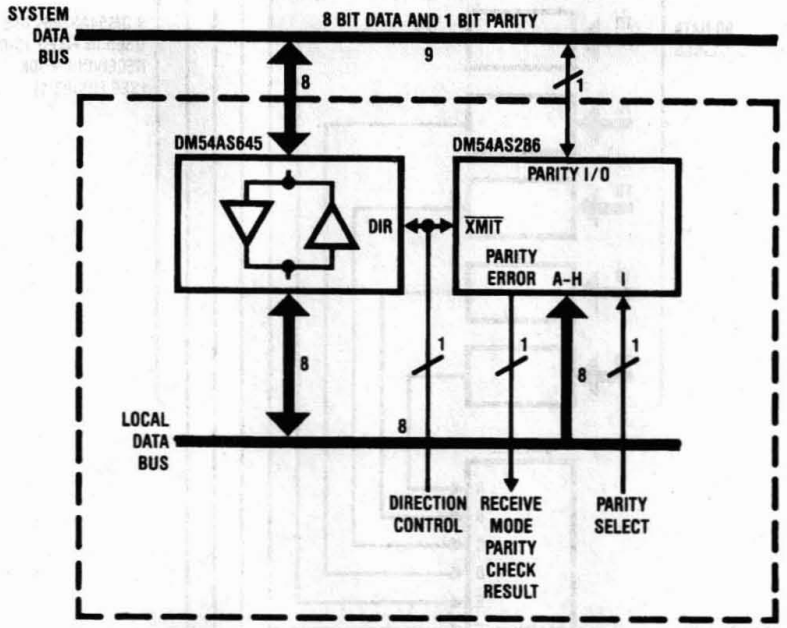
Typical Applications



TL/F/6305–2

Number of Inputs that are Logic "1"		Parity Result Output
0, 2, 4, 6, 8, 10	Even	L
1, 3, 5, 7, 9	Odd	H

FIGURE 1. Dedicated 10-Bit Parity Sensing Configuration



TL/F/6305–3

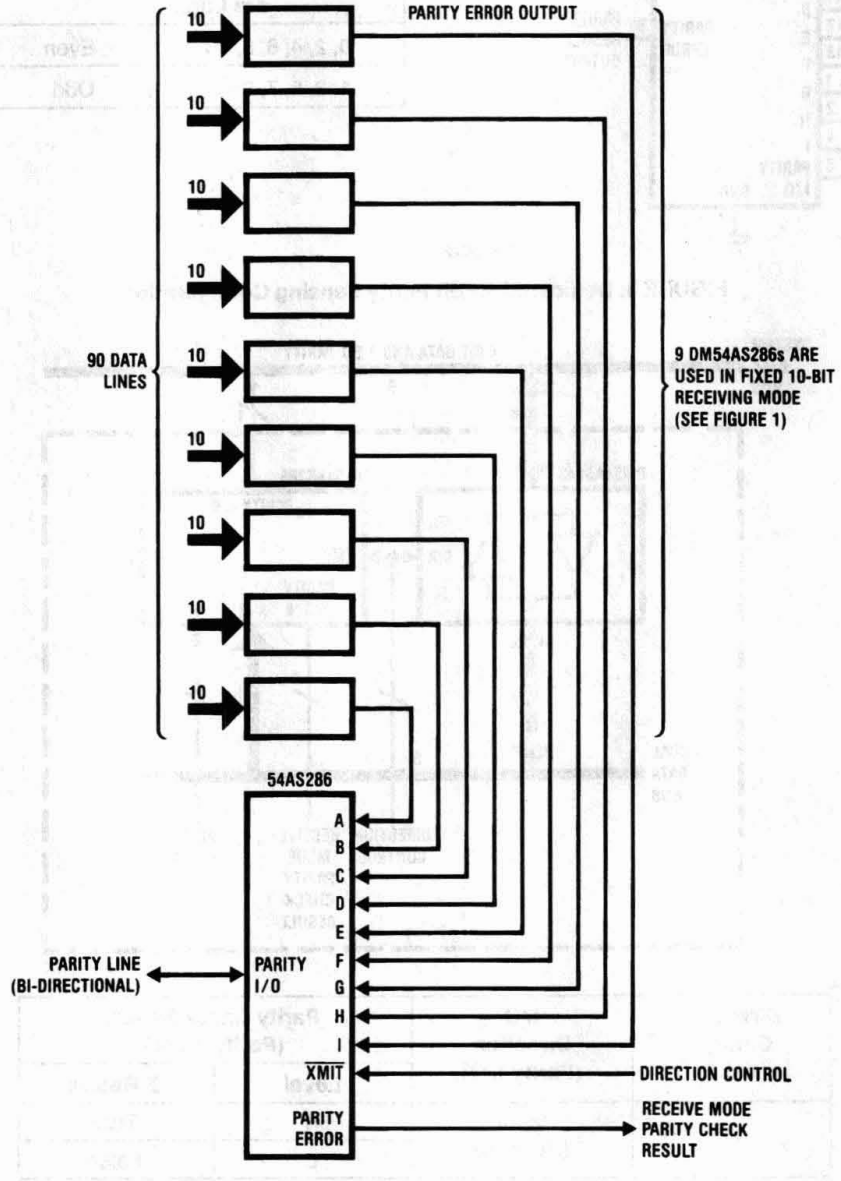
Direction Control (XMIT)	I/O Direction (Parity I/O)	Parity Check Result (Parity Error)	
		Level	Σ Result
H	Input (Receive)	H	True
		L	False
L	Output (Transmit)	H	N/A

L = Low Logic Level
H = High Logic Level
N/A = Not Applicable

Parity Select (Input I)	
Level	Format
H	Even
L	Odd

FIGURE 2. Bus I/O Parity Implementation

Typical Applications (Continued)



Note: Parity format in this configuration is "odd parity"

FIGURE 3. 90-Bit Parity Generator/Checker Implementation Using Device Expansion Techniques

National Semiconductor Corporation

DM74AS373 Octal D-Type Transparent Latches with TRI-STATE® Outputs

General Description

These 8-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the AS373 are transparent D-type latches, meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was set up.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

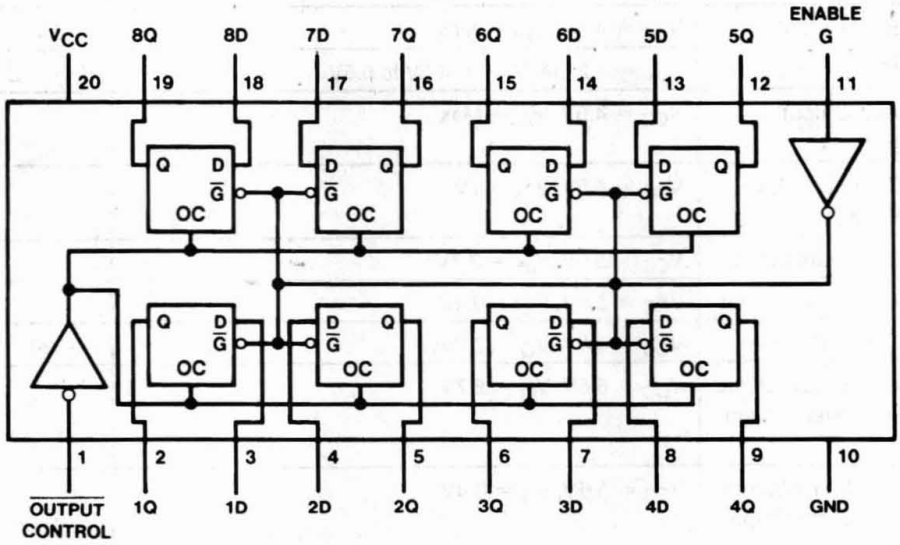
The output control does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with LS and ALS TTL counterparts
- Improved AC performance over LS and ALS TTL counterparts
- TRI-STATE buffer-type outputs drive bus lines directly

Connection Diagram

Dual-In-Line Package



TL/F/6309–1

Order Number DM74AS373WM or DM74AS373N
See NS Package Number M20B or N20A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Voltage Applied to Disabled Output	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−15	mA
I_{OL}	Low Level Output Current			48	mA
t_W	Width of Enable Pulse, High	4.5			ns
t_{SU}	Data Setup Time	2↓			ns
t_H	Data Hold Time	3↓			ns
T_A	Free Air Operating Temperature	0		70	°C

The (↓) arrow indicates the negative edge of the enable is used for reference.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

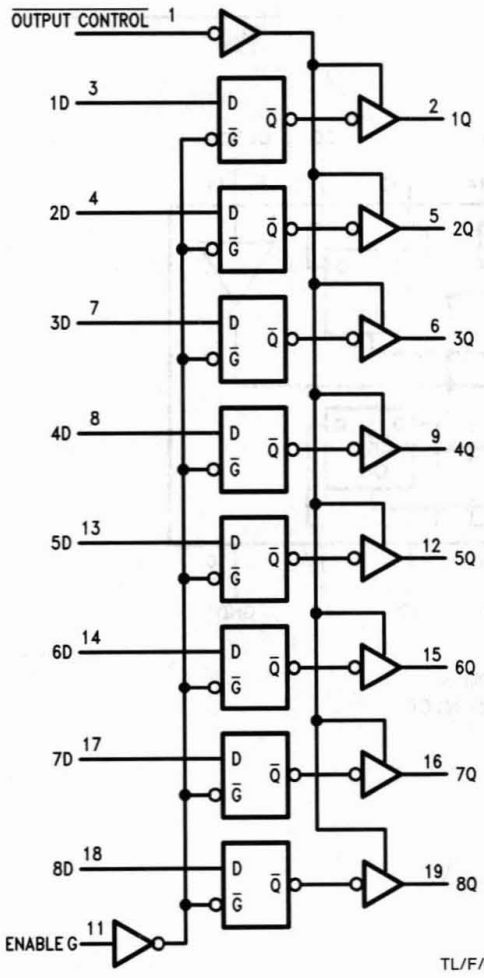
Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, I_{OH} = Max		2.4	3.2		V
		I_{OH} = −2 mA, V_{CC} = 4.5V to 5.5V		V_{CC} − 2			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = Max			0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{OZH}	Off-State Output Current with High Level Voltage Applied	V_{CC} = 5.5V, V_O = 2.7V				50	μA
I_{OZL}	Off-State Output Current with Low Level Voltage Applied	V_{CC} = 5.5V, V_O = 0.4V				−50	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		55	90	mA
			Outputs Low		55	85	
			Outputs Disabled		65	100	

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From	To	DM74AS373		Units
					Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	Data	Any Q	3.5	6	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Data	Any Q	3.5	6	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		Enable	Any Q	6.5	11.5	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Enable	Any Q	5	7.5	ns
t_{PZH}	Output Enable Time to High Level Output		Output Control	Any Q	2	6.5	ns
t_{PZL}	Output Enable Time to Low Level Output		Output Control	Any Q	4.5	9.5	ns
t_{PHZ}	Output Disable Time from High Level Output		Output Control	Any Q	3	6.5	ns
t_{PLZ}	Output Disable Time from Low Level Output		Output Control	Any Q	3	7	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6309–2

Function Table

$\overline{\text{Output Control}}$	Enable G	D	Output Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

L = Low State, H = High State, X = Don't Care

Z = High Impedance State, Q_0 = Previous Condition of Q

National Semiconductor Corporation

DM74AS374 Octal D-Type Edge-Triggered Flip-Flops with TRI-STATE® Outputs

General Description

These 8-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the AS374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

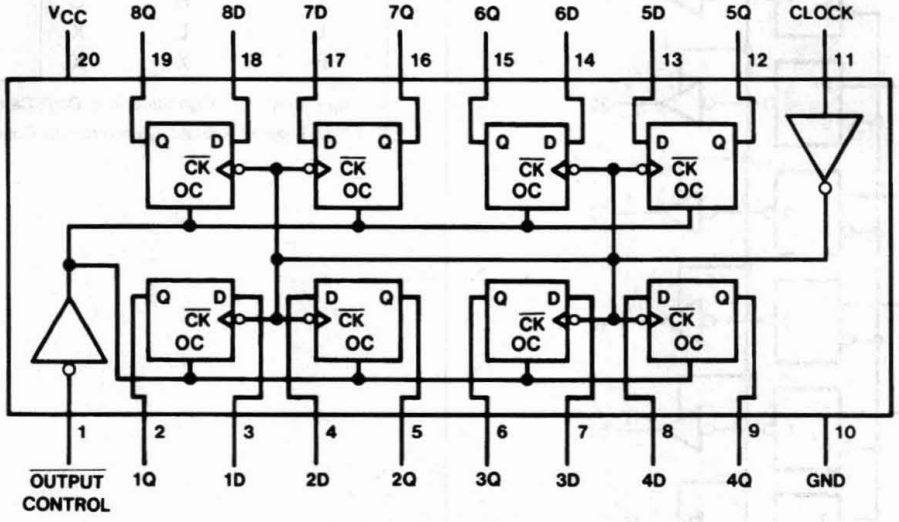
The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin-for-pin compatible with LS and ALS TTL counterparts
- Improved AC performance over LS and ALS TTL counterparts
- TRI-STATE buffer-type outputs drive bus lines directly

Connection Diagram

Dual-In-Line Package



TL/F/6310–1

Order Number DM74AS374WM, N
See NS Package Number M20B or N20A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Voltage Applied to Disabled Output	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−15	mA
I_{OL}	Low Level Output Current				48	mA
f_{CLK}	Clock Frequency		0		125	MHz
t_W	Width of Clock Pulse	High	4			ns
		Low	3			
t_{SU}	Data Setup Time		2↑	0		ns
t_H	Data Hold Time		3↑	0		ns
T_A	Operating Free Air Temperature		0		70	°C

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, I_{OH} = Max		2.4	3.2		V
		I_{OH} = −2 mA, V_{CC} = 4.5V to 5.5V		V_{CC} − 2			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = Max			0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = 5.5V, V_O = 2.7V				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V, V_O = 0.4V				−50	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		77	120	mA
			Outputs Low		84	128	
			Outputs Disabled		84	128	

3

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From	To	Min	Max	Units
f_{MAX}	Maximum Clock Frequency	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF			125		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output		Clock	Any Q	3	8	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Clock	Any Q	4	9	ns
t_{PZH}	Output Enable Time to High Level Output		Output Control	Any Q	2	6	ns
t_{PZL}	Output Enable Time to Low Level Output		Output Control	Any Q	3	10	ns
t_{PHZ}	Output Disable Time from High Level Output		Output Control	Any Q	2	6	ns
t_{PLZ}	Output Disable Time from Low Level Output		Output Control	Any Q	2	6	ns

Note 1: See Section 1 for test waveforms and output load.

Function Table

$\overline{\text{Output Control}}$	Clock	D	Output Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

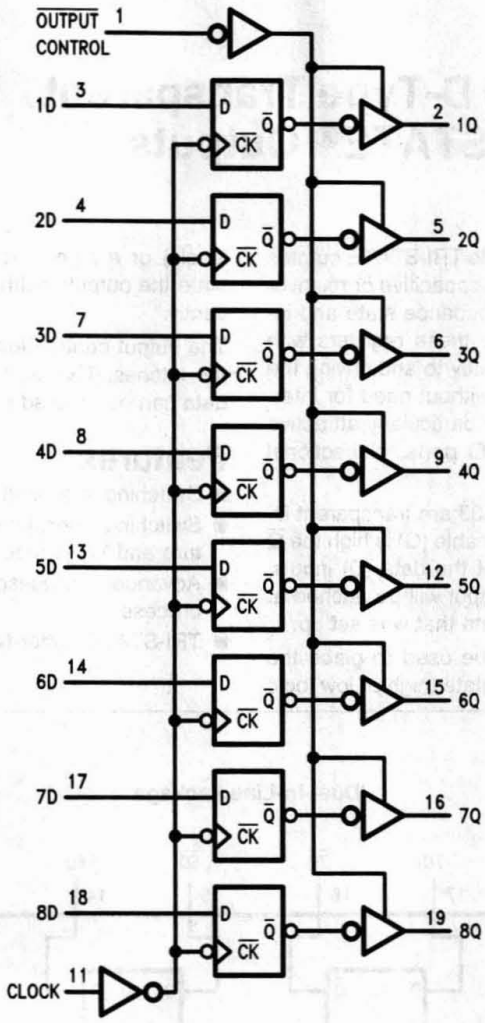
L = Low State, H = High State, X = Don't Care

↑ = Positive Edge Transition

Z = High Impedance State

Q_0 = Previous Condition of Q

Logic Diagram



TL/F/6310–2

National Semiconductor Corporation

DM74AS533 Octal D-Type Transparent Latches with TRI-STATE® Outputs

General Description

These 8-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight inverting latches of the AS533 are transparent D-type latches, meaning that while the enable (G) is high the $\overline{Q}$ outputs will follow the complement of the data (D) inputs. When the enable is taken low the output will be latched at the complement of the level of the data that was set up.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

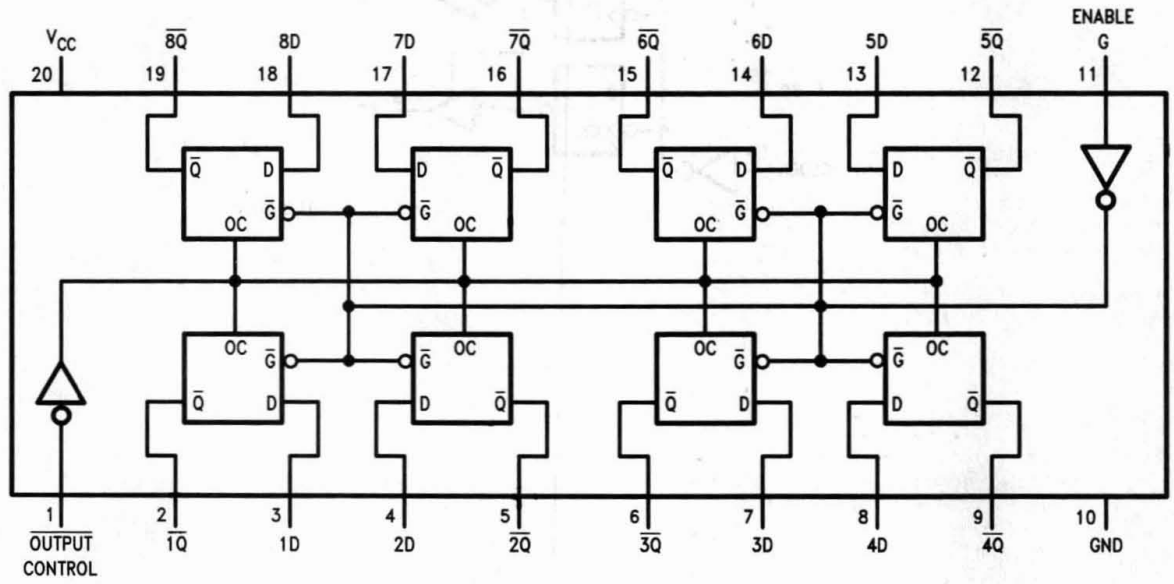
The output control does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- TRI-STATE buffer-type outputs drive bus lines directly

Connection Diagram

Dual-In-Line Package



TL/F/6311–1

Order Number DM74AS533N
See NS Package Number N20A*

*Contact your local NSC representative about surface mount (M) package availability.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Voltage Applied to Disabled Output	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−15	mA
I_{OL}	Low Level Output Current			48	mA
t_W	Width of Enable Pulse, High or Low	2			ns
t_{SU}	Data Setup Time	2↑			ns
t_H	Data Hold Time	3↑			ns
T_A	Free Air Operating Temperature	0		70	°C

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

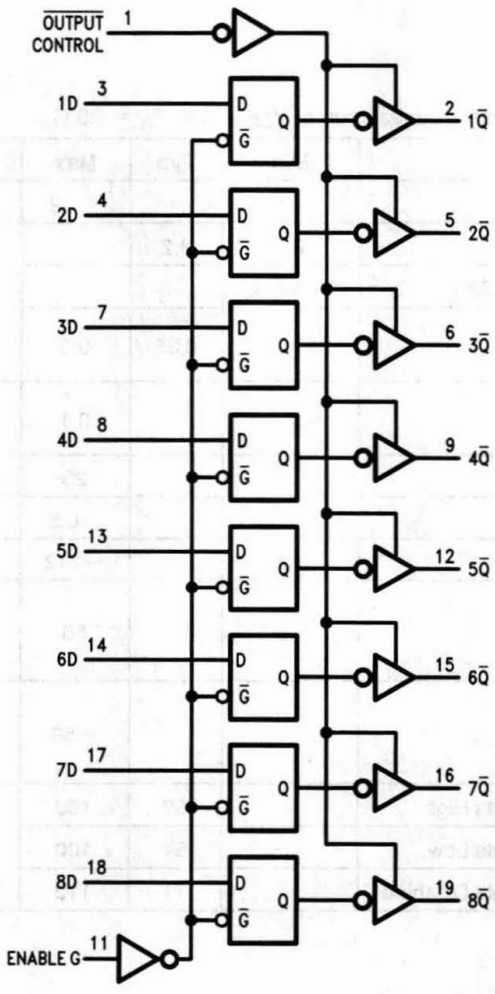
Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, I_{OH} = Max		2.4	3.2		V
		I_{OH} = −2 mA, V_{CC} = 4.5V to 5.5V		V_{CC} − 2			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = Max			0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = 5.5V, V_O = 2.7V				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V, V_O = 0.4V				−50	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		62	100	mA
			Outputs Low		64	100	
			Outputs Disabled		71	110	

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From	To	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	Data	Any $\overline{Q}$	4	7.5	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Data	Any $\overline{Q}$	4	7	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		Enable	Any $\overline{Q}$	5	9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Enable	Any $\overline{Q}$	4.5	8	ns
t_{PZH}	Output Enable Time to High Level Output		Output Control	Any $\overline{Q}$	2	6.5	ns
t_{PZL}	Output Enable Time to Low Level Output		Output Control	Any $\overline{Q}$	4.5	9.5	ns
t_{PHZ}	Output Disable Time from High Level Output		Output Control	Any $\overline{Q}$	3	6.5	ns
t_{PLZ}	Output Disable Time from Low Level Output		Output Control	Any $\overline{Q}$	3	7	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6311–2

Function Table

$\overline{\text{Output Control}}$	Enable G	D	Output $\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

L = Low State, H = High State, X = Don't Care

Z = High Impedance State

$\overline{Q}_0$ = Previous Condition of $\overline{Q}$

National Semiconductor Corporation

DM74AS534 Octal D-Type Edge-Triggered Flip-Flops with TRI-STATE® Outputs

General Description

These 8-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the AS534 are edge-triggered inverting D-type flip-flops. On the positive transition of the clock, the $\overline{Q}$ outputs will be set to the complement of the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

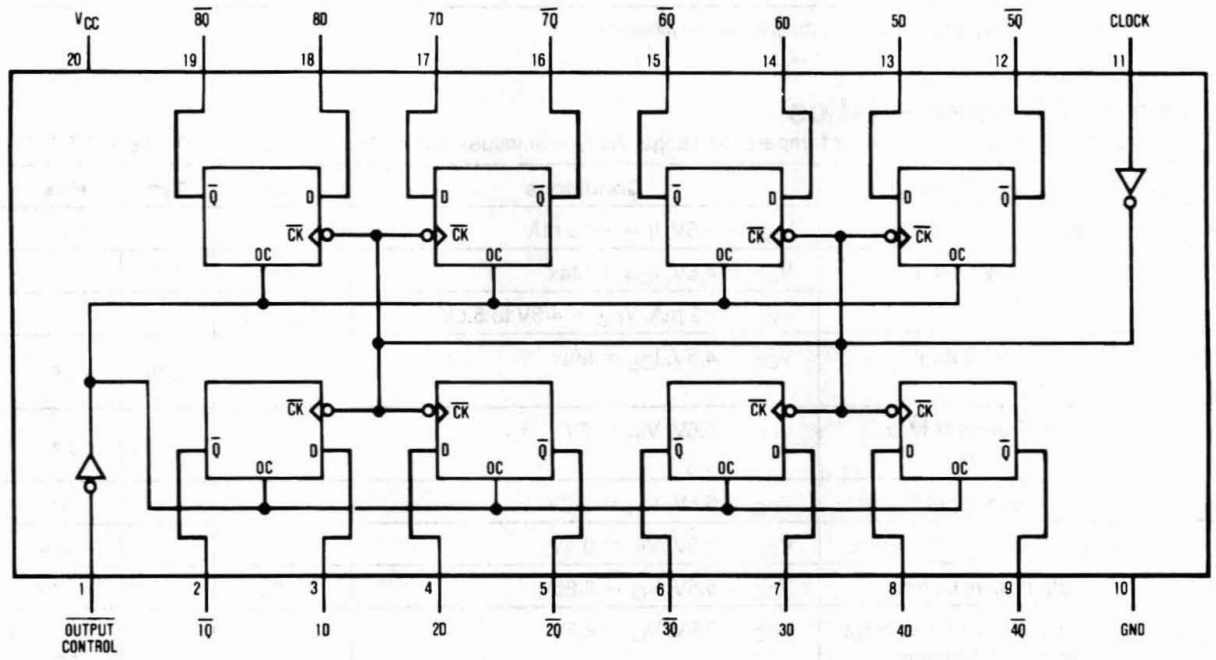
The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- TRI-STATE buffer-type outputs drive bus lines directly

Connection Diagram

Dual-In-Line Package



TL/F/6312–1

Order Number DM74AS534N
See NS Package Number N20A*

*Contact your local NSC representative about surface mount (M) package availability.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Voltage Applied to Disabled Output	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−15	mA
I_{OL}	Low Level Output Current				48	mA
f_{CLK}	Clock Frequency		0		125	MHz
t_W	Width of Clock Pulse	High	4			ns
		Low	3			
t_{SU}	Data Setup Time		2↑			ns
t_H	Data Hold Time		2↑			ns
T_A	Free Air Operating Temperature		0		70	°C

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, I_{OH} = Max		2.4	3.2		V
		I_{OH} = −2 mA, V_{CC} = 4.5V to 5.5V		V_{CC} − 2			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = Max			0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{OZH}	Off-State Output Current High Level Voltage Applied	V_{CC} = 5.5V, V_O = 2.7V				50	μA
I_{OZL}	Off-State Output Current Low Level Voltage Applied	V_{CC} = 5.5V, V_O = 0.4V				−50	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		77	120	mA
			Outputs Low		84	128	
			Outputs Disabled		84	128	

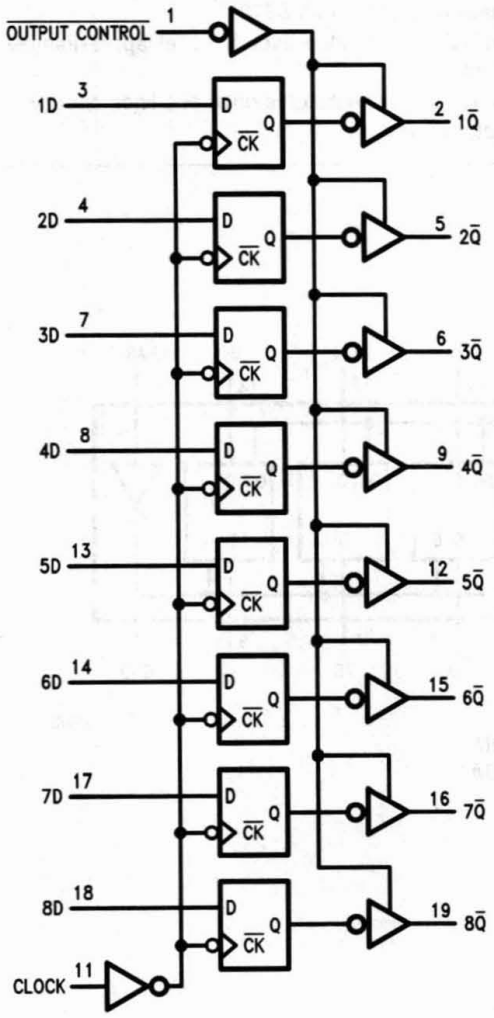
Switching Characteristics

over recommended operating free air temperature range (Note 1). All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions	From	To	Min	Max	Units
f_{MAX}		V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF			125		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output		Clock	Any $\overline{Q}$	3	8	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Clock	Any $\overline{Q}$	4	9	ns
t_{PZH}	Output Enable Time to High Level Output		Output Control	Any $\overline{Q}$	2	6	ns
t_{PZL}	Output Enable Time to Low Level Output		Output Control	Any $\overline{Q}$	3	10	ns
t_{PHZ}	Output Disable Time from High Level Output		Output Control	Any $\overline{Q}$	2	6	ns
t_{PLZ}	Output Disable Time from Low Level Output		Output Control	Any $\overline{Q}$	2	6	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6312–2

Function Table

$\overline{\text{Output Control}}$	Clock	D	Output $\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

L = Low State, H = High State, X = Don't Care

↑ = Positive Edge Transition

Z = High Impedance State

$\overline{Q}_0$ = Previous Condition of $\overline{Q}$

National Semiconductor Corporation

DM74AS573 Octal D-Type Transparent Latches with TRI-STATE® Outputs

General Description

These 8-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the AS573 are transparent D-type latches, meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was set up.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are off.

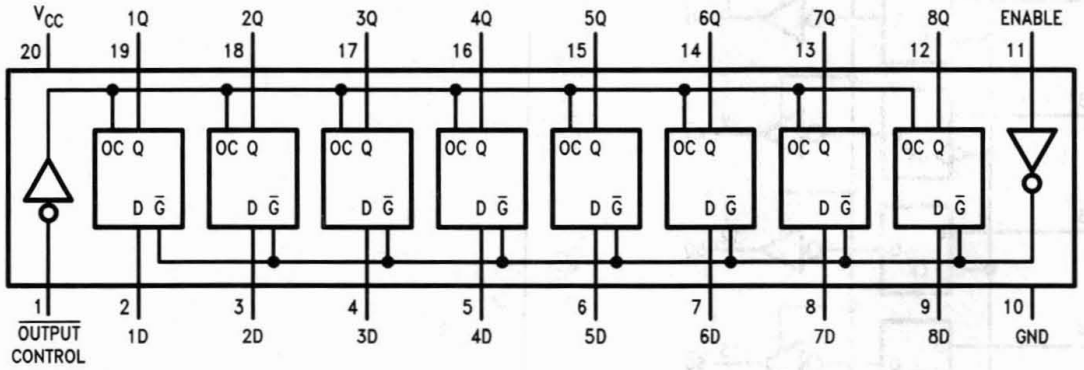
The pin-out is arranged to ease printed circuit board layout. All data inputs are on one side of the package while all the outputs are on the other side.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally equivalent with S373
- Improved AC performance over S373 at approximately half the power
- TRI-STATE buffer-type outputs drive bus lines directly
- Bus structured pinout

Connection Diagram

Dual-In-Line Package



TL/F/6313–1

Order Number DM74AS573N
See NS Package Number N20A*

*Contact your local NSC representative about surface mount (M) package availability.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Voltage Applied to Disabled Output	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−15	mA
I_{OL}	Low Level Output Current				48	mA
t_W	Width of Enable Pulse	High	4.5			ns
		Low	5.5			
t_{SU}	Data Setup Time		2↑			ns
t_H	Data Hold Time		3↑			ns
T_A	Free Air Operating Temperature		0		70	°C

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, V_{IL} = Max, I_{OH} = Max		2.4	3.3		V
		V_{CC} = 4.5V to 5.5V, I_{OH} = −2 mA		V_{CC} − 2			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, V_{IH} = 2V I_{OL} = Max			0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V, V_O = 2.7V				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V, V_O = 0.4V				−50	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		56	93	mA
			Outputs Low		55	90	
			Outputs Disabled		65	106	

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From	To	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	Data	Any Q	3	6	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Data	Any Q	3	6	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		Enable	Any Q	6	11.5	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Enable	Any Q	4	7.5	ns
t_{PZH}	Output Enable Time to High Level Output		Output Control	Any Q	2	6.5	ns
t_{PZL}	Output Enable Time to Low Level Output		Output Control	Any Q	4	9.5	ns
t_{PHZ}	Output Disable Time from High Level Output		Output Control	Any Q	2	6.5	ns
t_{PLZ}	Output Disable Time from Low Level Output		Output Control	Any Q	2	7	ns

Note 1: See Section 1 for test waveforms and output load.

Function Table

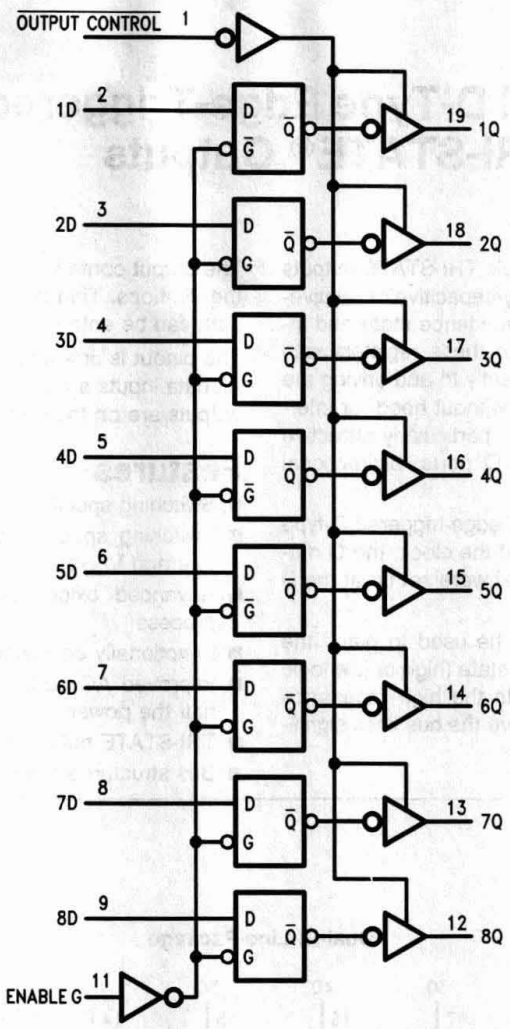
$\overline{\text{Output Control}}$	Enable G	D	Output Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

L = Low State, H = High State, X = Don't Care

Z = High Impedance State

Q_0 = Previous Condition of Q

Logic Diagram



TL/F/6313–2

National Semiconductor Corporation

DM74AS574 Octal D-Type Edge-Triggered Flip-Flops with TRI-STATE® Outputs

General Description

These 8-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the AS574 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

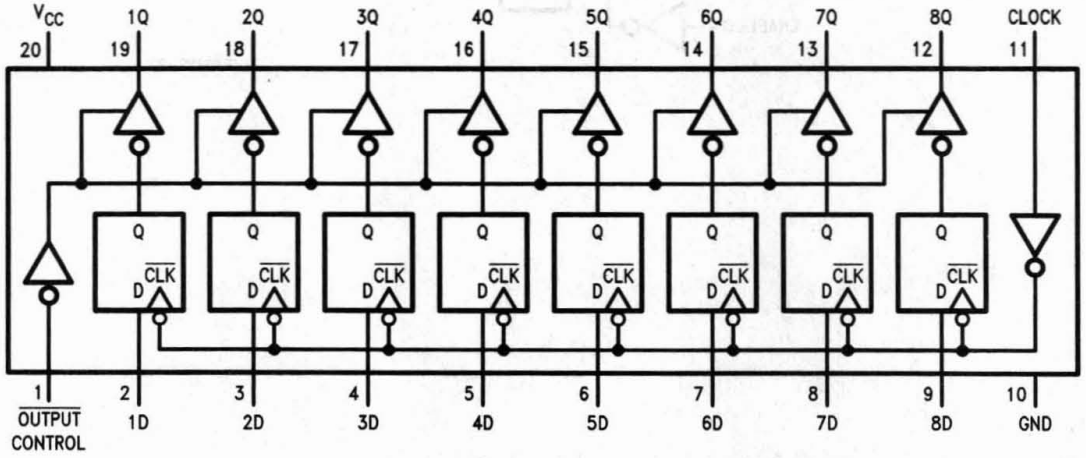
The pinout is arranged to ease printed circuit board layout. All data inputs are on one side of the package while all the outputs are on the other side.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally equivalent with S374
- Improved AC performance over S374 at approximately half the power
- TRI-STATE buffer-type outputs drive bus lines directly
- Bus structured pinout

Connection Diagram

Dual-In-Line Package



TL/F/6314–1

Order Number DM74AS574N
See NS Package Number N20A*

*Contact your local NSC representative about surface mount (M) package availability.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Voltage Applied to Disabled Output	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−15	mA
I_{OL}	Low Level Output Current				48	mA
f_{CLK}	Clock Frequency		0		80	MHz
t_{WCLK}	Width of Clock Pulse	High	4			ns
		Low	6			
t_{SU}	Data Setup Time		4↑			ns
t_H	Data Hold Time		2↑			ns
T_A	Free Air Operating Temperature		0		70	°C

The (↑) arrow indicates the positive edge of the clock is used for reference.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

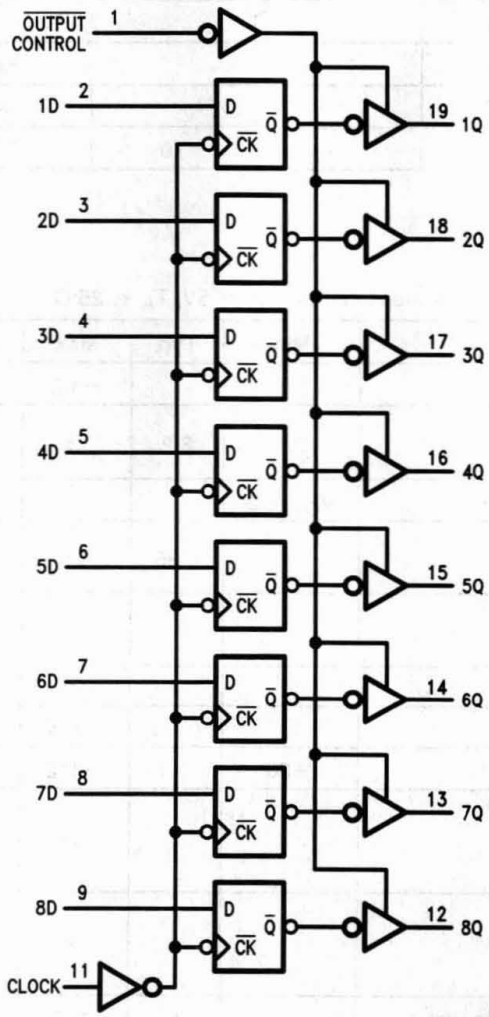
Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, V_{IL} = V_{IL} Max, I_{OH} = Max		2.4	3.2		V
		I_{OH} = −2 mA, V_{CC} = 4.5V to 5.5V		V_{CC} − 2			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, V_{IH} = 2V, I_{OL} = Max			0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V, V_O = 2.7V				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V, V_O = 0.4V				−50	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		73	116	mA
			Outputs Low		85	134	
			Outputs Disabled		84	134	

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From	To	Min	Max	Units
f_{MAX}	Maximum Clock Frequency	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF			80		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output		Clock	Any Q	3	8	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Clock	Any Q	4	9	ns
t_{PZH}	Output Enable Time to High Level Output		Output Control	Any Q	2	6	ns
t_{PZL}	Output Enable Time to Low Level Output		Output Control	Any Q	3	10	ns
t_{PHZ}	Output Disable Time from High Level Output		Output Control	Any Q	2	6	ns
t_{PLZ}	Output Disable Time from Low Level Output		Output Control	Any Q	2	6	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6314–2

Function Table

$\overline{\text{Output Control}}$	Clock	D	Output Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

L = Low State, H = High State, X = Don't Care

↑ = Positive Edge Transition

Z = High Impedance State

Q_0 = Previous Condition of Q

National Semiconductor Corporation

DM74AS575 Octal D-Type Edge-Triggered Flip-Flops with Synchronous Clear

General Description

These 8-bit registers feature totem-pole TRI-STATE® outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the AS575 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

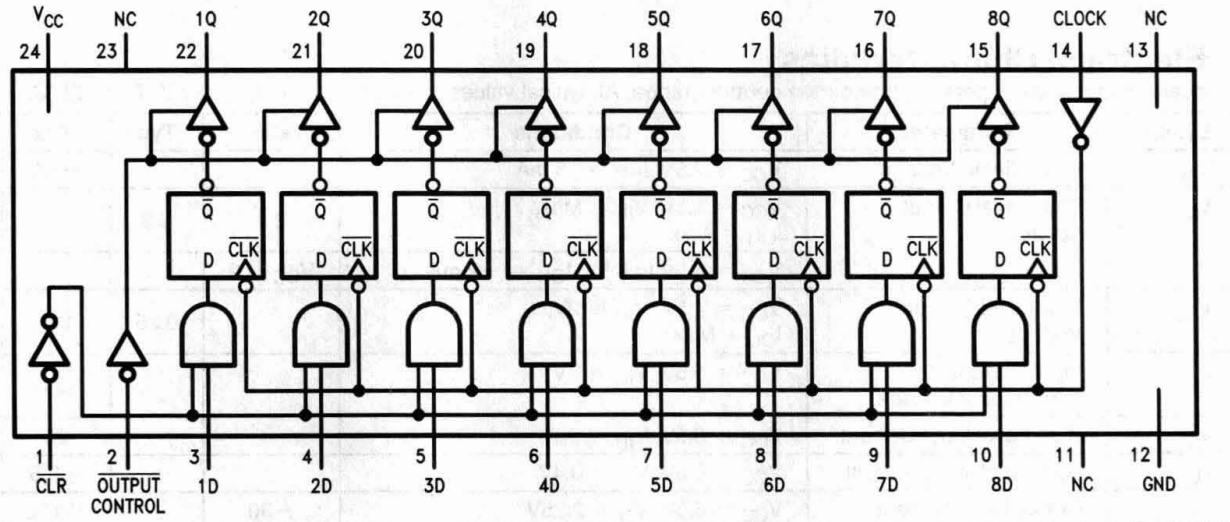
The pinout is arranged to ease printed circuit board layout. All data inputs are on one side of the package, while all the outputs are on the other side.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- TRI-STATE buffer-type outputs drive bus lines directly
- Synchronous clear
- Bus structured pinout

Connection Diagram

Dual-In-Line Package



TL/F/6315–1

Order Number DM74AS575N
See NS Package Number N20A*

*Contact your local NSC representative about surface mount (M) package availability.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Voltage Applied to Disabled Output	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−15	mA
I_{OL}	Low Level Output Current				48	mA
f_{CLK}	Clock Frequency		0		80	MHz
t_W	Width of Clock Pulse	High	4			ns
		Low	6			
t_{SU}	Data Setup Time	DATA	4↑			ns
		$\overline{CLR}$ High or Low	6↑			
t_H	Data Hold Time	DATA	2↑			ns
		$\overline{CLR}$	0↑			
T_A	Free Air Operating Temperature		0		70	°C

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

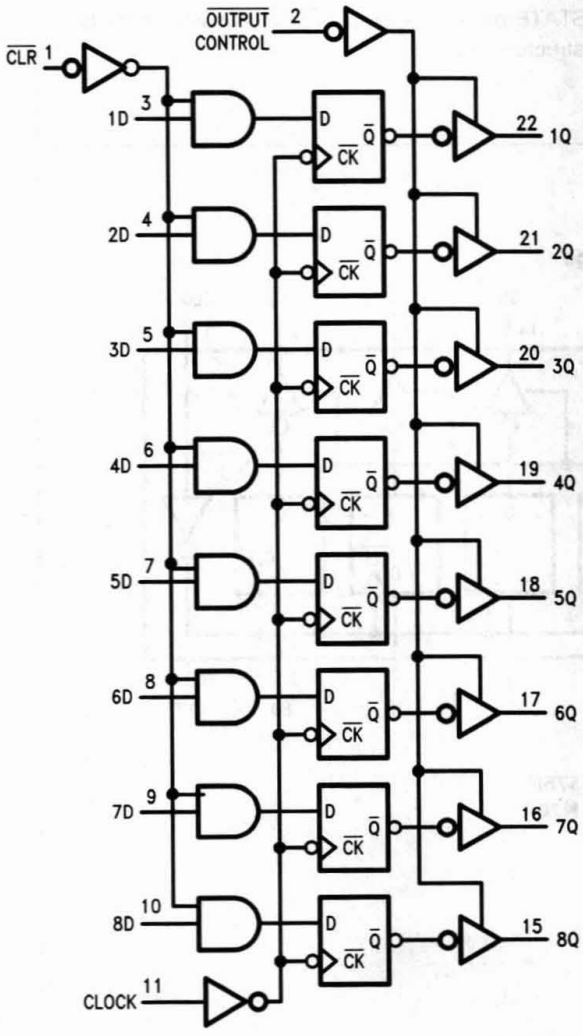
Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, V_{IL} = Max, I_{OH} = Max		2.4	3.3		V
		V_{CC} = 4.5V to 5.5V, I_{OH} = −2 mA		V_{CC} − 2			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, V_{IH} = 2V, I_{OL} = Max			0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V, V_O = 2.7V				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V, V_O = 0.4V				−50	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		78	126	mA
			Outputs Low		88	142	
			Outputs Disabled		88	142	

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From	To	Min	Max	Units
f_{MAX}	Maximum Clock Frequency	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF			80		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output		Clock	Any Q	3	8	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Clock	Any Q	4	9.5	ns
t_{PZH}	Output Enable Time to High Level Output		Output Control	Any Q	2	6	ns
t_{PZL}	Output Enable Time to Low Level Output		Output Control	Any Q	3	10	ns
t_{PHZ}	Output Disable Time from High Level Output		Output Control	Any Q	2	6	ns
t_{PLZ}	Output Disable Time from Low Level Output		Output Control	Any Q	2	6	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6315–2

Function Table

$\overline{\text{Output Control}}$	$\overline{\text{CLR}}$	Clock	D	Output Q
L	L	↑	X	L
L	H	↑	H	H
L	H	↑	L	L
L	H	L	X	Q_0
H	X	X	X	Z

L = Low State, H = High State, X = Don't Care

↑ = Positive Edge Transition

Z = High Impedance State

Q_0 = Previous Condition of Q

NC = No Internal Connection

National Semiconductor Corporation

DM74AS576 Octal D-Type Edge-Triggered Flip-Flops with Inverted Outputs

General Description

These 8-bit registers feature totem-pole TRI-STATE® outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the AS576 are edge-triggered inverting D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the complement of the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

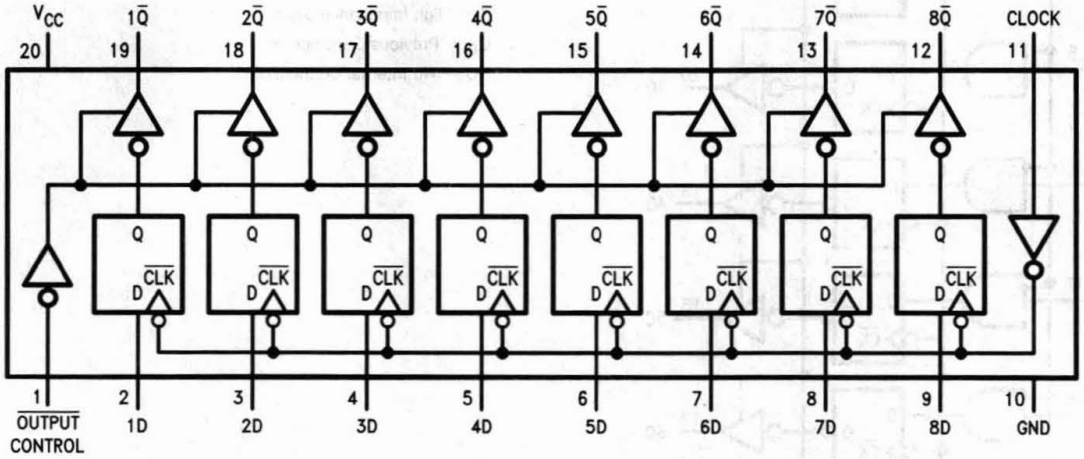
The pinout is arranged to ease printed circuit board layout. All data inputs are on one side of the package while the outputs are on the other side.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- TRI-STATE buffer-type outputs drive bus lines directly
- Bus structured pinout

Connection Diagram

Dual-In-Line Package



TL/F/6316–1

Order Number DM74AS576N
See NS Package Number N20A*

*Contact your local NSC representative about surface mount (M) package availability.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Voltage Applied to Disabled Output	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−15	mA
I_{OL}	Low Level Output Current				48	mA
f_{CLOCK}	Clock Frequency		0		80	MHz
t_W	Width of Enable Pulse	High	4			ns
		Low	6			
t_{SU}	Data Setup Time		4↑			ns
t_H	Data Hold Time		2↑			ns
T_A	Free Air Operating Temperature		0		70	°C

The (↑) arrow indicates the positive edge of the clock is used for reference.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

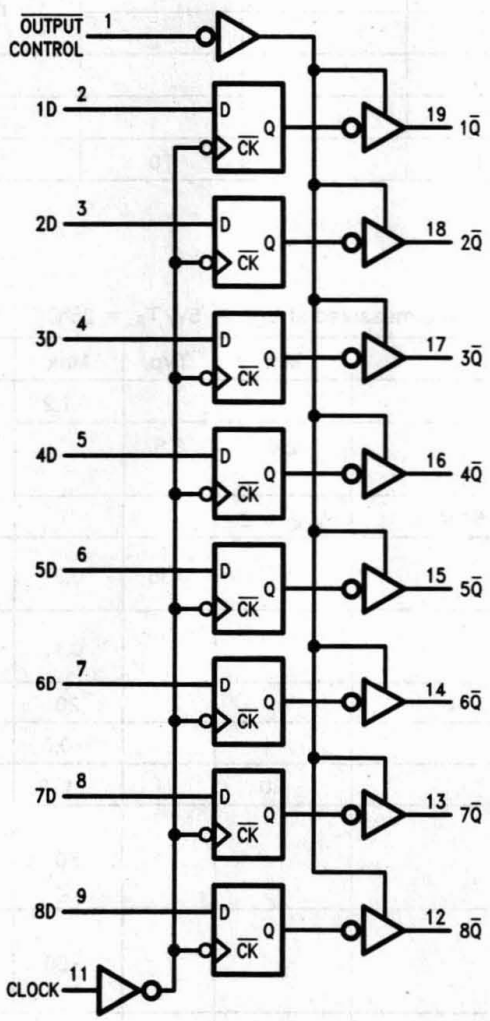
Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, V_{IL} = V_{IL} Max, I_{OH} = Max		2.4	3.3		V
		I_{OH} = −2 mA, V_{CC} = 4.5V to 5.5V		V_{CC} − 2			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, V_{IH} = 2V I_{OL} = Max			0.35	0.5	V
I_I	Input Current @ Max. Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V V_O = 2.7V				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V V_O = 0.4V				−50	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		77	125	mA
			Outputs Low		84	135	
			Outputs Disabled		84	135	

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From	To	Min	Max	Units
f_{MAX}	Maximum Clock Frequency	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF			80		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output		Clock	Any $\overline{Q}$	3	8	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Clock	Any $\overline{Q}$	4	9	ns
t_{PZH}	Output Enable Time to High Level Output		Output Control	Any $\overline{Q}$	2	6	ns
t_{PZL}	Output Enable Time to Low Level Output		Output Control	Any $\overline{Q}$	3	10	ns
t_{PHZ}	Output Disable Time from High Level Output		Output Control	Any $\overline{Q}$	2	6	ns
t_{PLZ}	Output Disable Time from Low Level Output		Output Control	Any $\overline{Q}$	2	6	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6316–2

Function Table

$\overline{\text{Output Control}}$	Clock	D	Output $\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

L = Low State, H = High State, X = Don't Care

↑ = Positive Edge Transition

Z = High Impedance State

$\overline{Q}_0$ = Previous Condition of $\overline{Q}$

National Semiconductor Corporation

DM74AS577 Octal D-Type Edge-Triggered Flip-Flops with Inverted Outputs and Synchronous Preset

General Description

These 8-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the AS577 are edge-triggered inverting D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the complement of the logic states that were set up at the $\overline{D}$ inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

When the CLR is held on during a positive transition of the clock the $\overline{Q}$ outputs of the flip-flops with go high.

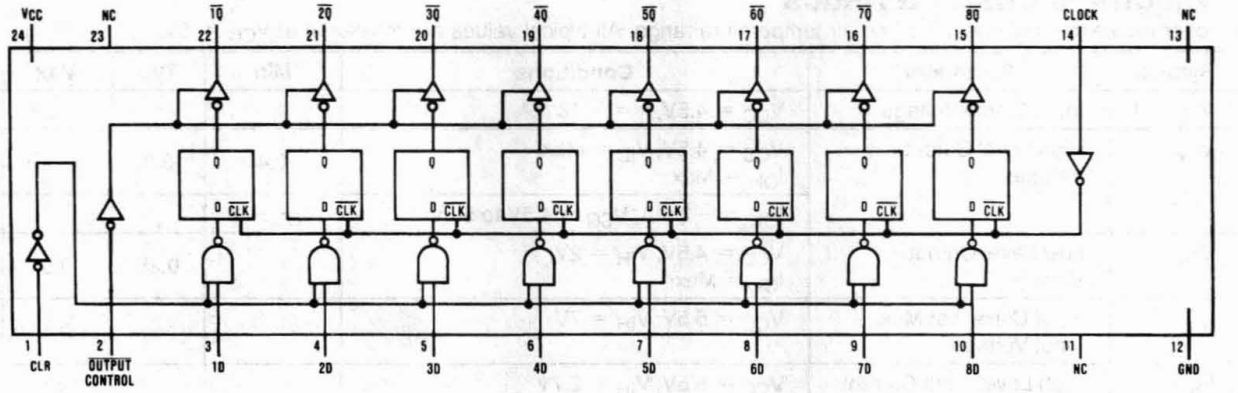
The pinout is arranged to ease printed circuit board layout. All data inputs are on one side of the package, while all the outputs are on the other side.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- TRI-STATE buffer-type outputs drive bus lines directly
- Synchronous preset
- Bus structured pinout

Connection Diagram

Dual-In-Line Package



TL/F/6317–1

Order Number DM74AS577N
See NS Package Number N24A*

*Contact your local NSC representative about surface mount (M) package availability.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Voltage Applied to Disabled Output	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−15	mA
I_{OL}	Low Level Output Current				48	mA
f_{CLK}	Clock Frequency		0		80	MHz
t_{WCLK}	Width of Clock Pulse	High	4			ns
		Low	6			ns
t_{SU}	Data Setup Time	Data	4↑			ns
		$\overline{CLR}$	6↑			ns
t_H	Data Hold Time	Data	2↑			ns
		$\overline{CLR}$	0↑			ns
T_A	Free Air Operating Temperature		0		70	°C

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

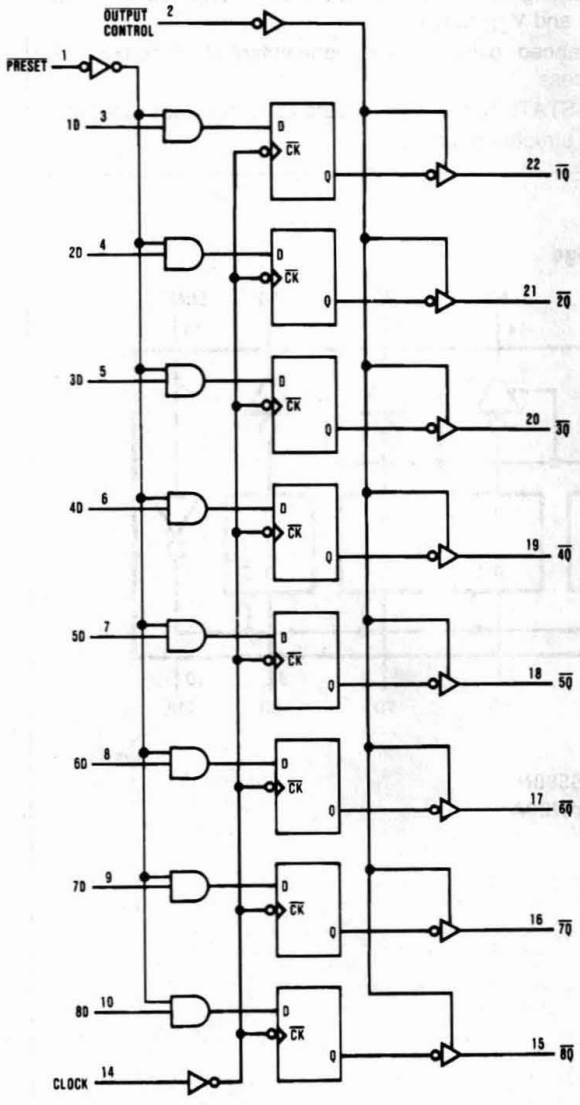
Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, V_{IL} = Max, I_{OH} = Max		2.4	3.3		V
		I_{OH} = −2 mA, V_{CC} = 4.5V to 5.5V		V_{CC} − 2			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, V_{IH} = 2V, I_{OL} = Max			0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V, V_O = 2.7V				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V, V_O = 0.4V				−50	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		78	126	mA
			Outputs Low		76	123	
			Outputs Disabled		88	142	

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From	To	Min	Max	Units
f_{MAX}	Maximum Clock Frequency	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF			80		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output		Clock	Any $\overline{Q}$	3	8	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Clock	Any $\overline{Q}$	4	9.5	ns
t_{PZH}	Output Enable Time to High Level Output		Output Control	Any $\overline{Q}$	2	6	ns
t_{PZL}	Output Enable Time to Low Level Output		Output Control	Any $\overline{Q}$	3	10	ns
t_{PHZ}	Output Disable Time from High Level Output		Output Control	Any $\overline{Q}$	2	6	ns
t_{PLZ}	Output Disable Time from Low Level Output		Output Control	Any $\overline{Q}$	2	6	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6317–2

Function Table

Output Control	CLR	Clock	$\overline{D}$	Output $\overline{Q}$
L	L	↑	X	H
L	H	↑	H	L
L	H	↑	L	H
L	H	L	X	$\overline{Q}_0$
H	X	X	X	Z

L = Low State, H = High State, X = Don't Care

↑ = Positive Edge Transition

Z = High Impedance State

$\overline{Q}_0$ = Previous Condition of $\overline{Q}$

National Semiconductor Corporation

DM74AS580 Octal D-Type Transparent Latches with TRI-STATE® Outputs

General Description

These 8-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight inverting latches of the AS580 are transparent D-type latches, meaning that while the enable (G) is high the Q outputs will follow the complement of the data (D) inputs. When the enable is taken low the output will be latched at the complement of the level of the data that was set up.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are off.

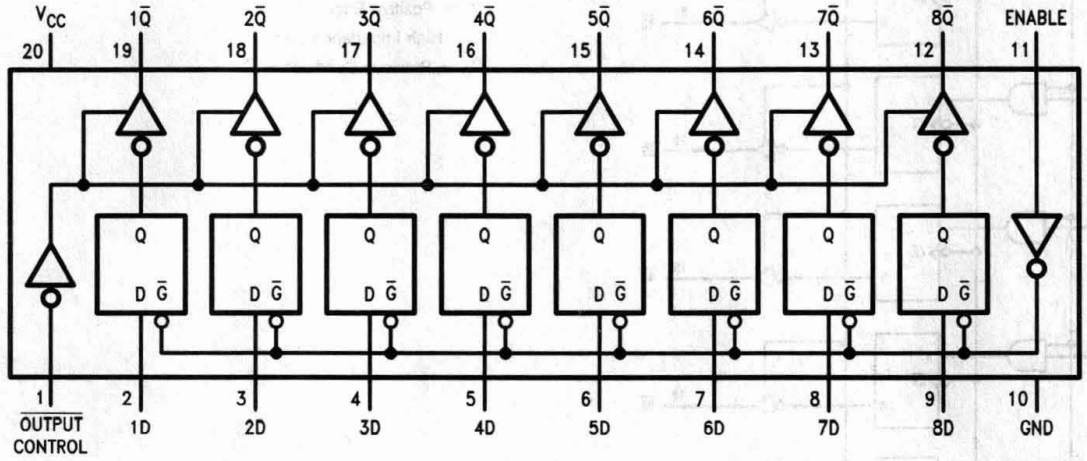
The pinout is arranged to ease printed circuit board layout. All data inputs are on one side of the package while all the outputs are on the other side.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- TRI-STATE buffer-type outputs drive bus lines directly
- Bus structured pinout

Connection Diagram

Dual-In-Line Package



TL/F/6318–1

Order Number DM74AS580N
See NS Package Number N20A*

*Contact your local NSC representative about surface mount (M) package availability.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Voltage Applied to Disabled Output	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−15	mA
I_{OL}	Low Level Output Current			48	mA
t_W	Width of Enable Pulse, High or Low	2			ns
t_{SU}	Data Setup Time	2			ns
t_H	Data Hold Time	3			ns
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, V_{IL} = V_{IL} Max, I_{OH} = Max		2.4	3.3		V
		I_{OH} = −2 mA, V_{CC} = 4.5V to 5.5V		V_{CC} − 2			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, V_{IH} = 2V, I_{OL} = Max			0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V, V_O = 2.7V				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V, V_O = 0.4V				−50	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		62	100	mA
			Outputs Low		65	106	
			Outputs Disabled		71	115	

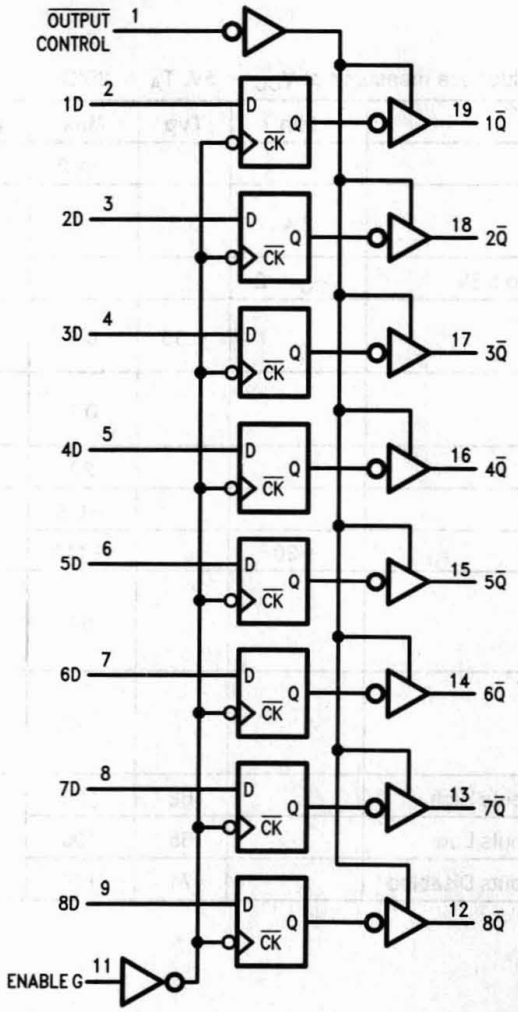
Switching Characteristics

over recommended operating free air temperature range (Note 1). All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions	From	To	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	Data	Any $\overline{Q}$	3	7.5	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Data	Any $\overline{Q}$	3	7	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		Enable	Any $\overline{Q}$	5	9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Enable	Any $\overline{Q}$	4	8	ns
t_{PZH}	Output Enable Time to High Level Output		Output Control	Any $\overline{Q}$	2	6.5	ns
t_{PZL}	Output Enable Time to Low Level Output		Output Control	Any $\overline{Q}$	4	9.5	ns
t_{PHZ}	Output Disable Time from High Level Output		Output Control	Any $\overline{Q}$	2	6.5	ns
t_{PLZ}	Output Disable Time from Low Level Output		Output Control	Any $\overline{Q}$	2	7	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6318–2

Function Table

Output Control	Enable G	D	Output $\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

L = Low State, H = High State, X = Don't Care

Z = High Impedance State

$\overline{Q}_0$ = Previous Condition of $\overline{Q}$

National Semiconductor Corporation

DM74AS620 Octal Bus Transceiver

General Description

This octal bus transceiver is designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

This device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the enable inputs ($\overline{G}$BA and GAB).

The enable inputs can be used to disable the device so that the buses are effectively isolated.

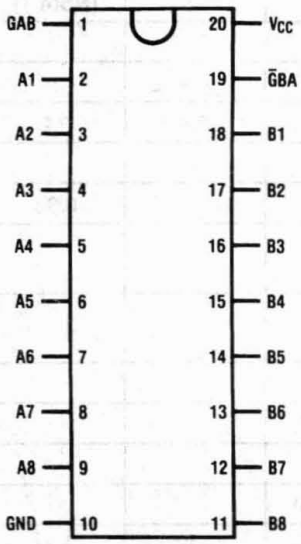
The dual-enable configuration gives the octal bus transceivers the capability of storing data by simultaneous enabling of $\overline{G}$BA and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states.

Features

- Local bus-latch capability
- Choice of true or inverting logic
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range

Connection Diagram

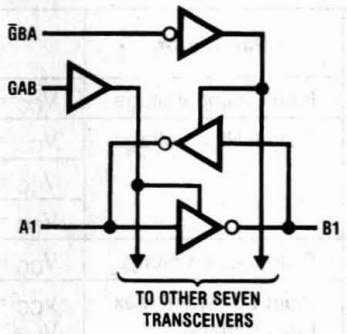
Dual-In-Line Package



TL/F/6319–1

Top View
Order Number DM74AS620N
See NS Package Number N20A*

Logic Diagram



TL/F/6319–2

Function Table

Enable Inputs		Operation
$\overline{G}$BA	GAB	
L	L	$\overline{B}$ Data to A Bus
H	H	$\overline{A}$ Data to B Bus
H	L	Isolation
L	H	$\overline{B}$ Data to A Bus, $\overline{A}$ Data to B Bus

*Contact your local NSC representative about surface mount (M) package availability.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage (I/O ports)	5.5V
Input Voltage (all other inputs)	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−15	mA
I_{OL}	Low Level Output Current			64	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	Output High Voltage	V_{CC} = 4.5V to 5.5V, I_{OH} = −2 mA		V_{CC} − 2			V
		V_{CC} = 4.5V, I_{OH} = −3 mA		2.4	3.2		
		V_{CC} = 4.5V, I_{OH} = Max		2			
V_{OL}	Output Low Voltage	V_{CC} = 4.5V, I_{OL} = Max			0.35	0.55	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_I = 7V	Control Inputs			0.1	mA
		V_{CC} = 5.5V, V_I = 5.5V	A or B Ports			0.1	
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_I = 2.7V	Control Inputs			20	μA
			A or B Ports (Note 3)			70	
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_I = 0.4V	Control Inputs			−0.5	mA
			A or B Ports (Note 3)			−0.75	
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V (Note 2)		−50		−150	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		35	57	mA
			Outputs Low		74	122	
			Outputs Disabled		48	77	

Note 1: All typical values are at V_{CC} = 5V, T_A = 25°C.

Note 2: The output conditions have been chosen to produce a current that closely approximates one half of the true short circuit output current, I_{OS}.

Note 3: For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

AS620 Switching Characteristics over recommended free air temperature range (Note 1)

Symbol	Parameter	Conditions	From (Input) To (Output)	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V C_L = 50 pF R1 = 500Ω R2 = 500Ω T_A = Min to Max	A to B	1	7	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		A to B	2	6	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		B to A	1	7	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		B to A	2	6	ns
t_{PZH}	Output Enable Time to High Level Output		$\overline{G}$BA to A	2	8	ns
t_{PZL}	Output Enable Time to Low Level Output		$\overline{G}$BA to A	2	9	ns
t_{PHZ}	Output Disable Time from High Level Output		$\overline{G}$BA to A	1	6	ns
t_{PLZ}	Output Disable Time from Low Level Output		$\overline{G}$BA to A	2	12	ns
t_{PZH}	Output Enable Time to High Level Output		GAB to B	2	8	ns
t_{PZL}	Output Enable Time to Low Level Output		GAB to B	2	9	ns
t_{PHZ}	Output Disable Time from High Level Output		GAB to B	1	6	ns
t_{PLZ}	Output DisableTime from Low Level Output		GAB to B	2	13	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM74AS640 TRI-STATE® Octal Bus Transceiver

General Description

This advanced Schottky device contains 8 pairs of TRI-STATE logic elements configured as octal bus transceiver. This circuit is designed for use in memory, microprocessor systems and in asynchronous bidirectional data buses. This device transmits data from the A bus to the B bus, or vice versa, depending upon the logic level of the direction control input (DIR). The enable input ($\overline{G}$) can be used to disable the devices, effecting isolation of buses A and B.

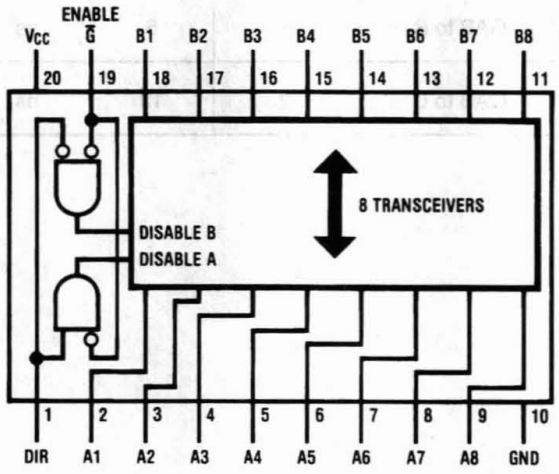
The TRI-STATE circuitry also contains a protection feature that prevents these transceivers from glitching the bus during power-up or power-down.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky, low power Schottky, and advanced low power Schottky TTL counterpart
- Improved AC performance over Schottky, low power Schottky, and advanced low power Schottky counterparts
- TRI-STATE outputs independently controlled on A and B buses
- Low output impedance drive to drive terminated transmission lines to 133Ω
- Specified to interface with CMOS at $V_{OH} = V_{CC} - 2V$

Connection Diagram

Dual-In-Line Package



TL/F/6708–1

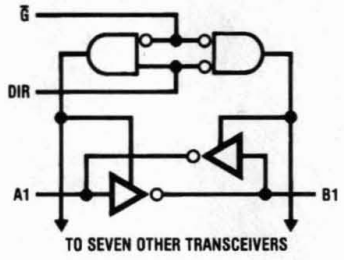
Top View

Order Number DM74AS640N
See NS Package Number N20A*

Function Table

Control Inputs		Operation
$\overline{G}$	DIR	
L	L	$\overline{B}$ Data to A Bus
L	H	$\overline{A}$ Data to B Bus
H	X	Isolation

Logic Diagram



TL/F/6708–2

*Contact your local NSC representative about surface mount (M) package availability.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	
Control Inputs	7V
I/O Ports	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−15	mA
I_{OL}	Low Level Output Current			64	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V, I_{OH} = −2 mA		V_{CC} − 2			V
		V_{CC} = 4.5V, I_{OH} = −3 mA		2.4			V
		V_{CC} = 4.5V, I_{OH} = Max		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max			0.35	0.55	V
I_I	Input Current at Max Input Voltage	V_{CC} = Max, V_I = 7V, (V_I = 5.5V for A or B Ports)				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V (Note 2)	Control Inputs			20	μA
			A or B Ports			70	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V (Note 2)	Control Inputs			−0.5	mA
			A or B Ports			−0.75	
I_O	Output Drive Current	V_{CC} = Max, V_O = 2.25V		−50		−150	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			37	58	mA
I_{CCL}	Supply Current with Outputs Low				78	123	mA
I_{CCZ}	Supply Current with Outputs in TRI-STATE				51	80	mA

Note 1: All typicals are at V_{CC} = 5.0V, T_A = 25°C.

Note 2: For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current, I_{OZH} and I_{OZL}.

Switching Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	From (Input)	To (Output)	V_{CC} = Min to Max, C_L = 50 pF, R_1 = R_2 = 500Ω		Units
				Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	A or B	B or A	2	7	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A or B	B or A	2	6	ns
t_{PZH}	Output Enable Time to High Level Output	$\overline{G}$	A or B	2	8	ns
t_{PZL}	Output Enable Time to Low Level Output	$\overline{G}$	A or B	2	10	ns
t_{PHZ}	Output Disable Time from High Level Output	$\overline{G}$	A or B	2	8	ns
t_{PLZ}	Output Disable Time from Low Level Output	$\overline{G}$	A or B	2	13	ns

National Semiconductor Corporation

DM74AS645 TRI-STATE® Octal Bus Transceiver

General Description

This advanced Schottky device contains 8 pairs of TRI-STATE logic elements configured as an octal bus transceiver. This circuit is designed for use in memory, microprocessor systems and in asynchronous bidirectional data buses. This device transmits data from the A bus to the B bus, or vice versa, depending upon the logic level of the direction control input (DIR). The enable input ($\overline{G}$) can be used to disable the devices, effecting isolation of buses A and B.

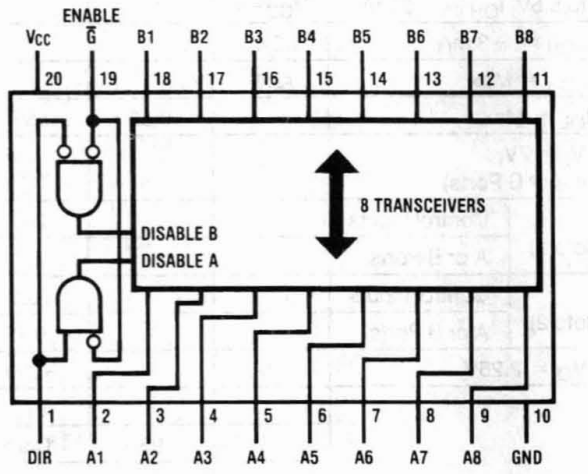
The TRI-STATE circuitry also contains a protection feature that prevents these transceivers from glitching the bus during power-up or power-down.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky, low power Schottky, and advanced low power Schottky TTL counterpart
- Improved AC performance over Schottky, low power Schottky, and advanced low power Schottky counterparts
- TRI-STATE outputs independently controlled on A and B buses
- Low output impedance drive to drive terminated transmission lines to 133Ω
- Specified to interface with CMOS at $V_{OH} = V_{CC} - 2V$

Connection Diagram

Dual-In-Line Package



TL/F/9311–1

Top View

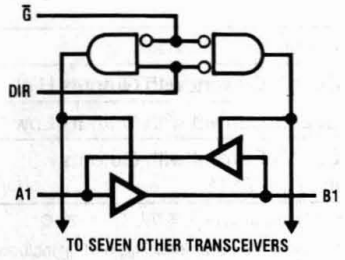
Order Number DM74AS645N
See NS Package Number N20A*

Function Table

Control Inputs		Operation
$\overline{G}$	DIR	
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	Isolation

Logic Diagram

DM74AS645



TL/F/9311–2

*Contact your local NSC representative about surface mount (M) package availability.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	
Control Inputs	7V
I/O Ports	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−15	mA
I_{OL}	Low Level Output Current			64	mA
T_A	Free Air Operating Temperature	0		70	°C

DM74AS645 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V, I_{OH} = −2 mA		V_{CC}−2			V
		V_{CC} = 4.5V, I_{OH} = −3 mA		2.4			V
		V_{CC} = 4.5V, I_{OH} = Max		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max			0.35	0.55	V
I_I	Input Current at Max Input Voltage	V_{CC} = Max, V_I = 7V, (V_I = 5.5V for A or B Ports)				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V (Note 2)	Control Inputs			20	μA
			A or B Ports			70	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V (Note 2)	Control Inputs			−0.5	mA
			A or B Ports			−0.75	
I_O	Output Drive Current	V_{CC} = Max, V_O = 2.25V		−50		−150	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			62	97	mA
I_{CCL}	Supply Current with Outputs Low				95	149	mA
I_{CC}	Supply Current with Outputs in TRI-STATE				79	123	mA

Note 1: All typicals are at V_{CC} = 5.0V, T_A = 25°C.

Note 2: For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current, I_{OZH} and I_{OZL}.

Switching Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	From (Input)	To (Output)	V_{CC} = Min to Max, C_L = 50 pF, R_1 = R_2 = 500Ω		Units
				Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	A or B	B or A	2	9.5	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A or B	B or A	2	9	ns
t_{PZH}	Output Enable Time to High Level Output	$\overline{G}$	A or B	2	11	ns
t_{PZL}	Output Enable Time to Low Level Output	$\overline{G}$	A or B	2	10	ns
t_{PHZ}	Output Disable Time from High Level Output	$\overline{G}$	A or B	2	7	ns
t_{PLZ}	Output Disable Time from Low Level Output	$\overline{G}$	A or B	2	12	ns

National Semiconductor Corporation

DM74AS646/DM74AS648 Octal Bus Transceivers and Registers

General Description

These devices incorporate an octal bus transceiver and an octal D-type register configured to enable multiplexed transmission of data from bus to bus or internal register to bus.

These bus transceivers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these devices with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The registers in the AS646, 648 are edge-triggered D-type flip-flops. On the positive transition of the clock (CAB or CBA), the input bus data is stored.

The SAB and SBA control pins are provided to select whether real-time data or stored data is transferred. A low input level selects real-time data, and a high level selects stored data. The select controls have a "make before break" configuration to eliminate a glitch which would normally occur in a typical multiplexer during the transition between stored and real-time data.

The enable $\overline{G}$ and direction control pins provide four modes of operation; real-time data transfer from bus A to B, real-time data transfer from bus B to A, real-time bus A and/or B data transfer to internal storage, or internal store data transfer to bus A or B.

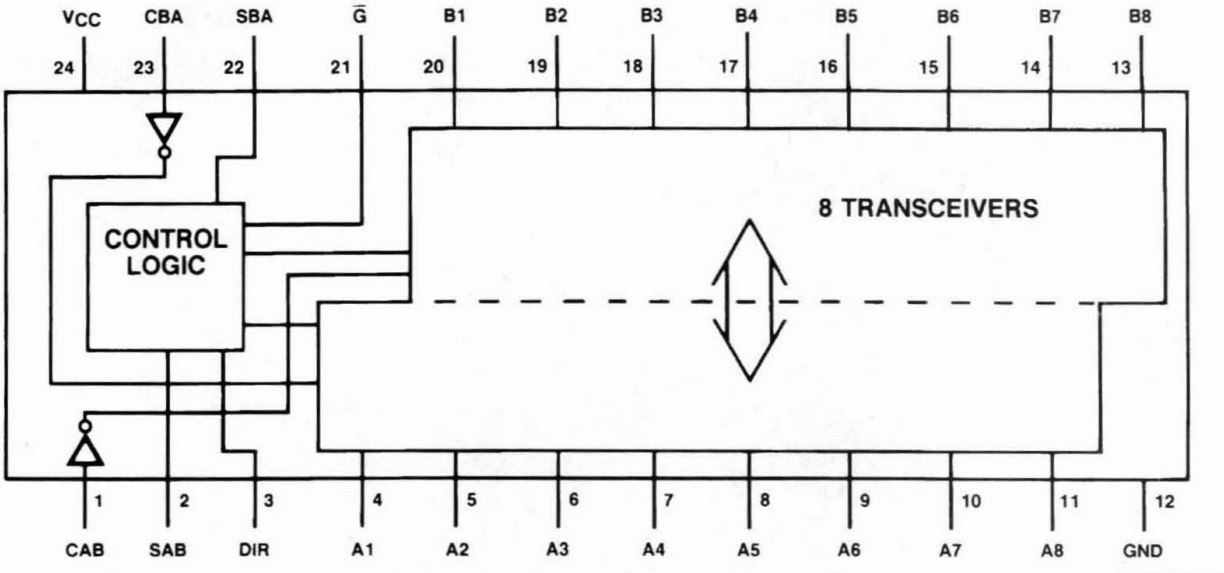
When the enable $\overline{G}$ pin is low, the direction pin selects which bus receives data. When the enable $\overline{G}$ pin is high, both buses become disabled yet their input function is still enabled.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin-for-pin compatible with LS TTL counterpart
- TRI-STATE® buffer-type outputs drive bus lines directly

Connection Diagram

Dual-In-Line Package



TL/F/6324–1

Order Number DM74AS646NT or DM74AS648NT
See NS Package Number N24C*

*Contact your local NSC representative about surface mount (M) package availability.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	
Control Inputs	7V
I/O Ports	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM74AS646, 648			Units
			Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−15	mA
I_{OL}	Low Level Output Current				48	mA
f_{CLK}	Clock Frequency		0		90	MHz
t_W	Width of Clock Pulse	High	5			ns
		Low	6			ns
t_{SU}	Data Setup Time		6↑			ns
t_H	Data Hold Time		0↑			ns
T_A	Free Air Operating Temperature		0		70	°C

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions			Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA					−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, V_{IL} = Max, V_{IH} = Min		I_{OH} = Max	2			V
				I_{OH} = −3 mA	2.4	3.2		
		V_{CC} = 4.5V to 5.5V, I_{OH} = −2 mA			V_{CC} − 2			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, V_{IL} = Min, V_{IH} = 2V, I_{OL} = Max				0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V	V_I = 7V	Control Inputs			0.1	mA
			V_I = 5.5V	A or B Ports			0.1	
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V (Note 1)		Control Inputs			20	μA
				A or B Ports			70	
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V (Note 1)		Control Inputs			−0.5	mA
				A or B Ports			−0.75	
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V			−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	'AS646	Outputs High		120	195	mA
				Outputs Low		130	211	
				Outputs Disabled		130	211	
			'AS648	Outputs High		110	185	
				Outputs Low		120	195	
				Outputs Disabled		120	195	

Note 1: For I/O ports, the parameters I_{IH} and I_{IL} include the off-state current, I_{OZH} and I_{OZL}.

3

'AS646 Switching Characteristics over recommended operating free air temperature range (Note 1).

Symbol	Parameter	Conditions	From (Input)	To (Output)	DM74AS646		Units
					Min	Max	
f_{MAX}	Maximum Clock Frequency	V_{CC} = 4.5V to 5.5V, $R_1 = R_2 = 500\Omega$, C_L = 50 pF (Note 1)			90		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output		CBA or CAB	A or B	2	8.5	ns
t_{PHL}	Propagation Delay Time High to Low Level Output				2	9	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		A or B	B or A	2	9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output				1	7	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		SBA or SAB (Note 2)	A or B	2	11	ns
t_{PHL}	Propagation Delay Time High to Low Level Output				2	9	ns
t_{PZH}	Output Enable Time to High Level Output		Enable $\overline{G}$	A or B	2	9	ns
t_{PZL}	Output Enable Time to Low Level Output				3	14	ns
t_{PHZ}	Output Disable Time from High Level Output				2	9	ns
t_{PLZ}	Output Disable Time from Low Level Output				2	9	ns
t_{PZH}	Output Enable Time to High Level Output		DIR	A or B	3	16	ns
t_{PZL}	Output Enable Time to Low Level Output				3	18	ns
t_{PHZ}	Output Disable Time from High Level Output				2	10	ns
t_{PLZ}	Output Disable Time from Low Level Output				2	10	ns

Note 1: See Section 1 for test waveforms and output load.

Note 2: These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

'AS648 Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From (Input)	To (Output)	DM74AS648 Min	DM74AS648 Max	Units
f_{MAX}	Maximum Clock Frequency	V_{CC} = 4.5V to 5.5V, $R_1 = R_2 = 500\Omega$, C_L = 50 pF (Note 1)			90		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output		CAB or CBA	A or B	2	8.5	ns
t_{PHL}	Propagation Delay Time High to Low Level Output				2	9	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		A or B	B or A	2	8	ns
t_{PHL}	Propagation Delay Time High to Low Level Output				1	7	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		SBA or SAB (Note 2)	A or B	2	11	ns
t_{PHL}	Propagation Delay Time High to Low Level Output				2	9	ns
t_{PZH}	Output Enable Time to High Level Output		Enable $\overline{G}$	A or B	2	9	ns
t_{PZL}	Output Enable Time to Low Level Output				3	15	ns
t_{PHZ}	Output Disable Time from High Level Output				2	9	ns
t_{PLZ}	Output Disable Time from Low Level Output				2	9	ns
t_{PZH}	Output Enable Time to High Level Output		DIR	Bus	3	16	ns
t_{PZL}	Output Enable Time to Low Level Output				3	18	ns
t_{PHZ}	Output Disable Time from High Level Output				2	10	ns
t_{PLZ}	Output Disable Time from Low Level Output				2	10	ns

Note 1: See Section 1 for test waveforms and output load.

Note 2: These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

Function Table

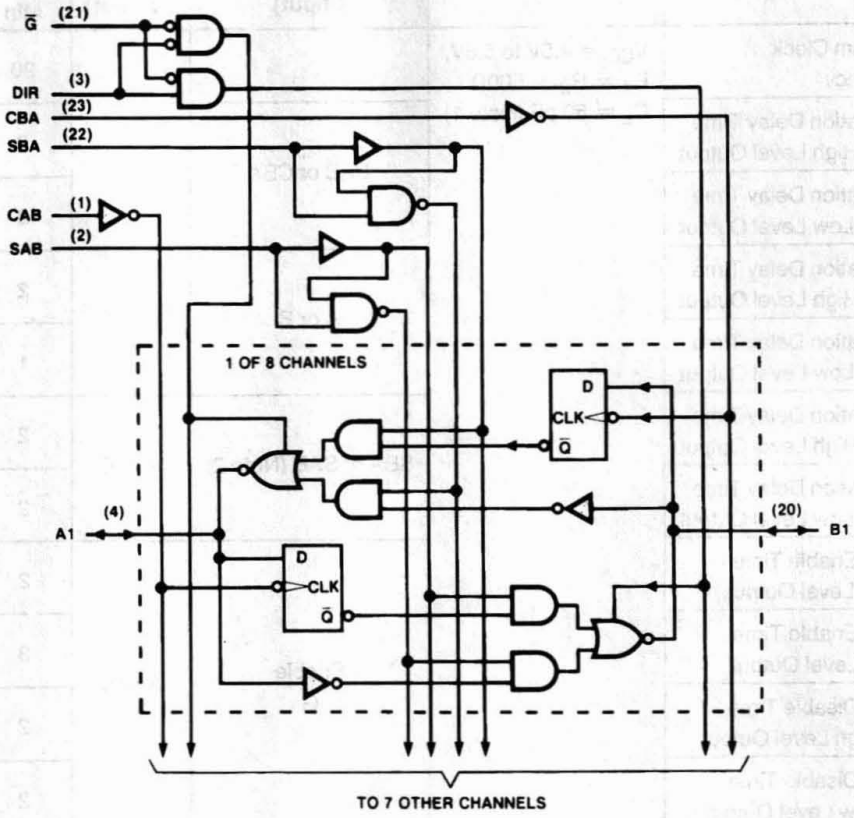
Inputs						Data I/O*		Operation or Function	
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A1 thru A8	B1 thru B8	'AS646	'AS648
H	X	H or L	H or L	X	X	Input	Input	Isolation, Hold Storage	Isolation, Hold Storage
	X	↑	↑	X	X			Store A and B Data	Store A and B Data
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus	Real $\overline{B}$ Data to A Bus
	L	X	H or L	X	H			Stored B Data to A Bus	Stored $\overline{B}$ Data to A Bus
L	H	X	X	L	X	Input	Output	Real Time A Data to B Bus	Real Time $\overline{A}$ Data to B Bus
	H	H or L	X	H	X			Stored A Data to B Bus	Stored $\overline{A}$ Data B Bus
X	X	↑	X	X	X	Input	Unspecified*	Store A, B Unspecified*	Store A, B Unspecified*
X	X	X	↑	X	X	Unspecified*	Input	Store B, A Unspecified*	Store B, A Unspecified*

H—high level; L—low level; X—irrelevant; ↑—low-to-high level transition

*The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

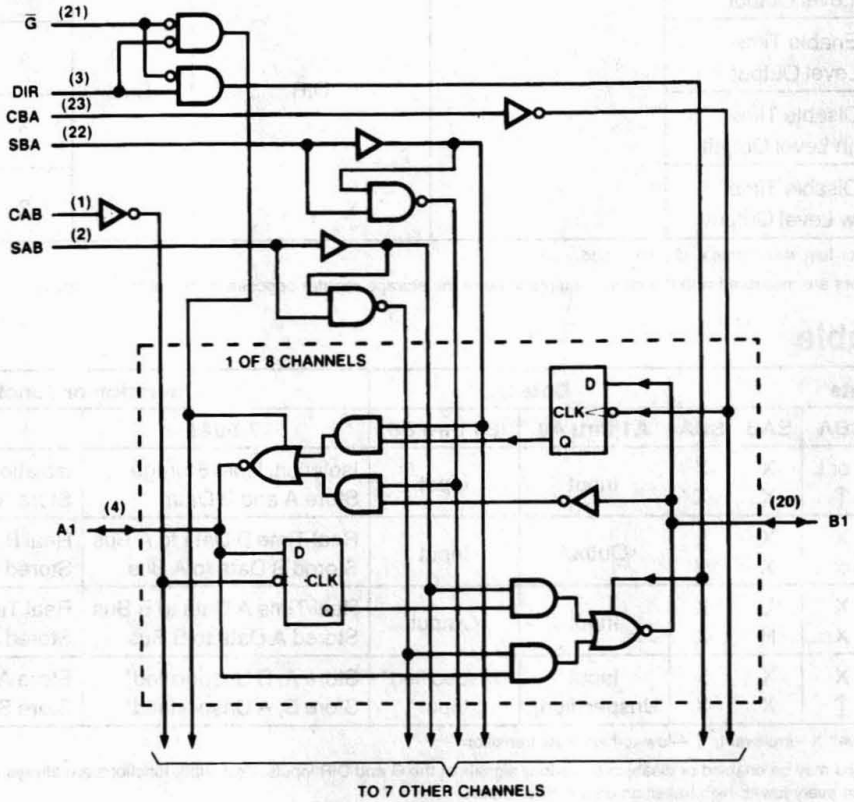
Block Diagram (positive logic)

'AS646



TL/F/6324–2

'AS648



TL/F/6324–5

National Semiconductor Corporation

DM74AS651/DM74AS652 Octal Bus Transceiver and Register

General Description

These devices incorporate an octal transceiver and an octal D-type register configured to enable transmission of data from bus to bus or internal register to bus.

These bus transceivers feature totem-pole TRI-STATE® outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these devices with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The registers in the AS651, 652 are edge-triggered D-type flip-flops. On the positive transition of the clock (CAB or CBA), the input data is stored.

The SAB and SBA control pins are provided to select whether real-time data or stored data is transferred. A low input level selects real-time data and a high level selects stored data. The select controls have a "make before break" configuration to eliminate a glitch which would normally occur in a typical multiplexer during the transition between stored and real-time data.

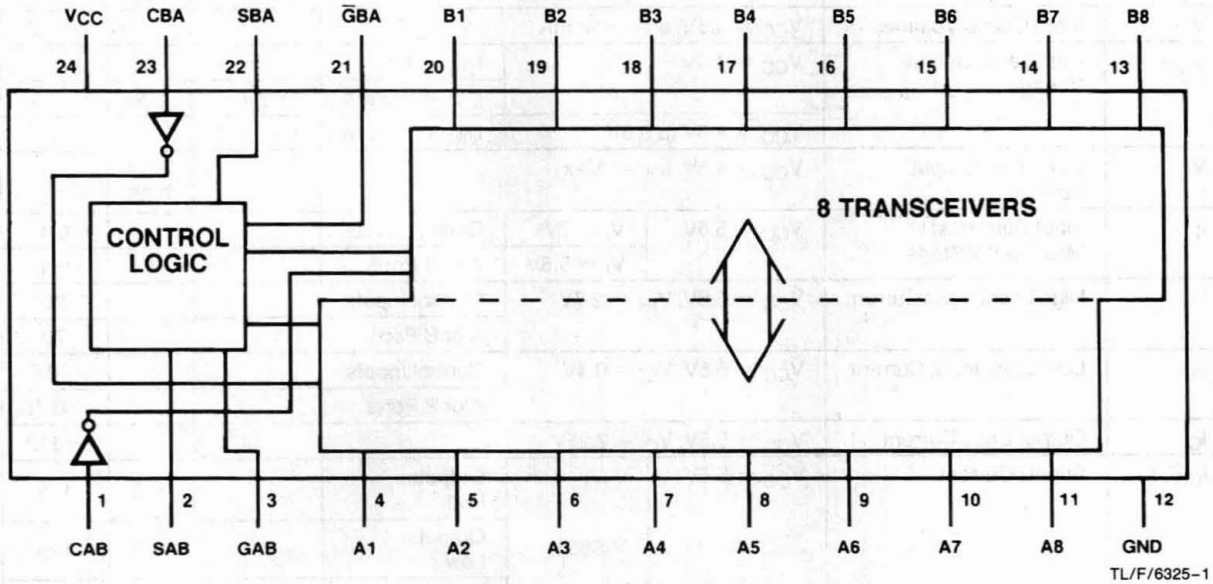
The Enable (GAB and $\overline{GBA}$) control pins provide four modes of operation; real-time data transfer from bus A to B, real-time data transfer from bus B to A, real-time bus A and/or B data transfer to internal storage, or internal stored data transfer to bus A and/or B.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- TRI-STATE® buffer-type outputs drive bus lines directly

Connection Diagram

Dual-In-Line Package



TL/F/6325–1

Order Number DM74AS651NT
See NS Package Number N24C*

*Contact your local NSC representative about surface mount (M) package availability.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	
Control Inputs	7V
I/O Ports	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−15	mA
I_{OL}	Low Level Output Current				48	mA
f_{CLK}	Clock Frequency		0		90	MHz
t_{WCLK}	Width of Enable Pulse	High	5			ns
		Low	6			
t_{SU}	Data Setup Time		6			ns
t_H	Data Hold Time		0			ns
T_A	Operating free Air Temperature		0		70	°C

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions			Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA					−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V		I_{OH} = Max	2			V
				I_{OH} = −3 mA	2.4	3.2		
		V_{CC} = 4.5V to 5.5V		I_{OH} = −2 mA	V_{CC} − 2			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = Max				0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V	V_I = 7V	Control Inputs			0.1	mA
			V_I = 5.5V	A or B Ports			0.1	
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V		Control Inputs			20	μA
				A or B Ports			70	
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V		Control Inputs			−0.5	mA
				A or B Ports			−0.75	
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V			−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	'AS651	Outputs High		110	185	mA
				Outputs Low		120	195	
				Outputs Disabled		130	195	
			'AS652	Outputs Low		120	195	
				Outputs High		130	211	
				Outputs Disabled		130	211	

'AS651 Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From	To	Min	Max	Units
f_{MAX}	Maximum Clock Frequency	V_{CC} = 4.5V to 5.5V $R_1 = R_2 = 500\Omega$ C_L = 50 pF			90		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output		CBA or CAB	A or B	2	8.5	ns
t_{PHL}	Propagation Delay Time High to Low Level Output				2	9	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		A or B	B or A	2	8	ns
t_{PHL}	Propagation Delay Time High to Low Level Output				1	7	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		SBA or SAB (Note 2)	A or B	2	11	ns
t_{PHL}	Propagation Delay Time High to Low Level Output				2	9	ns
t_{PZH}	Output Enable Time to High Level Output		Enable $\overline{G}$BA	A	2	10	ns
t_{PZL}	Output Enable Time to Low Level Output				3	16	ns
t_{PHZ}	Output Disable Time from High Level Output				2	9	ns
t_{PLZ}	Output Disable Time from Low Level Output				2	9	ns
t_{PZH}	Output Disable Time to High Level Output		Enable GAB	B	3	11	ns
t_{PZL}	Output Disable Time to Low Level Output				3	16	ns
t_{PHZ}	Output Disable Time from High Level Output				2	10	ns
t_{PLZ}	Output Disable Time from Low Level Output				2	11	ns

Note 1: See Section 1 for test waveforms and output load.

Note 2: These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

'AS652 Switching Characteristics over recommended operating free air temperature range (Note 1)

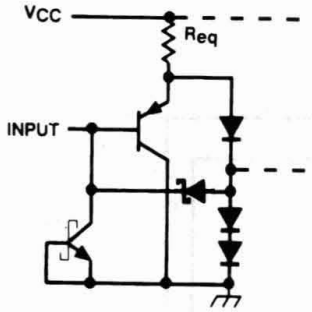
Symbol	Parameter	Conditions	From	To	Min	Max	Units
f_{MAX}	Maximum Clock Frequency	V_{CC} = 4.5V to 5.5V $R_1 = R_2 = 500\Omega$ C_L = 50 pF			90		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output		CBA or CAB	A or B	2	8.5	ns
t_{PHL}	Propagation Delay Time High to Low Level Output				2	9	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		A or B	B or A	2	9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output				1	7	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		SBA or SAB	A or B	2	11	ns
t_{PHL}	Propagation Delay Time High to Low Level Output				2	9	ns
t_{PZH}	Output Enable Time to High Level Output		Enable $\overline{G}$BA	A	2	10	ns
t_{PZL}	Output Enable Time to Low Level Output				3	16	ns
t_{PHZ}	Output Disable Time from High Level Output				2	9	ns
t_{PLZ}	Output Disable Time from Low Level Output				2	9	ns
t_{PZH}	Output Disable Time to High Level Output		Enable GAB	B	3	11	ns
t_{PZL}	Output Disable Time to Low Level Output				3	16	ns
t_{PHZ}	Output Disable Time from High Level Output				2	10	ns
t_{PLZ}	Output Disable Time from Low Level Output				2	11	ns

Note 1: See Section 1 for test waveforms and output load.

Note 2: These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

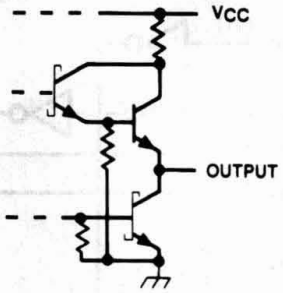
Schematics of Inputs and Outputs

Equivalent of All Other Inputs



TL/F/6325–4

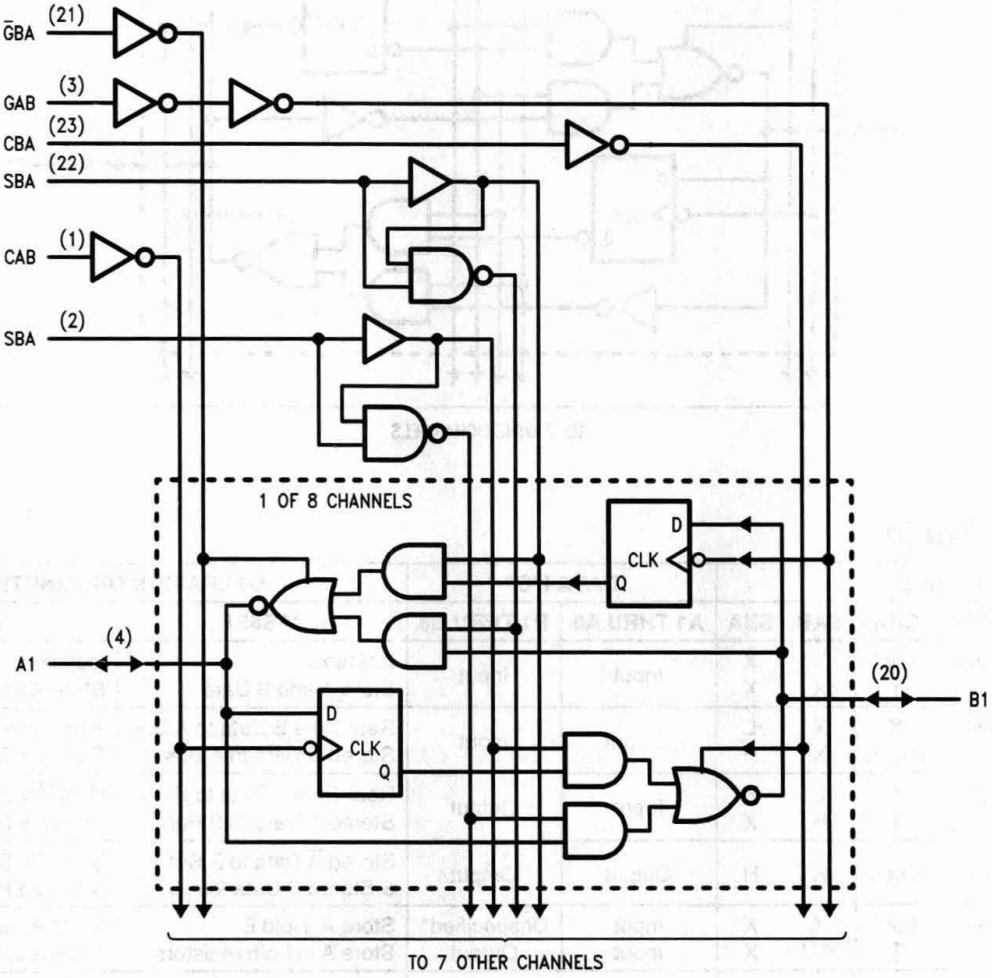
Typical of All 'AS651, 'AS652 Outputs



TL/F/6325–5

Block Diagram

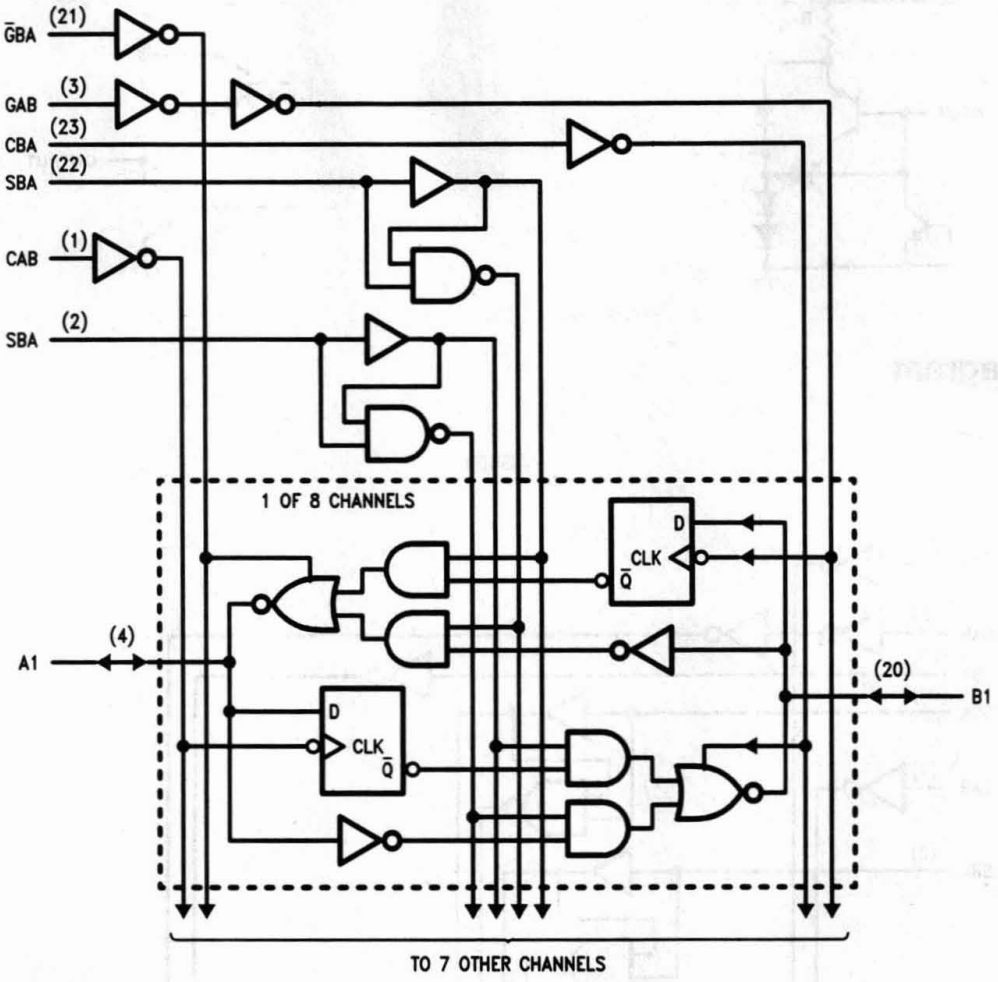
'AS651



TL/F/6325–2

Block Diagram (Continued)

'AS652



TL/F/6325–3

Function Table

INPUTS						DATA I/O*		OPERATION OR FUNCTION	
GAB	$\overline{GBA}$	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	'AS651	'AS652
L	H	H or L	H or L	X	X	Input	Input	Isolation	Isolation
L	H	↑	↑	X	X			Store A and B Data	Store A and B Data
L	L	X	X	X	L	Output	Input	Real Time $\overline{B}$ Data to A Bus	Real Time B Data to A Bus
L	L	X	H or L	X	H			Stored $\overline{B}$ Data to A Bus	Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real Time $\overline{A}$ Data to B Bus	Real Time A Data to B Bus
H	H	H or L	X	H	X			Stored $\overline{A}$ Data to B Bus	Stored A Data B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ Data to B Bus & Stored $\overline{B}$ Data to A Bus	Stored A Data to B Bus & Stored B Data to A Bus
X	H	↑	H or L	X	X	Input	Unspecified*	Store A, Hold B	Store A, Hold B
H	H	↑	↑	X(1)	X	Input	Output	Store A in both registers	Store A in both registers
L	X	H or L	↑	X	X	Unspecified*	Input	Hold A, Store B	Hold A, Store B
L	L	↑	↑	X	X(1)	Output	Input	Store B in both registers	Store B in both registers

Note 1: If the select control is low, the clocks can occur simultaneously. If the select control is high, the clocks must be staggered in order to load both registers.

H—high level L—low level X—irrelevant ↑—low-to-high transition

*The data output functions may be enabled or disabled by various signals at the GAB and $\overline{GBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

National Semiconductor Corporation

DM74AS804B Hex 2-Input NAND Drivers

General Description

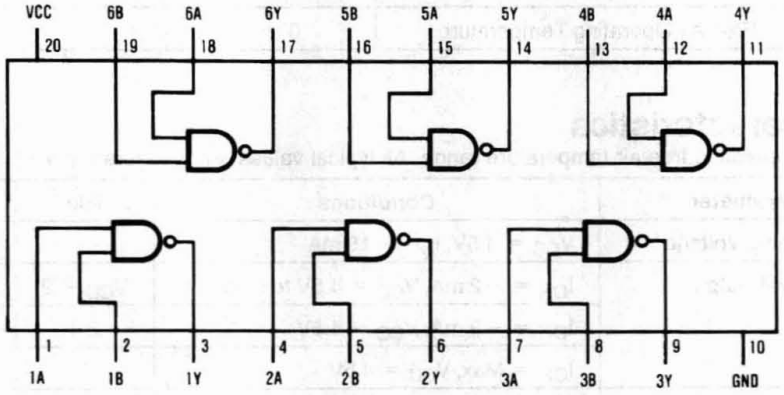
These devices contain six independent drivers, each of which performs the logic NAND function. Each driver has increased output drive capability to allow the driving of high capacitive loads.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with advanced low power Schottky TTL counterpart

Connection Diagram

Dual-In-Line Package



TL/F/6326–1

Order Number DM74AS804BN
See NS Package Number N20A*

Function Table

$Y = \overline{AB}$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level

L = Low Logic Level

*Contact your local NSC representative about surface mount (M) package availability.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−48	mA
I_{OL}	Low Level Output Current			48	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2 mA, V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
		I_{OH} = −3 mA, V_{CC} = 4.5V		2.4			
		I_{OH} = Max, V_{CC} = 4.5V		2			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = Max V_{IH} = 2V			0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−50	−135	−200	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		3.5	5	mA
			Outputs Low		16	27	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	1	4	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		1	4	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM74AS805B Hex 2-Input NOR Drivers

General Description

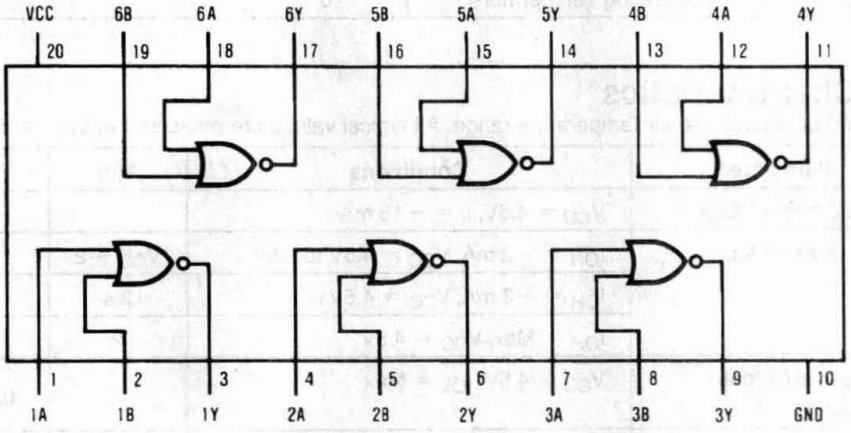
These devices contain six independent drivers, each of which performs the logic NOR function. Each driver has increased output drive capability to allow the driving of high capacitive loads.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with advanced low power Schottky TTL counterpart

Connection Diagram

Dual-In-Line Package



TL/F/6327–1

Order Number DM74AS805BWM or DM74AS805BN
See NS Package Number M20B or N20A

Function Table

$$Y = \overline{A + B}$$

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−48	mA
I_{OL}	Low Level Output Current			48	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2 mA, V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
		I_{OH} = −3 mA, V_{CC} = 4.5V		2.4			
		I_{OH} = Max, V_{CC} = 4.5V		2			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = Max			0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−50	−135	−200	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		6.5	10	mA
			Outputs Low		18	32	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	1	4.3	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		1	4.3	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM74AS808B Hex 2-Input AND Driver

General Description

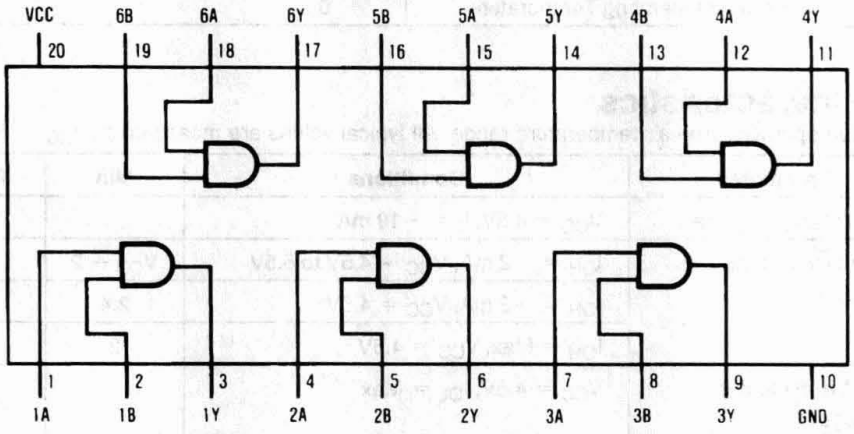
This device contains six independent drivers, each of which performs the logic AND function. Each driver has increased output drive capability to allow the driving of high capacitive loads.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with advanced low power Schottky TTL counterpart

Connection Diagram

Dual-In-Line Package



TL/F/6328–1

Order Number DM74AS808BWM or DM74AS808BN
See NS Package Number M20B or N20A

Function Table

Y = AB

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = High Logic Level

L = Low Logic Level

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−48	mA
I_{OL}	Low Level Output Current			48	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2 mA, V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
		I_{OH} = −3 mA, V_{CC} = 4.5V		2.4			
		I_{OH} = Max, V_{CC} = 4.5V		2			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = Max			0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−50	−135	−200	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		8	13	mA
			Outputs Low		20	33	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	1	6	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		1	6	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM74AS810 Quad 2-Input Exclusive-NOR Gate

General Description

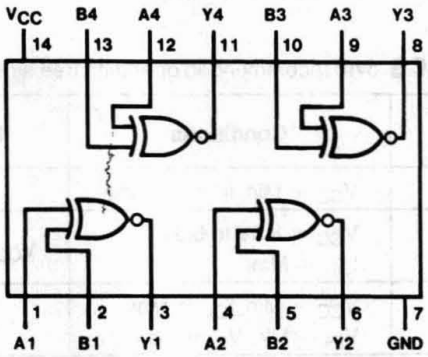
This device contains four independent gates each of which performs the logic exclusive-NOR function.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with advanced low power Schottky TTL counterpart
- Improved AC performance over advanced low power Schottky counterparts
- PNP input design reduces input loading

Connection Diagram

Dual-In-Line Package



TL/F/6724–1

Order Number DM74AS810N
See NS Package Number N14A*

Function Table

$$\overline{Y} = A \oplus B$$

Inputs		Output
A	B	$\overline{Y}$
L	L	H
L	H	L
H	L	L
H	H	H

H = High Logic Level, L = Low Logic Level

*Contact your local NSC representative about surface mount (M) package availability.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−2	mA
I_{OL}	Low Level Output Current			20	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V I_{OH} = Max	V_{CC} − 2V	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max		0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V			−0.5	mA
I_O	Output Drive Current	V_{CC} = Max, V_O = 2.25V	−30		−112	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max (Note 3)		18	26	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max (Note 2)		25	36	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: I_{CCL} is measured with all outputs open, one input of each gate at 4.5V, and the other inputs grounded.

Note 3: I_{CCH} is measured with all outputs open and all inputs at 4.5V.

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	Other Input Low V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	1	6.5	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		1	6.5	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Other Input High V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	2	7	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		2	7	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM74AS811 Quad 2-Input Exclusive-NOR Gates with Open-Collector Outputs

General Description

This device contains four independent gates, each of which performs the logic exclusive-NOR function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC\,(Min)} - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC\,(Max)} - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

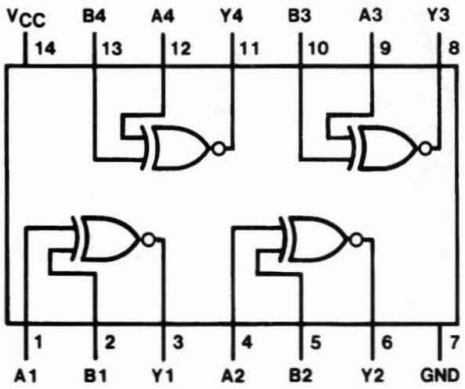
$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with advanced low power Schottky TTL counterpart
- Improved AC performance over advanced low power Schottky counterparts
- Open collector outputs for wired AND cascading
- PNP input design reduces input loading

Connection Diagram

Dual-In-Line Package



TL/F/6725–1

Order Number DM74ALS811N
See NS Package Number N14A*

Function Table

$$\overline{Y} = A \oplus B$$

Inputs		Output $\overline{Y}$
A	B	
L	L	H
L	H	L
H	L	L
H	H	H

H = High Logic Level

L = Low Logic Level

*Contact your local NSC representative about surface mount (M) package availability.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Off State Output Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
V_{OH}	High Level Output Voltage			5.5	V
I_{OL}	Low Level Output Current			20	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.2	V
I_{CEX}	High Level Output Current Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max, V_{IH} = Min			100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max		0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			20	μA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max (Note 3)		19.6	28	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max (Note 2)		25	36	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: I_{CCL} is measured with all outputs open, one input of each at 4.5V, and the other inputs grounded.

Note 3: I_{CCH} is measured with all outputs open and all inputs at 4.5V.

Switching Characteristics over recommended operating free air temperature range (Note 4)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	Other Input Low V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	5	45	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		1	8.5	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Other Input High V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	5	45	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		2	9	ns

Note 4: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM74AS832B Hex 2-Input OR Drivers

General Description

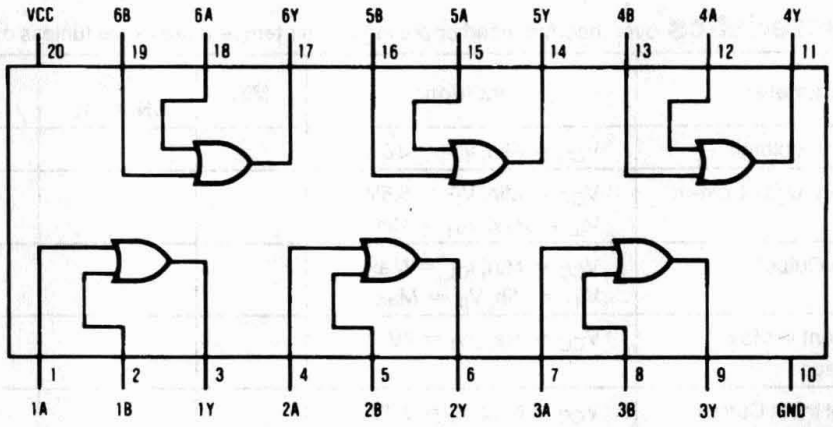
These devices contain six independent drivers, each of which performs the logic OR function. Each driver has increased output drive capability to allow the driving of high capacitive loads.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin for pin compatible with Schottky and low power Schottky TTL counterpart
- Improved AC performance over Schottky and low power Schottky counterparts

Connection Diagram

Dual-In-Line Package



TL/F/6329–1

Order Number DM74AS832BWM or DM74AS832BN
See NS Package Number M20B or N20A

Function Table

$Y = A + B$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

H = High Logic Level

L = Low Logic Level

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−48	mA
I_{OL}	Low Level Output Current			48	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2 mA, V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
		I_{OH} = −3 mA, V_{CC} = 4.5V		2.4			
		I_{OH} = Max, V_{CC} = 4.5V		2			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = Max			0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−50	−135	−200	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		11	17	mA
			Outputs Low		22	36	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	1	6.3	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		1	6.3	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM74AS873 Dual 4-Bit D-Type Transparent Latches with TRI-STATE® Outputs

General Description

These dual 4-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the AS873 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was set up.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are off.

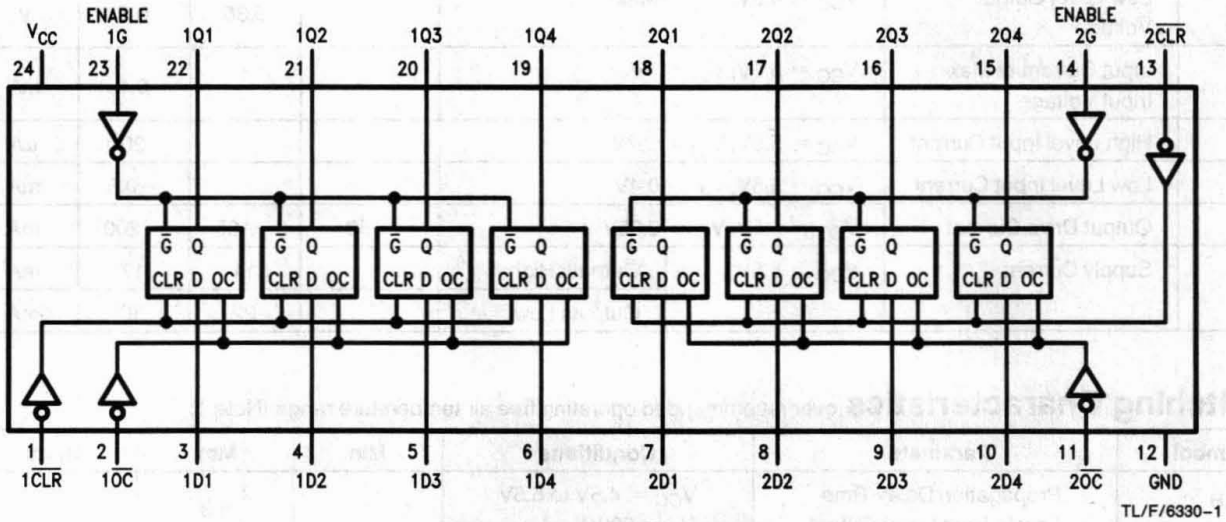
The pinout is arranged to ease printed circuit board layout. All data inputs are on one side of the package while all outputs are on the other side.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- TRI-STATE buffer-type outputs drive bus lines directly
- Space Saving 300 Mil Wide Package
- Bus structured pinout

Connection Diagram

Dual-In-Line Package



TL/F/6330–1

Order Number DM74AS873NT
See NS Package Number N24C

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Voltage Applied to Disabled Output	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−15	mA
I_{OL}	Low Level Output Current				48	mA
t_W	Pulse Width	Enable High	5.5			ns
		Clear Low	3.5			
t_{SU}	Data Setup Time		2↓			ns
t_H	Data Hold Time		3↓			ns
T_A	Free Air Operating Temperature		0		70	°C

The (↓) arrow indicates the negative edge of the enable is used for reference.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, V_{IL} = Max, I_{OH} = Max		2.4	3.3		V
		I_{OH} = −2 mA, V_{CC} = 4.5V to 5.5V		V_{CC} −2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, V_{IH} = 2V, I_{OL} = Max			0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V, V_O = 2.7V				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V, V_O = 0.4V				−50	μA
I_{CC}	Supply Current	V_{CC} = 5.5V, Outputs Open	Outputs High		68	110	mA
			Outputs Low		67	109	mA
			Outputs Disabled		80	129	mA

Switching Characteristics

over recommended operating free air temperature range (Note 1). All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions	From	To	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	Data	Any Q	3	6.5	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Data	Any Q	3	6	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		Enable	Any Q	6	11.5	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Enable	Any Q	4	7.5	ns
t_{PZH}	Output Enable Time to High Level Output		Output Control	Any Q	2	6.5	ns
t_{PZL}	Output Enable Time to Low Level Output		Output Control	Any Q	4	9.5	ns
t_{PHZ}	Output Disable Time from High Level Output		Output Control	Any Q	2	6.5	ns
t_{PLZ}	Output Disable Time from Low Level Output		Output Control	Any Q	2	7.5	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Clear	Any Q	3	8.5	ns

Note 1: See Section 1 for test waveforms and output load.

Function Table

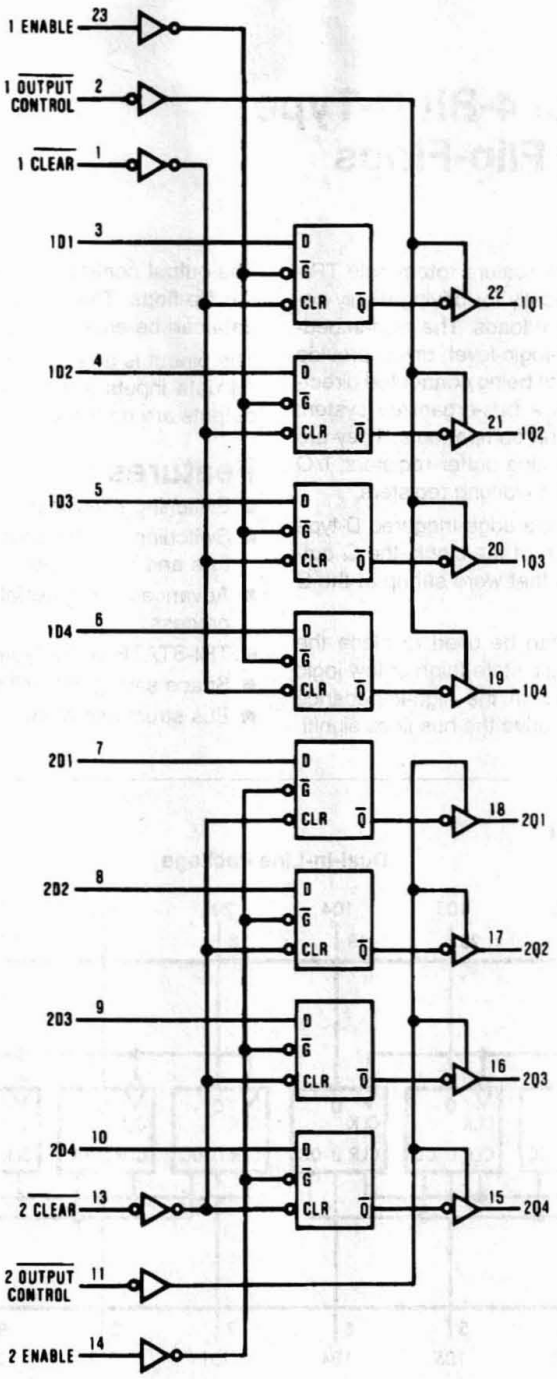
Inputs				Output
$\overline{CLR}$	D	EN	$\overline{OC}$	Q
X	X	X	H	Z
L	X	X	L	L
H	H	H	L	H
H	L	H	L	L
H	X	L	L	Q_0

L = Low State, H = High State, X = Don't Care

Z = High Impedance State

Q_0 = Previous Condition of Q

Logic Diagram



TL/F/6330–2

National Semiconductor Corporation

DM74AS874 Dual 4-Bit D-Type Edge-Triggered Flip-Flops

General Description

These dual 4-bit inverting registers feature totem-pole TRI-STATE® outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the AS874 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

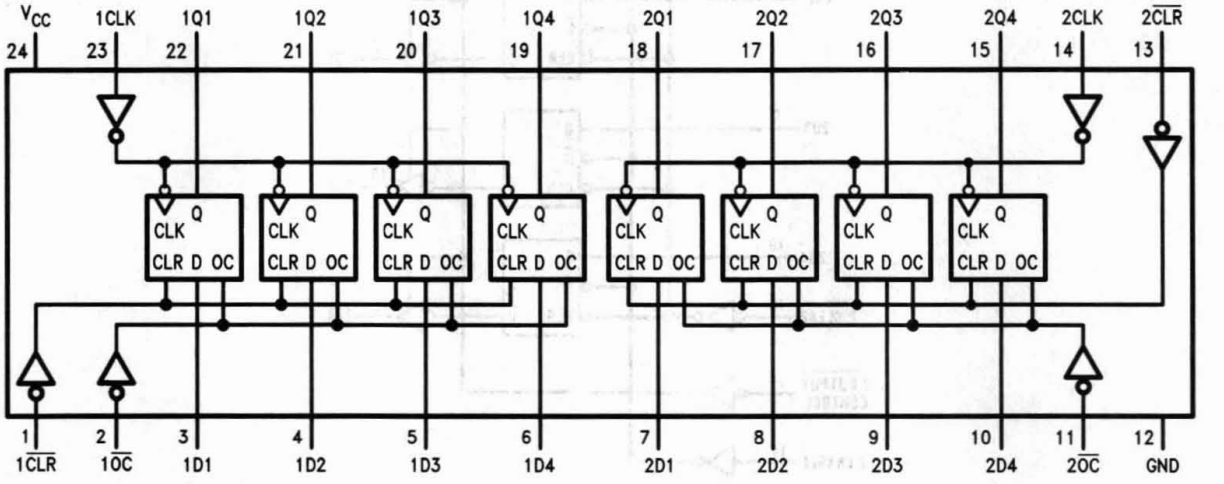
The pinout is arranged to ease printed circuit board layout. All data inputs are on one side of the package, while all outputs are on the other side.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- TRI-STATE buffer-type outputs drive bus lines directly
- Space saving 300 mil wide package
- Bus structured pinout

Connection Diagram

Dual-In-Line Package



TL/F/6331–1

Order Number DM74AS874NT
See NS Package Number N24C*

*Contact your local NSC representative about surface mount (M) package availability.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Voltage Applied to Disabled Output	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−15	mA
I_{OL}	Low Level Output Current				48	mA
f_{CLK}	Clock Frequency		0		80	MHz
t_{WCLK}	Width of Clock Pulse	High	3			ns
		Low	6			
t_{WCLR}	Width of Clear Pulse	Low	2			ns
t_{SU}	Setup Time	Data	4↑			ns
		Clear Inactive	5↑			
t_H	Data Hold Time		1↑			ns
T_A	Free Air Operating Temperature		0		70	°C

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, V_{IL} = V_{IL} Max, I_{OH} = Max		2.4	3.3		V
		I_{OH} = −2 mA, V_{CC} = 4.5V to 5.5V		V_{CC} − 2			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, V_{IH} = 2V, I_{OL} = Max			0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V, V_O = 2.7V,				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V, V_O = 0.4V				−50	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		82	133	mA
			Outputs Low		92	149	
			Outputs Disabled		100	160	

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From	To	Min	Max	Units
f_{MAX}	Maximum Clock Frequency	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF			80		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output		Clock	Any Q	3	8.5	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Clock	Any Q	4	10.5	ns
t_{PZH}	Output Enable Time to High Level Output		Output Control	Any Q	2	7	ns
t_{PZL}	Output Enable Time to Low Level Output		Output Control	Any Q	3	10.5	ns
t_{PHZ}	Output Disable Time from High Level Output		Output Control	Any Q	2	6	ns
t_{PLZ}	Output Disable Time from Low Level Output		Output Control	Any Q	2	7.5	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Clear	Any Q	4	11.5	ns

Note 1: See Section 1 for test waveforms and output load.

Function Table

Inputs				Output
$\overline{CLR}$	D	CLK	$\overline{OC}$	Q
X	X	X	H	Z
L	X	X	L	L
H	H	↑	L	H
H	L	↑	L	L
H	X	L	L	Q_0

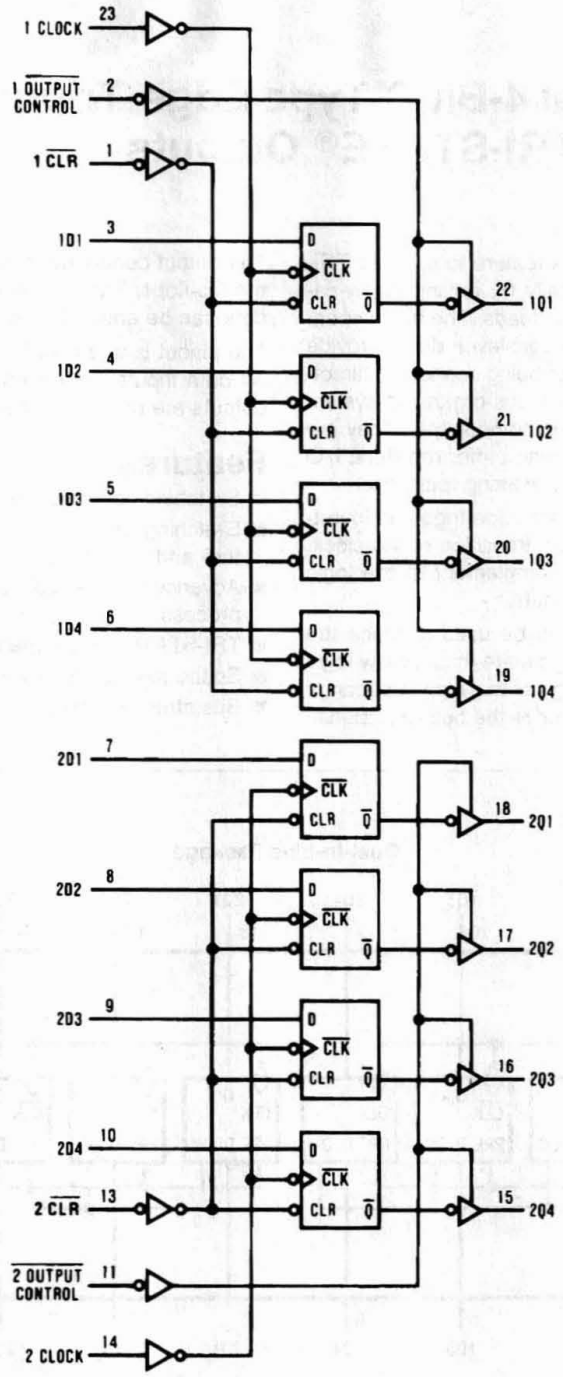
L = Low State, H = High State, X = Don't Care

↑ = Positive Edge Transition

Z = High Impedance State

Q_0 = Previous Condition of Q

Logic Diagram



TL/F/6331–2

National Semiconductor Corporation

DM74AS876 Dual 4-Bit D-Type Edge-Triggered Flip-Flops with TRI-STATE® Outputs

General Description

These inverting dual 4-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the AS876 are edge-triggered inverting D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the complement of the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

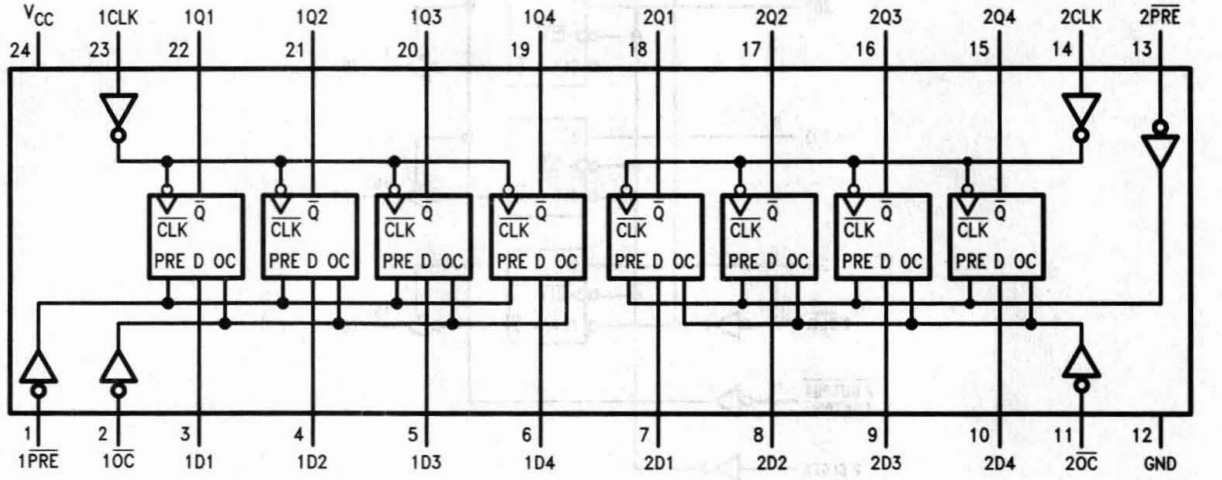
The pinout is arranged to ease printed circuit board layout. All data inputs are on one side of the package, while all outputs are on the other side.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- TRI-STATE buffer-type outputs drive bus lines directly
- Space saving 300 mil wide package
- Bus structured pinout

Connection Diagram

Dual-In-Line Package



TL/F/6332–1

Order Number DM74AS876NT
See NS Package Number N24C*

*Contact your local NSC representative about surface mount (M) package availability.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Voltage Applied to Disabled Output	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−15	mA
I_{OL}	Low Level Output Current				48	mA
f_{CLK}	Clock Frequency		0		80	MHz
$t_{W(CLK)}$	Width of Clock Pulse	High	3			ns
		Low	6			
$t_{W(PRE)}$	Width of Preset Pulse	Low	2			ns
t_{SU}	Data	Data	4↑			ns
		Preset Inactive	5↑			
t_H	Data Hold Time		1↑			ns
T_A	Free Air Operating Temperature		0		70	°C

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

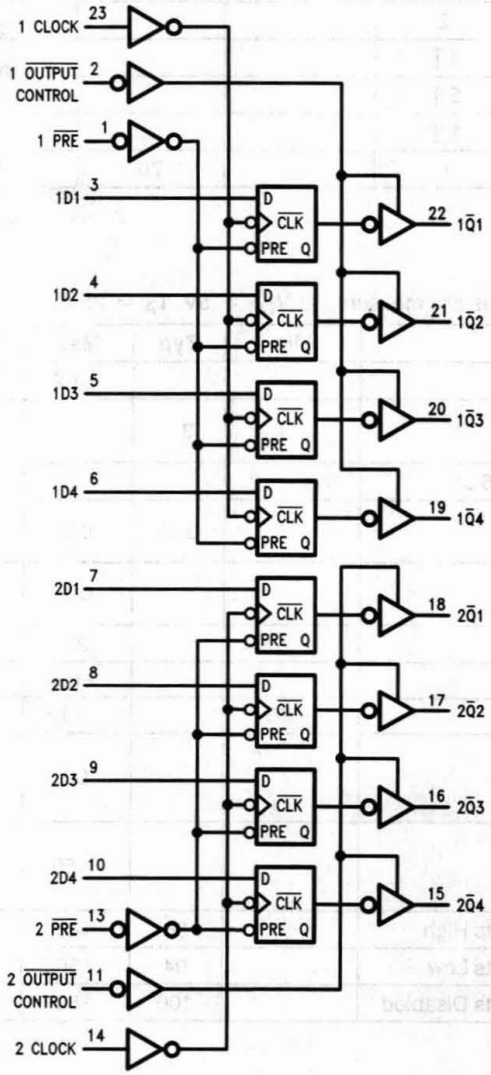
Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, V_{IL} = V_{IL} Max, I_{OH} = Max		2.4	3.3		V
		I_{OH} = −2 mA, V_{CC} = 4.5V to 5.5V		V_{CC} − 2			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, V_{IH} = 2V, I_{OL} = Max			0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V, V_O = 2.7V,				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V, V_O = 0.4V				−50	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		88	142	mA
			Outputs Low		94	150	
			Outputs Disabled		100	160	

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From	To	Min	Max	Units
f_{MAX}	Maximum Clock Frequency	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF			80		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output		Clock	Any $\overline{Q}$	3	8.5	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Clock	Any $\overline{Q}$	4	10.5	ns
t_{PZH}	Output Enable Time to High Level Output		Output Control	Any $\overline{Q}$	2	7	ns
t_{PZL}	Output Enable Time to Low Level Output		Output Control	Any $\overline{Q}$	3	10.5	ns
t_{PHZ}	Output Disable Time from High Level Output		Output Control	Any $\overline{Q}$	2	6	ns
t_{PLZ}	Output Disable Time from Low Level Output		Output Control	Any $\overline{Q}$	2	6	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Preset	Any $\overline{Q}$	4	10	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6332–2

Function Table

Inputs				Output
$\overline{PRE}$	D	CLK	$\overline{OC}$	$\overline{Q}$
X	X	X	H	Z
L	X	X	L	L
H	H	↑	L	L
H	L	↑	L	H
H	X	L	L	$\overline{Q}_0$

L = Low State, H = High State, X = Don't Care

↑ = Positive Edge Transition

Z = High Impedance State

$\overline{Q}_0$ = Previous Condition of $\overline{Q}$

National Semiconductor Corporation

DM74AS878 Dual 4-Bit D-Type Edge-Triggered Flip-Flops with Synchronous Clear

General Description

These dual 4-bit registers feature totem-pole TRI-STATE® outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the AS878 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

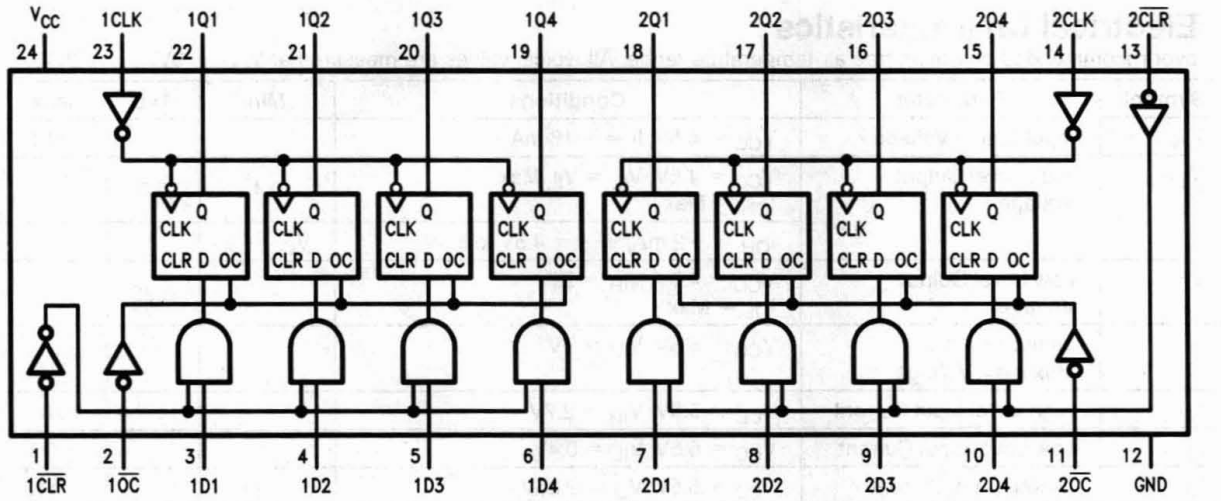
The pinout is arranged to ease printed circuit board layout. All data inputs are on one side of the package while all outputs are on the other side.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- TRI-STATE buffer-type outputs drive bus lines directly
- Synchronous clear
- Bus structured pinout

Connection Diagram

Dual-In-Line Package



TL/F/6333–1

Order Number DM74AS878N
See NS Package Number N20A*

*Contact your local NSC representative about surface mount (M) package availability.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Voltage Applied to Disabled Output	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−15	mA
I_{OL}	Low Level Output Current				48	mA
f_{CLK}	Clock Frequency		0		80	MHz
t_{WCLK}	Width of Enable Pulse	High	4			ns
		Low	6			
t_{SU}	Data Setup Time	Data	4↑			ns
		$\overline{CLR}$	6↑			
t_H	Data Hold Time	Data	2↑			ns
		$\overline{CLR}$	0↑			
T_A	Free Air Operating Temperature		0		70	ns

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

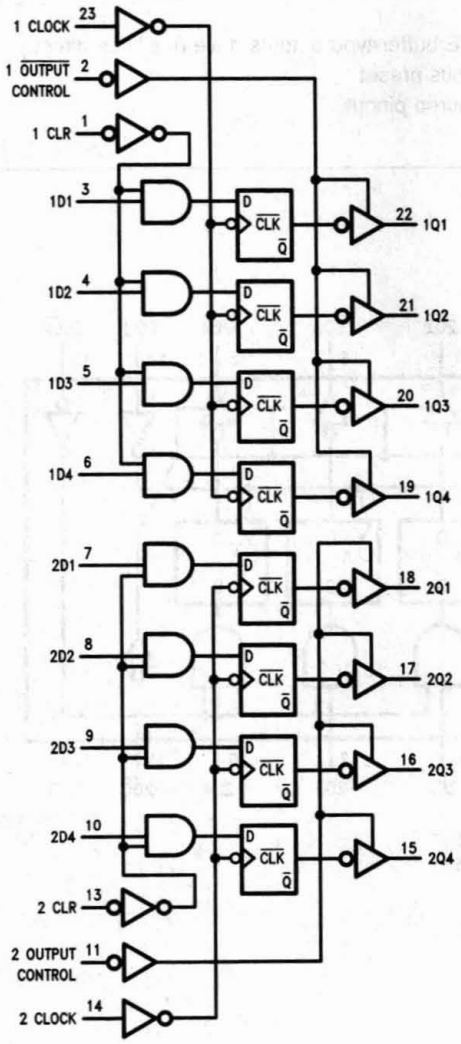
Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, V_{IL} = V_{IL} Max, I_{OH} = Max		2.4	3.3		V
		I_{OH} = −2 mA, V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, V_{IH} = 2V, I_{OL} = Max			0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V, V_O = 2.7V				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V, V_O = 0.4V				−50	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		82	132	mA
			Outputs Low		96	155	
			Outputs Disabled		100	160	

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From	To	DM74AS878		Units
					Min	Max	
f_{MAX}	Maximum Clock Frequency	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF			80		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output		Clock	Any Q	3	8.5	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Clock	Any Q	4	10.5	ns
t_{PZH}	Output Enable Time to High Level Output		Output Control	Any Q	2	7	ns
t_{PZL}	Output Enable Time to Low Level Output		Output Control	Any Q	3	10.5	ns
t_{PHZ}	Output Disable Time from High Level Output		Output Control	Any Q	2	6	ns
t_{PLZ}	Output Disable Time from Low Level Output		Output Control	Any Q	2	6	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



TL/F/6333–2

Function Table

Inputs				Output
$\overline{CLR}$	D	CLK	$\overline{OC}$	Q
X	X	X	H	Z
L	X	↑	L	L
H	H	↑	L	H
H	L	↑	L	L
H	X	L	L	Q_0

L = Low State, H = High State, X = Don't Care

↑ = Positive Edge Transition

Z = High Impedance State

Q_0 = Previous Condition of Q

National Semiconductor Corporation

DM74AS879 Dual 4-Bit D-Type Edge-Triggered Flip-Flops with TRI-STATE® Outputs and Synchronous Clear

General Description

These inverting dual 4-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the AS879 are edge-triggered inverting D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the complement of the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

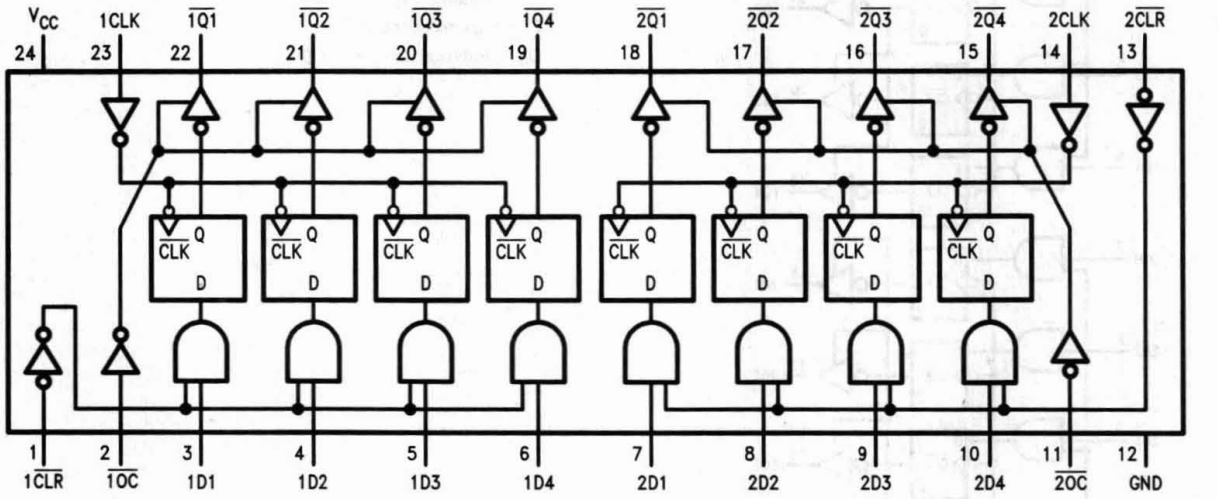
The pinout is arranged to ease printed circuit board layout. All data inputs are on one side of the package while all outputs are on the other side.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- TRI-STATE buffer-type outputs drive bus lines directly
- Synchronous preset
- Bus structured pinout

Connection Diagram

Dual-In-Line Package



TL/F/6334–1

Order Number DM74AS879N
See NS Package Number N20A*

*Contact your local NSC representative about surface mount (M) package availability.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Voltage Applied to Disabled Output	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−15	mA
I_{OL}	Low Level Output Current				48	mA
f_{CLK}	Clock Frequency		0		80	MHz
t_{WCLK}	Width of Clock Pulse	High	4			ns
		Low	6			
t_{SU}	Data Setup Time	Data	4↑			ns
		$\overline{CLR}$	6↑			
t_H	Data Hold Time	Data	2↑			ns
		$\overline{CLR}$	0↑			
T_A	Free Air Operating Temperature		0		70	°C

The (↑) arrow indicates the positive edge of the clock is used for reference.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

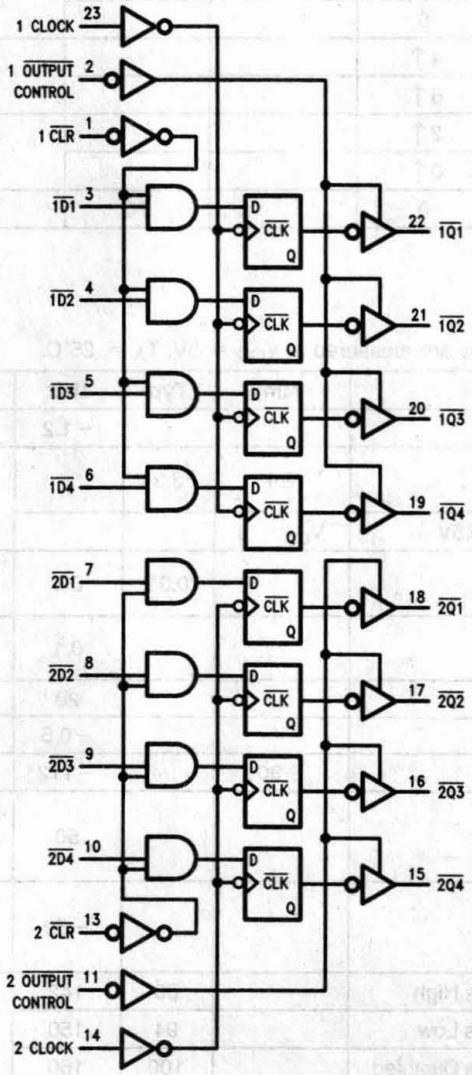
Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, V_{IL} = Max, I_{OH} = Max		2.4	3.3		V
		I_{OH} = −2 mA, V_{CC} = 4.5V to 5.5V		V_{CC} − 2			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, V_{IH} = 2V, I_{OL} = Max			0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V, V_O = 2.7V				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V, V_O = 0.4V				−50	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		88	142	mA
			Outputs Low		94	150	
			Outputs Disabled		100	160	

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From	To	Min	Max	Units
f_{MAX}	Maximum Clock Frequency	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF			80		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output		Clock	Any $\overline{Q}$	3	8.5	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Clock	Any $\overline{Q}$	4	10.5	ns
t_{PZH}	Output Enable Time to High Level Output		Output Control	Any $\overline{Q}$	2	7	ns
t_{PZL}	Output Enable Time to Low Level Output		Output Control	Any $\overline{Q}$	3	10.5	ns
t_{PHZ}	Output Disable Time from High Level Output		Output Control	Any $\overline{Q}$	2	6	ns
t_{PLZ}	Output Disable Time from Low Level Output		Output Control	Any $\overline{Q}$	2	6	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



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Function Table

Inputs				Output
$\overline{CLR}$	D	Clock	$\overline{OC}$	$\overline{Q}$
X	X	X	H	Z
L	X	↑	L	H
H	H	↑	L	L
H	L	↑	L	H
H	X	L	L	$\overline{Q}_0$

L = Low State, H = High State, X = Don't Care

↑ = Positive Edge Transition

Z = High Impedance State

$\overline{Q}_0$ = Previous Condition of $\overline{Q}$

National Semiconductor Corporation

DM74AS880 Dual 4-Bit D-Type Transparent Latches with TRI-STATE® Outputs

General Description

These dual 4-bit inverting registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight inverting latches of the AS880 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the complement of the data (D) inputs. When the enable is taken low the output will be latched at the complement of the level of the data that was set up.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are off.

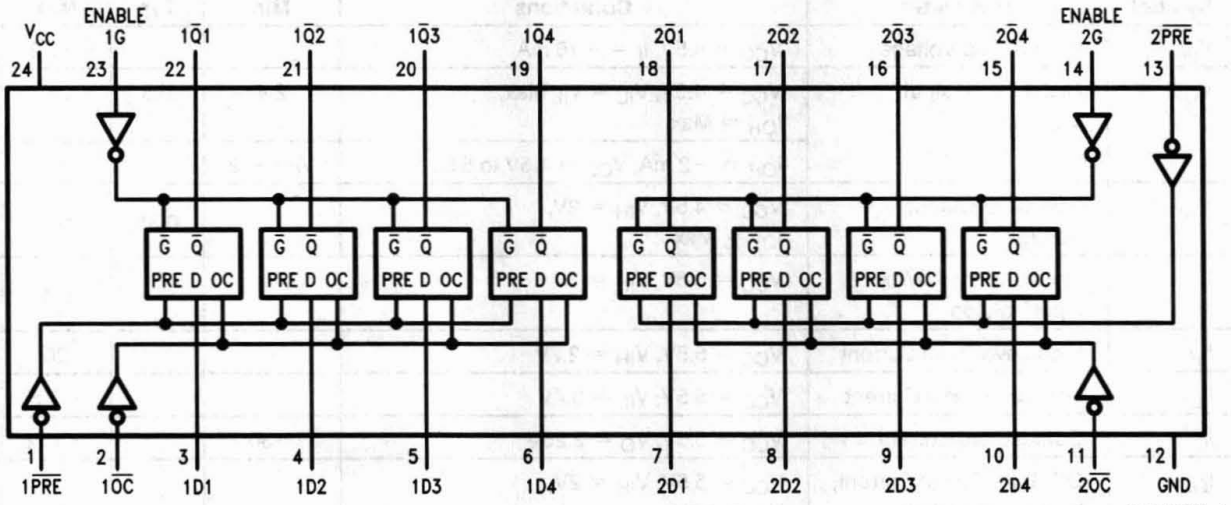
The pinout is arranged to ease printed circuit board layout. All data inputs are on one side of the package while all outputs are on the other side.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- TRI-STATE buffer-type outputs drive bus lines directly
- Space saving 300 mil wide package
- Bus structured pinout

Connection Diagram

Dual-In-Line Package



TL/F/6335–1

Order Number DM74AS880NT
See NS Package Number N24C*

*Contact your local NSC representative about surface mount (M) package availability.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Voltage Applied to Disabled Output	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−15	mA
I_{OL}	Low Level Output Current				48	mA
t_W	Pulse Width	Enable	2.5			ns
		Preset Low	4			ns
t_{SU}	Data Setup Time		2↓			ns
t_H	Data Hold Time		1↓			ns
T_A	Free Air Operating Temperature		0		70	°C

The (↓) arrow indicates the negative edge of the enable is used for reference.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, V_{IL} = V_{IL} Max, I_{OH} = Max		2.4	3.3		V
		I_{OH} = −2 mA, V_{CC} = 4.5V to 5.5V		V_{CC} − 2			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, V_{IH} = 2V, I_{OL} = Max			0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V, V_O = 2.7V				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V, V_{IH} = 2V, V_O = 0.4V				−50	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		73	118	mA
			Outputs Low		76	122	
			Outputs Disabled		86	137	

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From	To	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	Data	Any $\overline{Q}$	4	9.5	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Data	Any $\overline{Q}$	4	8.5	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		Enable	Any $\overline{Q}$	6	11.5	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Enable	Any $\overline{Q}$	4	8	ns
t_{PZH}	Output Enable Time to High Level Output		Output Control	Any $\overline{Q}$	2	7.5	ns
t_{PZL}	Output Enable Time to Low Level Output		Output Control	Any $\overline{Q}$	4	10	ns
t_{PHZ}	Output Disable Time from High Level Output		Output Control	Any $\overline{Q}$	2	6.5	ns
t_{PLZ}	Output Disable Time from Low Level Output		Output Control	Any $\overline{Q}$	2	8	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		Preset	Any $\overline{Q}$	4	10	ns

Note 1: See Section 1 for test waveforms and output load.

Function Table

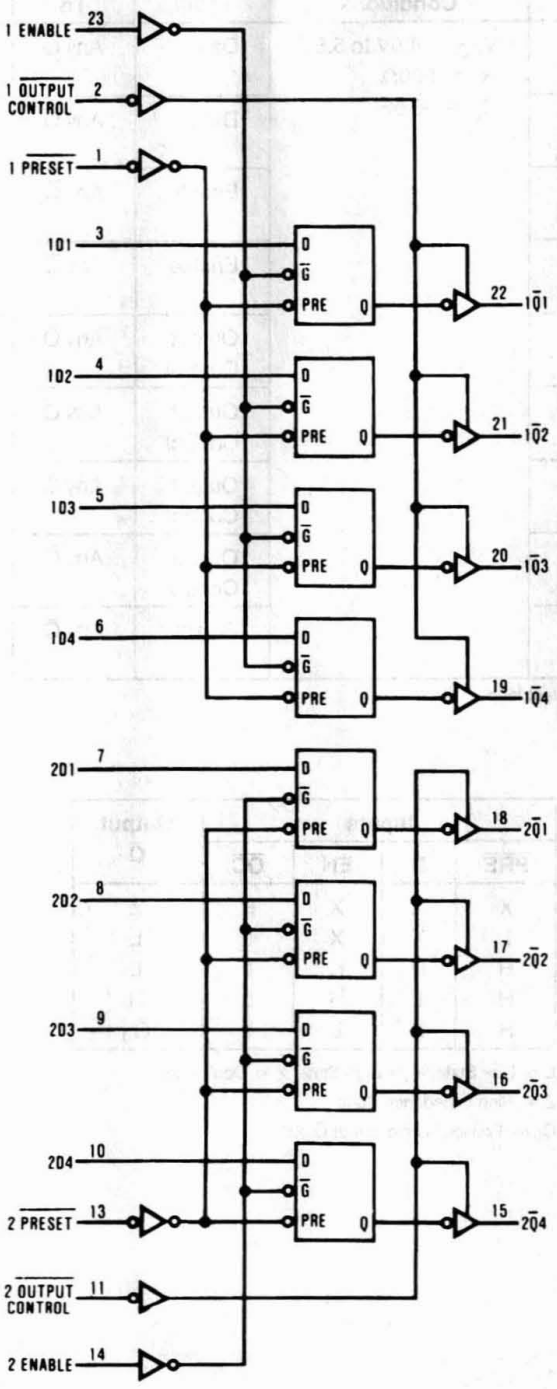
Inputs				Output
$\overline{PRE}$	D	EN	$\overline{OC}$	$\overline{Q}$
X	X	X	H	Z
L	X	X	L	L
H	H	H	L	L
H	L	H	L	H
H	X	L	L	$\overline{Q}_0$

L = Low State, H = High State, X = Don't Care

Z = High Impedance State

$\overline{Q}_0$ = Previous Condition of $\overline{Q}$

Logic Diagram



TL/F/6335–2

National Semiconductor Corporation

DM74AS881B 4-Bit Arithmetic Logic Unit/Function Generator

General Description

The DM74AS881B is an arithmetic logic unit (ALU)/function generator that has a complexity of 77 equivalent gates, respectively, on a monolithic chip. These circuits perform 16 binary arithmetic operations on two 4-bit words, as shown in Tables I and II. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade outputs (pins 15 and 17) for the four bits in the package. When used in conjunction with the DM74AS882 full carry look-ahead circuits, high speed arithmetic operations can be performed. The typical addition times shown previously illustrate the little additional time required for addition of longer words when full carry look-ahead is employed. The method of cascading 'AS882 circuits with these ALUs to provide multi-level full carry look-ahead is illustrated under "signal designations."

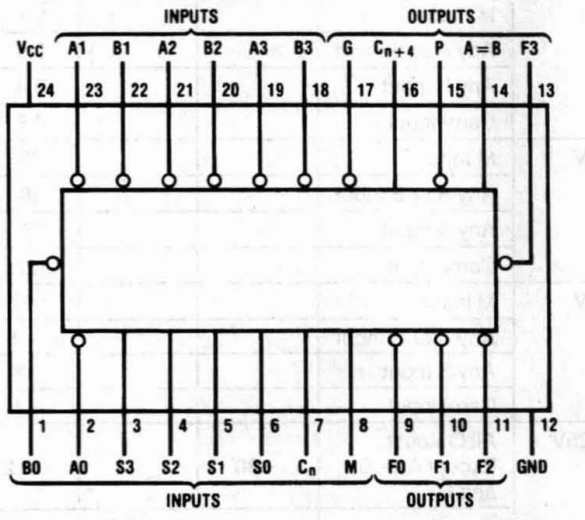
If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_{n+4}) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word-lengths can be performed without external circuitry.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin-for-pin compatible with Schottky TTL counterpart
- Improved AC performance over Schottky counterpart
- Arithmetic operating modes:
  - Addition
  - Subtraction
  - Shift operand A one position
  - Magnitude comparison
  - Plus twelve other arithmetic operations
- Logic function modes:
  - Exclusive-OR
  - Comparator
  - AND, NAND, OR, NOR
  - Plus ten other logic operations
- Full look-ahead for high speed operations on long words

Connection Diagram

Dual-In-Line Package


INPUTS
OUTPUTS
VCC A1 B1 A2 B2 A3 B3 G Cn+4 P A=B F3
24 23 22 21 20 19 18 17 16 15 14 13
1 2 3 4 5 6 7 8 9 10 11 12
B0 A0 S3 S2 S1 S0 Cn M F0 F1 F2 GND
INPUTS
OUTPUTS

TL/F/6336–1

Top View

Order Number DM74AS881BNT
See NS Package Number N24C*

Pin Designations

Designation	Pin Number	Function
A3, A2, A1, A0	19, 21, 23, 2	Word A Inputs
B3, B2, B1, B0	18, 20, 22, 1	Word B Inputs
S3, S2, S1, S0	3, 4, 5, 6	Function-Select Inputs
C_n	7	Inv. Carry Input
M	8	Mode Control Input
F3, F2, F1, F0	13, 11, 10, 9	Function Outputs
A = B	14	Comparator Output
P	15	Carry Propagate Output
C_{n+4}	16	Inv. Carry Output
G	17	Carry Generate Output
V_{CC}	24	Supply Voltage
GND	12	Ground

*Contact your local NSC representative about surface mount (M) package availability.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		Min	Typ	Max	Units
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			V
V_{OH}	High Level Output Voltage A = B Output Only				5.5	V
I_{OH}	High Level Output Current	All Outputs Except A = B and $\overline{G}$			−2	mA
		$\overline{G}$			−3	
I_{OL}	Low Level Output Current	All Outputs Except $\overline{G}$			20	mA
		$\overline{G}$			48	
T_A	Operating Free Air Temperature		0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V, I_{OH} = −2 mA	Any Output Except A = B	V_{CC} − 2			V
		V_{CC} = 4.5V, I_{OH} = −3 mA	$\overline{G}$	2.4	3.4		
I_{OH}	High Level Output Current	V_{CC} = 4.5V, V_{OH} = 5.5V	A = B			0.1	mA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 20 mA	Any Output Except $\overline{G}$		0.3	0.5	V
		V_{CC} = 4.5V, I_{OL} = 48 mA	$\overline{G}$		0.4	0.5	
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_I = 7V	M Input			0.1	mA
			Any A or B Input			0.3	
			Any S Input			0.4	
			Carry Input			0.6	
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_I = 2.7V	M Input			20	μA
			Any A or B Input			60	
			Any S Input			80	
			Carry Input			120	
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_I = 0.4V	M Input			−0.5	mA
			Any A or B Input			−1.5	
			Any S Input			−2	
			Carry Input			−3	
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V	All Outputs Except A = B and $\overline{G}$	−30		−112	mA
			$\overline{G}$		−165		
I_{CC}	Supply Current	V_{CC} = 5.5V			70	104	mA

Note 1: All typical values are at V_{CC} = 5V, T_A = 25°C.

Switching Characteristics

Symbol	Parameter	Conditions	From (Input)	To (Output)	C_L = 50 pF (15 pF for A = B), R_L = 500Ω (280Ω for A = B)		Units
					Min	Max	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		C_n	C_{n+4}	2	9	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	9	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 4.5V, S1 = S2 = 0V ($\overline{SUM}$ Mode)	Any A or B	C_{n+4}	2	12	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	12	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 0V, S1 = S2 = 4.5V ($\overline{DIFF}$ Mode)	Any A or B	C_{n+4}	2	16	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	16	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V ($\overline{SUM}$ or $\overline{DIFF}$ Mode)	C_n	Any F	3	9	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				3	9	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 4.5V, S1 = S2 = 0V ($\overline{SUM}$ Mode)	Any A or B	G	2	7	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	7	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 0V, S1 = S2 = 4.5V ($\overline{DIFF}$ Mode)	Any A or B	G	2	9	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	9	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 4.5V, S1 = S2 = 0V ($\overline{SUM}$ Mode)	Any A or B	P	2	8	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	8	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 0V, S1 = S2 = 4.5V ($\overline{DIFF}$ Mode)	Any A or B	P	2	10	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	10	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 4.5V, S1 = S2 = 0V ($\overline{SUM}$ Mode)	A_i or B_i	F_i	2	8	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	8	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 0V, S1 = S2 = 4.5V ($\overline{DIFF}$ Mode)	A_i or B_i	F_i	2	10	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	10	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 4.5V (Logic Mode)	A_i or B_i	F_i	2	11	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	11	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 0V, S1 = S2 = 4.5V ($\overline{DIFF}$ Mode)	Any A or B	A = B	4	21	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				4	21	

Switching Characteristics (Continued)

Symbol	Parameter	Conditions	From (Input)	To (Output)	C_L = 50 pF (15 pF for A = B) R_L = 500Ω (280Ω for A = B)		Units
					Min	Max	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_n = M = S0 = S3 = 4.5V, S1 = S2 = 0V, Equality ($A_i = B_i$ or $A_i \neq B_i$)	Any A or B	P	2	15	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	15	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_n = M = S3 = 4.5V, S1 = S2 = 0V, Equality ($A_i = B_i$ or $A_i \neq B_i$)	Any A or B	C_{n+4}	2	18	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	18	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_n = m = S2 = 4.5V, S0 = S1 = S3 = 0V, ($A_i = B_i$ = H or A_i or B_i = L)	Any A or B	P	2	15	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	15	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_n = M = S2 = 4.5V, S0 = S1 = S3 = 0V, ($A_i = B_i$ = H or A_i or B_i = L)	Any A or B	C_{n+4}	2	19	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output				2	19	

Number of Bits	Typical Addition Times Using AS881 and AS882	Package Count		Carry Method Between ALUs
		Arithmetic/ Logic Units	Look-Ahead Carry Generators	
1 to 4	5	1	0	None
5 to 8	10	2	0	Ripple
9 to 16	14	3 or 4	1	Full Look-Ahead
17 to 64	19	5 to 16	2 to 5	Full Look-Ahead

Functional Description

The DM74AS881B will accommodate active-high or active-low data if the pin designations are interpreted as follows:

Pin Number	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-Low Data (Table I)	$\overline{A}0$	$\overline{B}0$	$\overline{A}1$	$\overline{B}1$	$\overline{A}2$	$\overline{B}2$	$\overline{A}3$	$\overline{B}3$	$\overline{F}0$	$\overline{F}1$	$\overline{F}2$	$\overline{F}3$	C_n	C_{n+4}	$\overline{P}$	$\overline{G}$
Active-High Data (Table II)	A0	B0	A1	B1	A2	B2	A3	B3	F0	F1	F2	F3	$\overline{C}_n$	$\overline{C}_{n+4}$	X	Y

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A − B − 1, which requires an end-around or forced carry to provide A − B.

The DM74AS881B can also be utilized as a comparator. The A = B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A = B). The ALU must be in the subtract mode with C_n = H when performing this comparison. The A = B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU must be placed in the subtract mode by placing the function-select inputs S3, S2, S1, S0 at L, H, H, L, respectively.

Input C_n	Output C_{n+4}	Active-Low Data *(Figure 1)*	Active-High Data *(Figure 2)*
H	H	A ≥ B	A ≤ B
H	L	A < B	A > B
L	H	A > B	A < B
L	L	A ≤ B	A ≥ B

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables I and II and include exclusive-OR, NAND, AND, NOR, and OR functions.

Functional Description (Continued)

TABLE I

Selection				Active-Low Data		
				M = H	M = L; Arithmetic Operations	
S3	S2	S1	S0	Logic Functions	C_n = L (No Carry)	C_n = H (With Carry)
L	L	L	L	$F = \overline{A}$	F = A Minus 1	F = A
L	L	L	H	$F = \overline{AB}$	F = AB Minus 1	F = AB
L	L	H	L	$F = \overline{A} + B$	F = $A\overline{B}$ Minus 1	F = $A\overline{B}$
L	L	H	H	F = 1	F = Minus 1 (2's Comp)	F = Zero
L	H	L	L	$F = \overline{A + B}$	F = A Plus (A + $\overline{B}$)	F = A Plus (A + $\overline{B}$) Plus 1
L	H	L	H	$F = \overline{B}$	F = AB Plus (A + $\overline{B}$)	F = AB Plus (A + $\overline{B}$) Plus 1
L	H	H	L	$F = \overline{A \oplus B}$	F = A Minus B Minus 1	F = A Minus B
L	H	H	H	$F = A + \overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) Plus 1
H	L	L	L	$F = \overline{A}B$	F = A Plus (A + B)	F = A Plus (A + B) Plus 1
H	L	L	H	$F = A \oplus B$	F = A Plus B	F = A Plus B Plus 1
H	L	H	L	F = B	F = $A\overline{B}$ Plus (A + B)	F = $A\overline{B}$ Plus (A + B) Plus 1
H	L	H	H	F = A + B	F = A + B	F = (A + B) Plus 1
H	H	L	L	F = 0	F = A Plus A*	F = A Plus A Plus 1
H	H	L	H	$F = A\overline{B}$	F = AB Plus A	F = AB Plus A Plus 1
H	H	H	L	F = AB	F = $A\overline{B}$ Plus A	F = $A\overline{B}$ Plus A Plus 1
H	H	H	H	F = A	F = A	F = A Plus 1

*Each bit is shifted to the next more significant position.

TABLE II

Selection				Active-High Data		
				M = H	M = L; Arithmetic Operations	
S3	S2	S1	S0	Logic Functions	$\overline{C}_n$ = H (No Carry)	$\overline{C}_n$ = L (With Carry)
L	L	L	L	$F = \overline{A}$	F = A	F = A Plus 1
L	L	L	H	$F = \overline{A + B}$	F = A + B	F = (A + B) Plus 1
L	L	H	L	$F = \overline{A}B$	F = A + $\overline{B}$	F = (A + $\overline{B}$) Plus 1
L	L	H	H	F = 0	F = Minus 1 (2's Comp)	F = Zero
L	H	L	L	$F = \overline{A\overline{B}}$	F = A Plus $A\overline{B}$	F = A Plus $A\overline{B}$ Plus 1
L	H	L	H	$F = \overline{B}$	F = (A + $\overline{B}$) Plus $A\overline{B}$	F = (A + B) Plus $A\overline{B}$ Plus 1
L	H	H	L	$F = A \oplus B$	F = A Minus B Minus 1	F = A Minus B
L	H	H	H	$F = A\overline{B}$	F = $A\overline{B}$ Minus 1	F = $A\overline{B}$
H	L	L	L	$F = \overline{A} + B$	F = A Plus AB	F = A Plus AB Plus 1
H	L	L	H	$F = \overline{A \oplus B}$	F = A Plus B	F = A Plus B Plus 1
H	L	H	L	F = B	F = (A + $\overline{B}$) Plus AB	F = (A + $\overline{B}$) Plus AB Plus 1
H	L	H	H	F = AB	F = AB Minus 1	F = AB
H	H	L	L	F = 1	F = A Plus A*	F = A Plus A Plus 1
H	H	L	H	$F = A + \overline{B}$	F = (A + B) Plus A	F = (A + B) Plus A Plus 1
H	H	H	L	F = A + B	F = (A + $\overline{B}$) Plus A	F = (A + $\overline{B}$) Plus A Plus 1
H	H	H	H	F = A	F = A Minus 1	F = A

*Each bit is shifted to the next more significant position.

Functional Description (Continued)

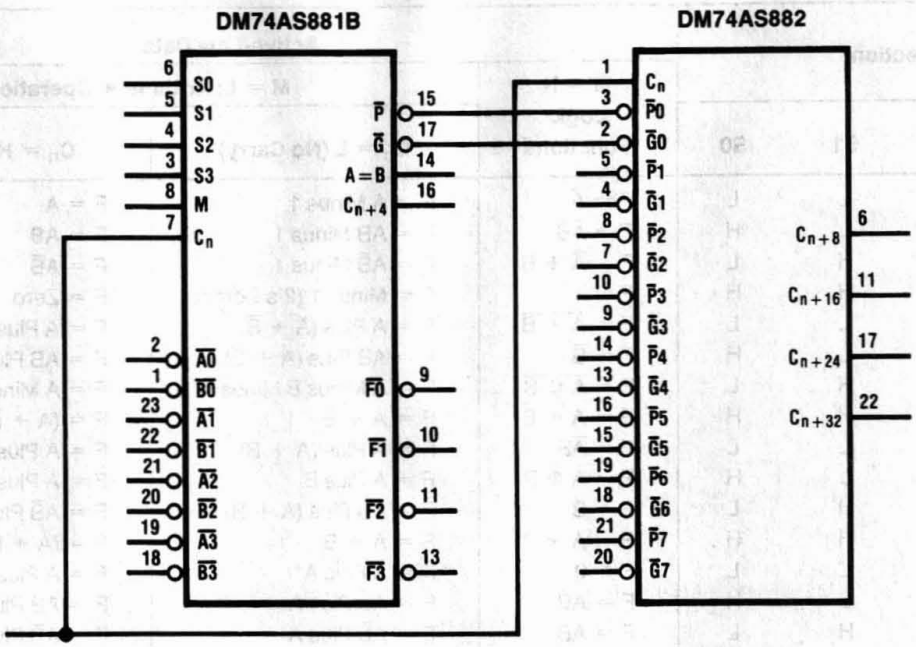


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FIGURE 1 (Use with Table I)

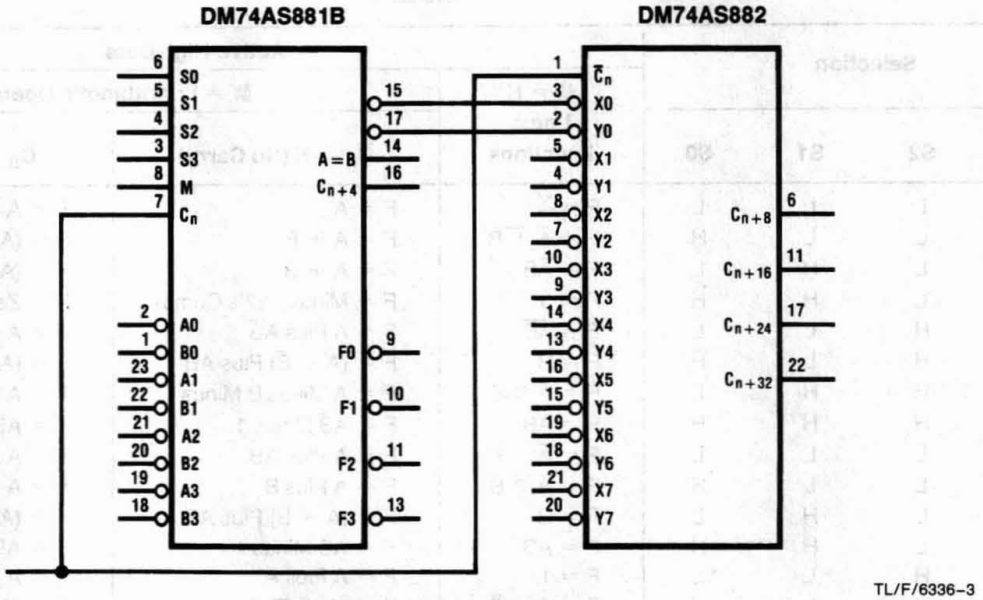

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FIGURE 2 (Use with Table II)

Functional Description (Continued)

The DM74AS881B has the same pinout and same functionality as the DM74AS181B, except for the $\overline{P}$, $\overline{G}$, and C_{n+4} outputs when the device is in the logic mode (M = H).

In the logic mode, the DM74AS881B provides the user with a status check on the input words, A and B, and the output word, F. While in the logic mode, the $\overline{P}$, $\overline{G}$ and C_{n+4} outputs supply status information based upon the following logical combinations:

$$\overline{P} = F0 + F1 + F2 + F3$$

$$\overline{G} = H$$

$$C_{n+4} = PC_n.$$

The combination of signals on the S3 through S0 control lines determines the operation performed on the data words to generate the output bits, F_i. By monitoring the $\overline{P}$ and C_{n+4} outputs, the user can determine if all pairs of input bits are equal (see Function Table for Input Bits Equal/Not Equal) or if any pair of inputs is high (see Function Table for Input Pairs High/Not High). The DM74AS881B has the unique feature of providing an A = B status while the exclusive-OR ($\oplus$) function is being utilized. When the control inputs (S3, S2, S1, S0) equal H, L, L, H, a status check is generated to determine whether all pairs (A_i, B_i) are equal in the following manner: $\overline{P}$ = (A0 $\oplus$ B0) + (A1 $\oplus$ B1) + (A2 $\oplus$ B2) + (A3 $\oplus$ B3). This unique bit-by-bit comparison of the data words, which is available on the totem pole $\overline{P}$ output, is particularly useful when cascading in the DM74AS881B. As the A = B condition is sensed in the first stage, the signal is propagated through the same ports used for carry generation in the arithmetic mode ($\overline{P}$ and $\overline{G}$). Thus, the A = B status is transmitted to the second state more quickly without the need for external multiplexing logic. The A = B open-collector output allows the user to check the validity of the bit-by-bit result by comparing the two signals for parity.

If the user wishes to check for any pair of data inputs ($\overline{A}_i$, $\overline{B}_i$) being high, it is necessary to set the control lines (S3, S2, S1, S0) to L, H, L, L. The data pairs willl then be ANDed together and the results ORed in the following manner: $\overline{P} = \overline{A}0\overline{B}0 + \overline{A}1\overline{B}1 + \overline{A}2\overline{B}2 + \overline{A}3\overline{B}3$.

S3	S2	S1	S0	M	$\overline{P}$ = F0 + F1 + F2 + F3
L	H	L	L	H	$\overline{A}0\overline{B}0 + \overline{A}1\overline{B}1 + \overline{A}2\overline{B}2 + \overline{A}3\overline{B}3$
H	L	L	H	H	(A0 $\oplus$ B0) + (A1 $\oplus$ B1) + (A2 $\oplus$ B2) + (A3 $\oplus$ B3)

SIGNAL DESIGNATIONS

In both *Figures 1* and *2*, the polarity indicators indicate that the associated input or output is active-low with respect to the function shown inside the symbol, and that the symbols are the same in both figures. The signal designations in *Figure 1* agree with the indicated internal functions based on active-low data, and are for use with the logic functions and arithmetic operations shown in Table I. The signal designations have been changed in *Figure 2* to accommodate the logic functions and arithmetic operations for the active-high data given in Table II. The DM74AS181 and DM74AS881B, together with the DM74AS882 and DM74S182, can be used with the signal designation of either *Figure 1* or *Figure 2*.

Function Table for Input Pairs High/Not High
S0 = S1 = S3 = L, S2 = H, and M = H

C_n	Data Inputs				Outputs		
					$\overline{G}$	$\overline{P}$	C_{n+4}
H	A0 = B0	A1 = B1	A2 = B2	A3 = B3	H	L	H
L	A0 = B0	A1 = B1	A2 = B2	A3 = B3	H	L	L
X	A0 ≠ B0	X	X	X	H	H	L
X	X	A1 ≠ B1	X	X	H	H	L
X	X	X	A2 ≠ B2	X	H	H	L
X	X	X	X	A3 ≠ B3	H	H	L

Function Table for Input Bits Equal/Not Equal
S0 = S3 = H, S1 = S2 = L, and M = H

C_n	Data Inputs				Outputs		
					$\overline{G}$	$\overline{P}$	C_{n+4}
H	$\overline{A}0$ or $\overline{B}0$ = L	$\overline{A}1$ or $\overline{B}1$ = L	$\overline{A}2$ or $\overline{B}2$ = L	$\overline{A}3$ or $\overline{B}3$ = L	H	L	H
L	$\overline{A}0$ or $\overline{B}0$ = L	$\overline{A}1$ or $\overline{B}1$ = L	$\overline{A}2$ or $\overline{B}2$ = L	$\overline{A}3$ or $\overline{B}3$ = L	H	L	L
X	$\overline{A}0 = \overline{B}0$ = H	X	X	X	H	H	L
X	X	$\overline{A}1 = \overline{B}1$ = H	X	X	H	H	L
X	X	X	$\overline{A}2 = \overline{B}2$ = H	X	H	H	L
X	X	X	X	$\overline{A}3 = \overline{B}3$ = H	H	H	L

Parameter Measurement Information

$\overline{SUM}$ Mode Test Table
Function Inputs: S0 = S3 = 4.5V, S1 = S2 = M = 0V

Symbol	Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
			Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$	In-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$	In-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	In-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}	In-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	Out-of-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	Out-of-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							

Parameter Measurement Information (Continued)

Logic Mode Test Table
Function Inputs: S1 = S2 = M = 4.5V, S0 = S3 = 0V

Symbol	Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
			Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{A}_i$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}_i$	Out-of-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}_i$	Out-of-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							

$\overline{DIFF}$ Mode Test Table
Function Inputs: S1 = S2 = 4.5V, S0 = S3 = M = 0V

Symbol	Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
			Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$	In-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$	Out-of-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{A}_i$	None	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	In-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	Out-of-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	In-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	Out-of-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B	In-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							

Parameter Measurement Information (Continued)

$\overline{\text{DIFF}}$ Mode Test Table (Continued)
Function Inputs: S1 = S2 = 4.5V, S0 = S3 = M = 0V

Symbol	Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
			Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	Remaining or Any $\overline{F}$	A = B	Out-of-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	C_{n+4} or Any $\overline{F}$	In-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}	Out-of-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{B}_i$	NONE	$\overline{A}_I$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}	In-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							

Input Bits Equal/Not Equal Test Table
Function Inputs: S0 = S3 = M = 4.5V, S1 = S2 = 0V

Symbol	Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
			Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	$\overline{P}$	Out-of-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	$\overline{P}$	Out-of-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	$\overline{P}$	In-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	$\overline{P}$	In-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	C_{n+4}	In-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							

Parameter Measurement Information (Continued)

Input Bits Equal/Not Equal Test Table (Continued)
Function Inputs: S0 = S3 = M = 4.5V, S1 = S2 = 0V

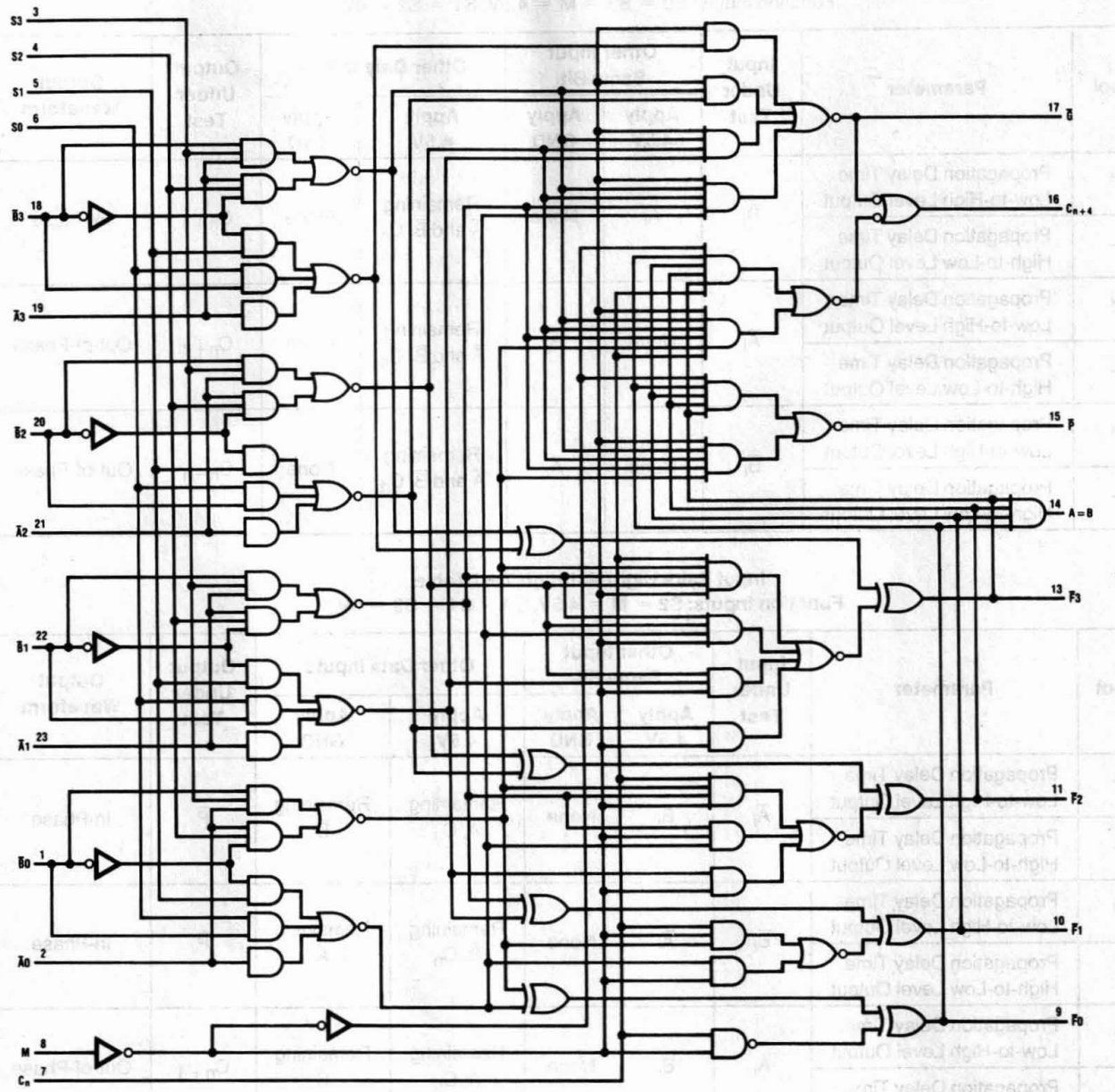
Symbol	Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
			Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	C_{n+4}	In-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	C_{n+4}	Out-of-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{A}$ and $\overline{B}$, C_n	None	C_{n+4}	Out-of-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							

Input Pairs High/Not High Test Table
Function Inputs: S2 = M = 4.5V, S0 = S1 = S3 = 0V

Symbol	Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
			Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$, C_n	Remaining $\overline{B}$	$\overline{P}$	In-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	$\overline{P}$	In-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$, C_n	Remaining $\overline{B}$	C_{n+4}	Out-of-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	C_{n+4}	Out-of-Phase
t_{PHL}	Propagation Delay Time High-to-Low Level Output							

Logic Diagram (Positive Logic)

74AS881B



TL/F/6336–4

National Semiconductor Corporation

DM74AS1000A Quadruple 2-Input NAND Drivers

General Description

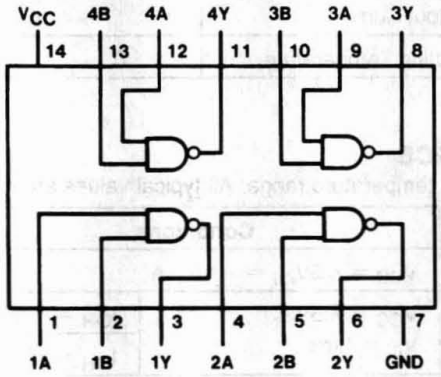
These devices contain four independent 2-input drivers, each of which performs the logic NAND function. The 'AS1000A is a driver version of the 'AS00. Each driver has increased output drive capability to allow the driving of high capacitive loads.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Improved line receiving characteristics

Connection Diagram

Dual-In-Line Package



TL/F/6337–1

Order Number DM74AS1000AN
See NS Package Number N14A*

Function Table

$$Y = \overline{AB}$$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level

L = Low Logic Level

*Contact your local NSC representative about surface mount (M) package availability.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−48	mA
I_{OL}	Low Level Output Current			48	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, V_{IL} = Max	I_{OH} = −3 mA	2.4	3.2		V
			I_{OH} = Max	2			
		I_{OH} = −2 mA, V_{CC} = 4.5V to 5.5V		V_{CC} − 2			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, V_{IH} = 2V, I_{OL} = Max			0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−50	−135	−200	mA
I_{CCH}	Supply Current	Outputs High, V_{CC} = 5.5V, V_I = 0V			2.3	3.5	mA
I_{CCL}	Supply Current	Outputs Low, V_{CC} = 5.5V, V_I = 4.5V			11.5	19	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V, R_L = 500Ω, C_L = 50 pF	1	4	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		1	4	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM74AS1004A Hex Inverting Drivers

General Description

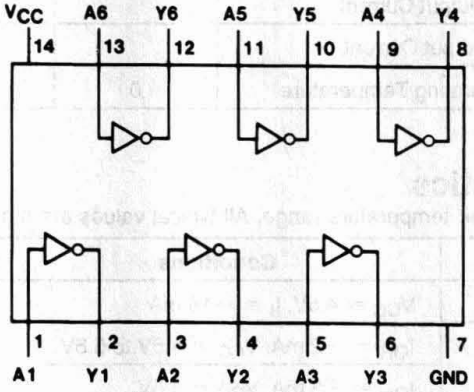
These devices contain six independent 2-input drivers, each of which performs the logic invert/complement function. The 'AS1004A is a driver version of the 'AS04. Each driver has increased output drive capability to allow the driving of high capacitive loads.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process

Connection Diagram

Dual-In-Line Package



TL/F/6338–1

Order Number DM74AS1004AN
See NS Package Number N14A*

Function Table

$A = \overline{Y}$

Input	Output
A	Y
L	H
H	L

H = High Logic Level
L = Low Logic Level

*Contact your local NSC representative about surface mount (M) package availability.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−48	mA
I_{OL}	Low Level Output Current			48	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2 mA, V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
		I_{OH} = −3 mA, V_{CC} = 4.5V		2.4	3.2		
		I_{OH} = Max, V_{CC} = 4.5V		2			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = Max			0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−50	−135	−200	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		3.2	5	mA
			Outputs Low		16	27	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	1	4	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		1	4	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM74AS1008A Quadruple 2-Input AND Driver

General Description

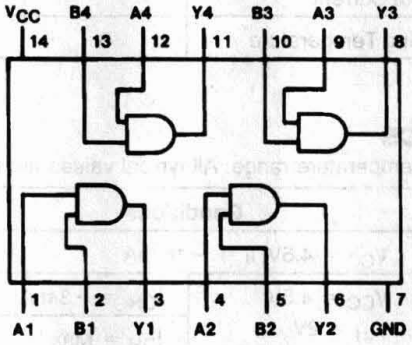
This device contains four independent 2-input drivers, each of which performs the logic AND function. The 'AS1008A is a driver version of the 'AS08. Each driver has increased output drive to allow the driving of high capacitive loads.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Improved line receiving characteristics

Connection Diagram

Dual-In-Line Package



TL/F/6339–1

Order Number DM74AS1008AN
See NS Package Number N14A*

Function Table

$Y = AB$

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

L = Low Logic Level
H = High Logic Level

*Contact your local NSC representative about surface mount (M) package availability.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−48	mA
I_{OL}	Low Level Output Current			48	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, V_{IH} = 2V	I_{OH} = −3 mA	2.4	3.2		V
			I_{OH} = Max	2			V
		I_{OH} = −2 mA, V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, V_{IL} = 0.8V, I_{OL} = Max			0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−50	−135	−200	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = 5.5V, V_I = 4.5V			5.6	9.5	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = 5.5V, V_I = 0V			13.5	22	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V, R_L = 500Ω, C_L = 50 pF	1	6	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		1	6	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM74AS1032A Quadruple 2-Input OR Driver

General Description

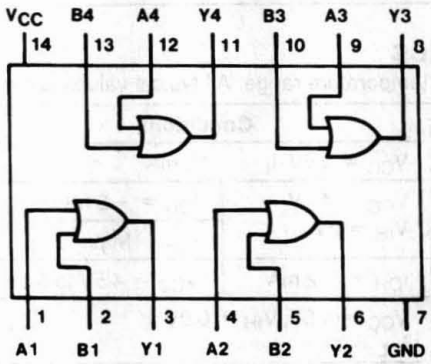
This device contains four independent 2-input drivers, each of which performs the logic OR function. The 'AS1032A is a driver version of the 'AS32A. Each driver has increased output drive capability to allow the driving of high capacitive loads.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Improved line receiving characteristics

Connection Diagram

Dual-In-Line Package



TL/F/6340–1

Order Number DM74AS1032AN
See NS Package Number N14A*

Function Table

$Y = A + B$

Inputs		Output
A	B	Y
L	L	L
H	X	H
X	H	H

L = Low Logic Level
H = High Logic Level
X = Either Low or High Logic Level

*Contact your local NSC representative about surface mount (M) package availability.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−48	mA
I_{OL}	Low Level Output Current			48	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, V_{IH} = 2V	I_{OH} = −3 mA	2.4	3.2		V
			I_{OH} = Max	2			V
		I_{OH} = −2 mA	V_{CC} = 4.5V to 5.5V	V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, V_{IH} = 0.8V, I_{OL} = Max			0.35	0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−50	−135	−200	mA
I_{CCH}	Supply Current	Outputs High, V_{CC} = 5.5V, V_I = 4.5V			7.7	11.5	mA
I_{CCL}	Supply Current	Outputs Low, V_{CC} = 5.5V, V_I = 0V			14.7	24	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V, R_L = 500Ω, C_L = 50 pF	1	6.3	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		1	6.3	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM74AS1034A Hex Non-Inverting Drivers

General Description

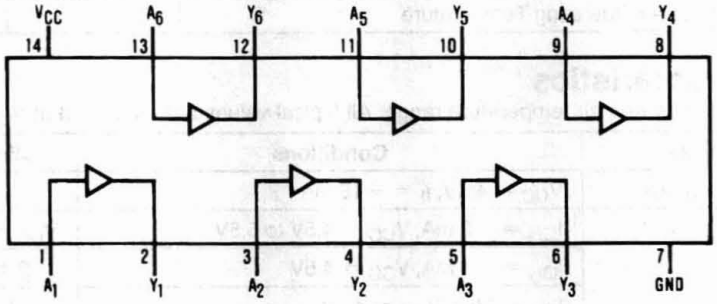
These devices contain six independent drivers, each of which performs the logic indentity function. The 'AS1034A is a driver version of the 'AS34. Each driver has increased output drive capability to allow the driving of high capacitive loads.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process

Connection Diagram

Dual-In-Line Package



TL/F/6341–1

Order Number DM74AS1034AN
See NS Package Number N14A*

Function Table

A = Y

Input A	Output Y
L	L
H	H

L = Low Logic Level
H = High Logic Level

*Contact your local NSC representative about surface mount (M) package availability.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−48	mA
I_{OL}	Low Level Output Current			48	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2 mA, V_{CC} = 4.5V to 5.5V		V_{CC} − 2			V
		I_{OH} = −3 mA, V_{CC} = 4.5V		2.4	3.2		V
		I_{OH} = Max, V_{CC} = 4.5V		2			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V I_{OL} = Max		0.35		0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−50	−135	−200	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		9	15	mA
			Outputs Low		21	35	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	1	6	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		1	6	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM74AS1036A Quad 2-Input NOR Drivers

General Description

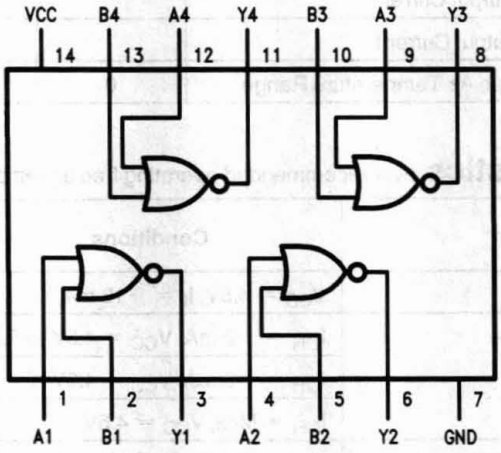
These devices contain four independent drivers, each of which performs the logic NOR function. Each driver has increased output drive capability, allowing the driving of high capacitive loads.

Features

- Switching specifications at 50 pF
- Switching specification guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process

Connection Diagram

Dual-In-Line Package



TL/F/6342–1

Order Number DM74AS1036AN
See NS Package Number N14A*

Function Table

$$Y = \overline{A + B}$$

Inputs		Output
A	B	Y
L	L	H
X	H	L
H	X	L

H = High Level
L = Low Level
X = Don't Care

*Contact your local NSC representative about surface mount (M) package availability.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−48	mA
I_{OL}	Low Level Output Current			48	mA
T_A	Operating Free Air Temperature Range	0		70	°C

Electrical Characteristics over recommended operating free air temperature range

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA			−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2 mA, V_{CC} = 4.5V to 5.5V	V_{CC} − 2			V
		I_{OH} = −3 mA, V_{CC} = 4.5V	2.4	3.2		
		I_{OH} = Max, V_{CC} = 4.5V	2			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = Max, V_{IH} = 2V		0.35	0.5	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = 5.5V, V_I = 7V			100	μA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_I = 2.7V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_I = 0.4V			−500	μA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V	−50	−135	−200	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = 5.5V		4.7	7	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = 5.5V		15.3	23	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions (Note 1)	Min	Max	Units
t_{PLH}	Propagation Delay Time, Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	1	4.3	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output		1	4.3	ns

Note 1: See Section 1 for test waveforms and output load.

Note 2: Typical values are measured at V_{CC} = 5V and T_A = 25°C.

National Semiconductor Corporation

DM74AS1804 Hex 2-Input NAND Drivers

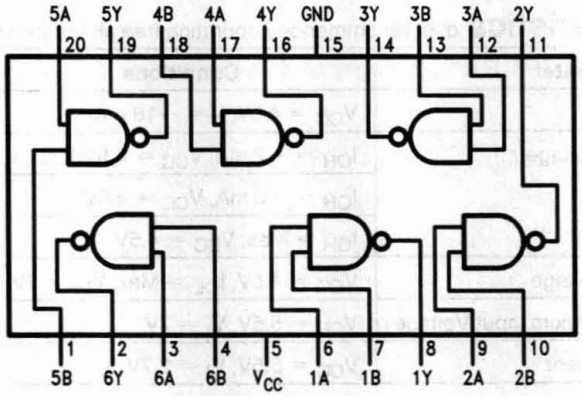
General Description

These devices contain six independent 2-Input drivers each of which performs the logic NAND function. The 'AS1804 is equivalent to the 'AS804B but the supply voltage and ground pins are centered in the package. This positioning of the supply voltage and ground pins reduce the lead inductance of these pins. This reduction of lead inductance will minimize noise generated onto either the supply voltage or ground bus which is significant in high current switching applications.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Centered V_{CC} and GND configuration provides minimum lead inductance for high current switching applications
- High capacitive drive capability

Connection Diagram



TL/F/8619–1

Order Number DM74AS1804N
See NS Package Number N20A

Function Table

$$Y = \overline{A \cdot B}$$

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−48	mA
I_{OL}	Low Level Output Current			48	mA
T_A	Operating Free Air Temperature Range	0		70	°C

Electrical Characteristics over recommended operating free air temperature range

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA			−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2 mA, V_{CC} = 4.5V to 5.5V	V_{CC} −2			V
		I_{OH} = −3 mA, V_{CC} = 4.5V	2.4	3.2		
		I_{OH} = Max, V_{CC} = 4.5V	2			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = Max, V_{IH} = 2V			0.5	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = 5.5V, V_I = 7V			100	μA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_I = 2.7V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_I = 0.4V			−500	μA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V	−50	−135	−200	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = 5.5V		3.5	5	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = 5.5V		16	27	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions (Note 1)	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	1	4	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		1	4	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM74AS1805 Hex 2-Input NOR Drivers

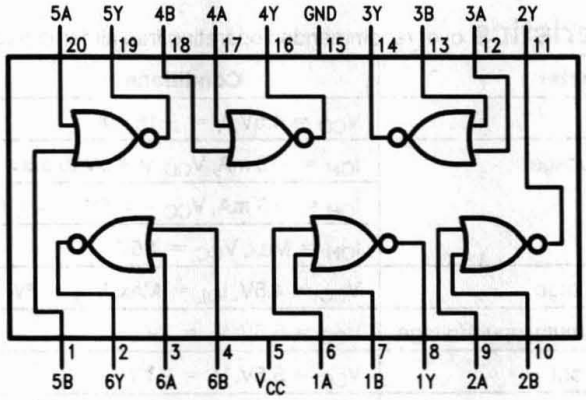
General Description

These devices contain six independent 2-Input drivers each of which performs the logic NOR function. The 'AS1805 is equivalent to the 'AS805B but the supply voltage and ground pins are centered in the package. This positioning of the supply voltage and ground pins reduce the lead inductance of these pins. This reduction of lead inductance will minimize noise generated onto either the supply voltage or ground bus which is significant in high current switching applications.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Centered V_{CC} and GND configuration provides minimum lead inductance for high current switching applications
- High capacitive drive capability

Connection Diagram



TL/F/8618–1

Order Number DM74AS1805N
See NS Package Number N20A

Function Table

$$Y = \overline{A + B}$$

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature	0°C to 70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−48	mA
I_{OL}	Low Level Output Current			48	mA
T_A	Operating Free Air Temperature Range	0		70	°C

Electrical Characteristics over recommended operating free air temperature range

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA			−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2 mA, V_{CC} = 4.5V to 5.5V	V_{CC} −2			V
		I_{OH} = −3 mA, V_{CC} = 4.5V	2.4	3.2		
		I_{OH} = Max, V_{CC} = 4.5V	2			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = Max, V_{IH} = 2V			0.5	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = 5.5V, V_I = 7V			100	μA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_I = 2.7V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_I = 0.4V			−500	μA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V	−50	−135	−200	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = 5.5V		6.5	10	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = 5.5V		20	32	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions (Note 1)	Min	Max	Units
T_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	1	4.3	ns
T_{PHL}	Propagation Delay Time High to Low Level Output		1	4.3	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM74AS1808 Hex 2-Input AND Drivers

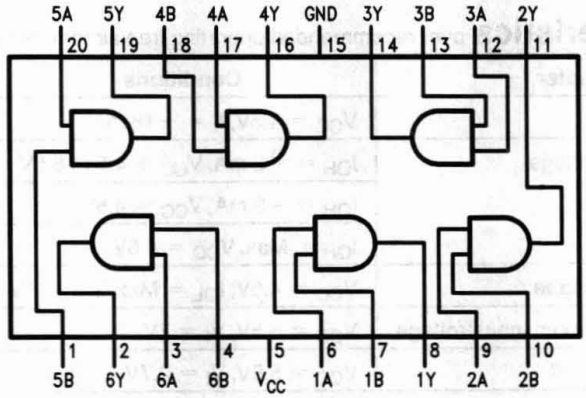
General Description

These devices contain six independent 2-Input drivers each of which performs the logic AND function. The 'AS1808 is equivalent to the 'AS808 but the supply voltage and ground pins are centered in the package. This positioning of the supply voltage and ground pins reduce the lead inductance of these pins. This reduction of lead inductance will minimize noise generated onto either the supply voltage or ground bus which is significant in high current switching applications.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Centered V_{CC} and GND configuration provides minimum lead inductance for high current switching applications
- High capacitive drive capability

Connection Diagram



TL/F/8620–1

Order Number DM74AS1808N
See NS Package Number N20A

Function Table

$Y = A \cdot B$

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Unit
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−48	mA
I_{OL}	Low Level Output Current			48	mA
T_A	Operating Free Air Temperature Range	0		70	°C

Electrical Characteristics over recommended operating free air temperature range

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA			−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2 mA, V_{CC} = 4.5 to 5.5V	V_{CC} −2			V
		I_{OH} = −3 mA, V_{CC} = 4.5V	2.4	3.2		
		I_{OH} = Max, V_{CC} = 4.5V	2			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = Max, V_{IH} = 2V			0.5	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = 5.5V, V_I = 7V			100	μA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_I = 2.7V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_I = 0.4V			−500	μA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V	−50	−135	−200	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = 5.5V		8	13	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = 5.5V		20	33	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions (Note 1)	Min	Max	Unit
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	1	6	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		1	6	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM74AS1832 Hex 2-Input OR Drivers

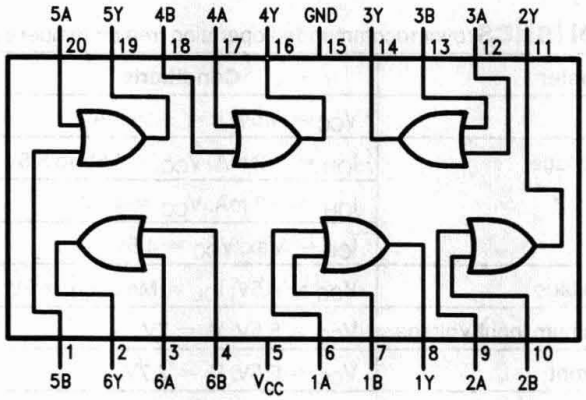
General Description

These devices contain six independent 2-Input drivers each of which performs the logic OR function. The 'AS1832 is equivalent to the 'AS832B but the supply voltage and ground pins are centered in the package. This positioning of the supply voltage and ground pins reduce the lead inductance of these pins. This reduction of lead inductance will minimize noise generated onto either the supply voltage or ground bus which is significant in high current switching applications.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Centered V_{CC} and GND configuration provides minimum lead inductance for high current switching applications
- High capacitive drive capability

Connection Diagram



TL/F/8621–1

Order Number DM74AS1832N
See NS Package Number N20A

Function Table

$Y = A + B$

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Unit
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−48	mA
I_{OL}	Low Level Output Current			48	mA
T_A	Operating Free Air Temperature Range	0		70	°C

Electrical Characteristics over recommended operating free air temperature range

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA			−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2 mA, V_{CC} = 4.5V to 5.5V	V_{CC} −2			V
		I_{OH} = −3 mA, V_{CC} = 4.5V	2.4	3.2		
		I_{OH} = Max, V_{CC} = 4.5V	2			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = Max, V_{IH} = 2V			0.5	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = 5.5V, V_I = 7V			100	μA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_I = 2.7V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_I = 0.4V			−500	μA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V	−50	−135	−200	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = 5.5V		11	17	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = 5.5V		22	36	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions (Note 1)	Min	Max	Unit
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	1	6.3	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		1	6.3	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

PRELIMINARY

DM74AS2620 Octal Bus Transceivers/MOS Drivers

General Description

These octal bus transceivers are designed to drive the capacitive input characteristics of MOS devices and allow asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the enable inputs ($\overline{G}$BA and GAB).

The enable inputs can be used to disable the device so that the buses are effectively isolated.

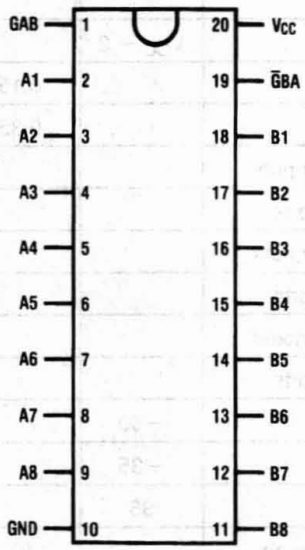
The dual enable configuration gives the 'AS2620 the capability to store data by simultaneous enabling of the $\overline{G}$BA and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. The 8-bit codes appearing on the two sets of buses will be complementary.

Features

- Bidirectional octal bus transceivers for driving MOS devices
- I/O ports have 25Ω series resistors so no external resistors are required
- Local bus-latch capability

Connection Diagram

Dual-In-Line Package

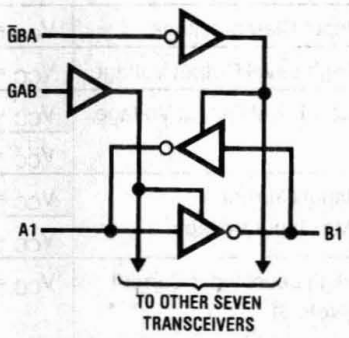


TL/F/6729–1

Top View

Order Number DM74AS2620N
See NS Package Number N20A*

Logic Diagram



TL/F/6729–2

Function Table

Enable Inputs		Operation
$\overline{G}$BA	GAB	
L	L	$\overline{B}$ Data to A Bus
H	H	$\overline{A}$ Data to B Bus
H	L	Isolation
L	H	$\overline{B}$ Data to A Bus, $\overline{A}$ Data to B Bus

*Contact your local NSC representative about surface mount (M) package availability.

This document contains information on a product under development. NSC reserves the right to change or discontinue this product without notice.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	
I/O Ports	5.5V
Other Ports	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V, I_{OH} = −2 mA		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 1 mA			0.15	0.4	V
		V_{CC} = 4.5V, I_{OL} = 12 mA			0.35	0.7	V
I_I	Input Current @ Max Input Voltage	V_{CC} = 5.5V, V_I = 7V	Control Inputs			0.1	mA
		V_{CC} = 5.5V, V_I = 5.5V	A or B Ports			0.1	mA
I_{IH}	High Level Input Current (Note 3)	V_{CC} = 5.5V, V_I = 2.7V	Control Inputs			20	μA
			A or B Ports			70	μA
I_{IL}	Low Level Input Current (Note 3)	V_{CC} = 5.5V, V_{IL} = 0.4V	Control Inputs			−0.5	mA
			A or B Ports			−0.75	mA
I_O	Output Current (Note 2)	V_{CC} = 5.5V, V_O = 2.25V		−50		−150	mA
I_{OH}	High Level Output Current	V_{CC} = 4.5V, V_O = 2V		−35			mA
I_{OL}	Low Level Output Current	V_{CC} = 4.5V, V_O = 2V		35			mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		62	100	mA
			Outputs Low		74	121	mA
			Outputs Disabled		48	77	mA

Note 1: All typical values are at V_{CC} = 5V, T_A = 25°C.

Note 2: The output conditions have been chosen to produce a current that closely approximates one half of the true short circuit output current, I_{OS}.

Note 3: For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	From (Input)	To (Output)	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	V_{CC} = 4.5V to 5.5V C_L = 50 pF R1 = 500Ω R2 = 500Ω T_A = Min to Max	A	B	1	8	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		A	B	1	6.5	ns
t_{PLH}	Propagation Delay Time Low to High Level Output		B	A	1	8	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		B	A	1	6.5	ns
t_{PZH}	Output Enable Time to High Level Output		$\overline{G}$BA	A	1	10	ns
t_{PZL}	Output Enable Time to Low Level Output		$\overline{G}$BA	A	1	11	ns
t_{PHZ}	Output Disable Time from High Level Output		$\overline{G}$BA	A	1	6	ns
t_{PLZ}	Output Disable Time from Low Level Output		$\overline{G}$BA	A	1	12	ns
t_{PZH}	Output Enable Time to High Level Output		GAB	B	1	8	ns
t_{PZL}	Output Enable Time to Low Level Output		GAB	B	1	8	ns
t_{PHZ}	Output Disable Time from High Level Output		GAB	B	1	11	ns
t_{PLZ}	Output Disable Time from Low Level Output		GAB	B	1	11	ns

Note 1: See Section 1 for test waveforms and output load.

National Semiconductor Corporation

DM74AS2645 TRI-STATE® Bus Transceivers/MOS Drivers

General Description

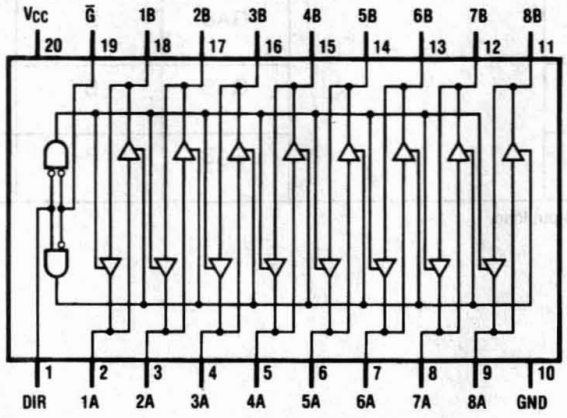
This device contains 8 pairs of logic elements configured as octal bus transceivers. They are designed to drive the capacitive input characteristics of MOS devices and allow asynchronous bidirectional communications between data buses. Data transmission from the A bus to the B bus or from the B bus to the A bus are selectively controlled by (DIR and $\overline{G}$) the direction and enable inputs. This enable input is also used to disable the device so that the buses are effectively isolated.

Features

- Bidirectional octal bus transceivers for driving MOS devices
- I/O ports have 25Ω series resistors so no external resistors are required
- Advanced oxide isolated, ion-implanted Schottky TTL process
- Switching response specified into 500Ω/50 pF load
- Switching specifications guaranteed over full temperature and V_{CC} range

Connection Diagram

Dual-In-Line Package



TL/F/6343–1

Order Number DM74AS2645N
See NS Package Number N20A*

Function Table

Control Inputs		Operation
$\overline{G}$	DIR	
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	Hi-Z

L = Low Logic Level
H = High Logic Level
Hi-Z = High Impedance State
X = Either Low or High Logic Level

*Contact your local NSC representative about surface mount (M) package availability.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V_{CC}	7V
Input Voltage	
Control Inputs	7V
I/O Ports	5.5V
Operating Free Air Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
T_A	Operating Free Air Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V to 5.5V, I_{OH} = −2 mA		V_{CC} − 2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	I_{OL} = −1 mA		0.25	0.4	V
			I_{OL} = 12 mA		0.35	0.7	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IN} = 7V (V_{IN} = 5.5V for A or B Ports)				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IN} = 2.7V	Control Inputs			20	µA
			A or B Ports			70	
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V	Control Inputs			−0.5	mA
			A or B Ports			−0.75	
I_O	Output Drive Current	V_{CC} = 5.5V, V_{OUT} = 2.25V		−50		−150	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		58	95	mA
			Outputs Low		95	155	mA
			TRI-STATE		73	119	mA

Switching Characteristics over recommended operating free air temperature range (Notes 1 and 2)

Symbol	Parameter	From (Input)	To (Output)	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	A or B	B or A	1	10	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A or B	B or A	1	9.5	ns
t_{PZL}	Output Enable Time to Low Level	$\overline{G}$	A or B	1	11.5	ns
t_{PZH}	Output Enable Time to High Level	$\overline{G}$	A or B	1	10.5	ns
t_{PLZ}	Output Disable Time from Low Level	$\overline{G}$	A or B	1	8	ns
t_{PHZ}	Output Disable Time from High Level	$\overline{G}$	A or B	1	12	ns

Note 1: See Section 1 for test waveforms and output load.

Note 2: Switching characteristic conditions are V_{CC} = 4.5V to 5.5V, R_L = 500Ω, C_L = 50 pF.

Section 4

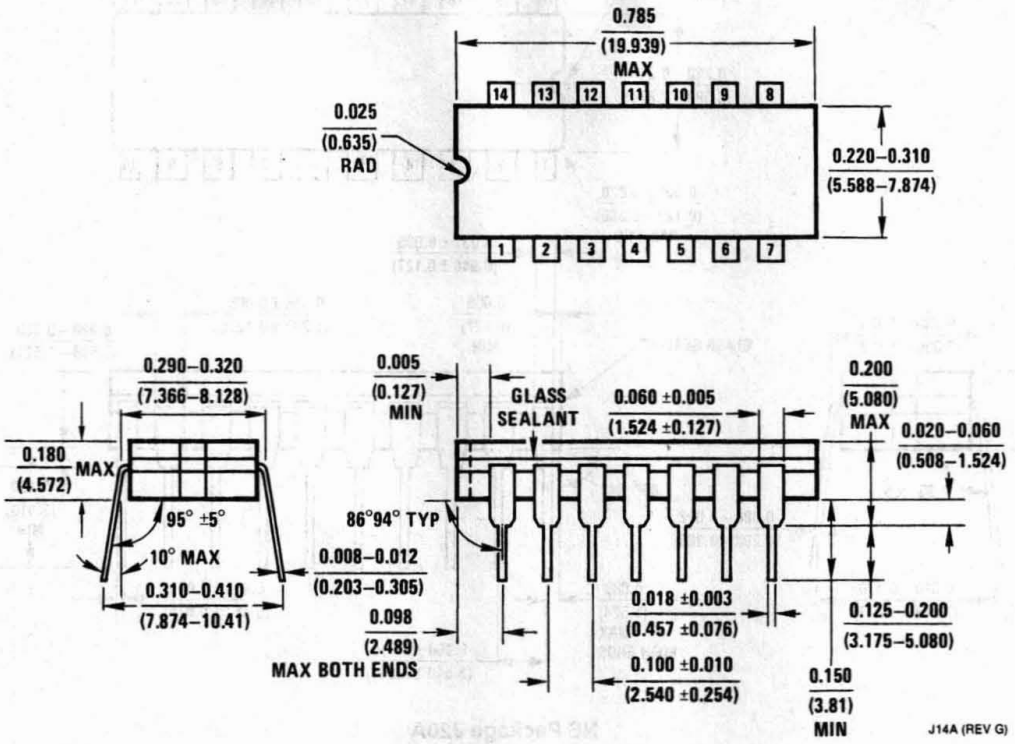
Physical Dimensions/ Appendices

Section 4 Contents

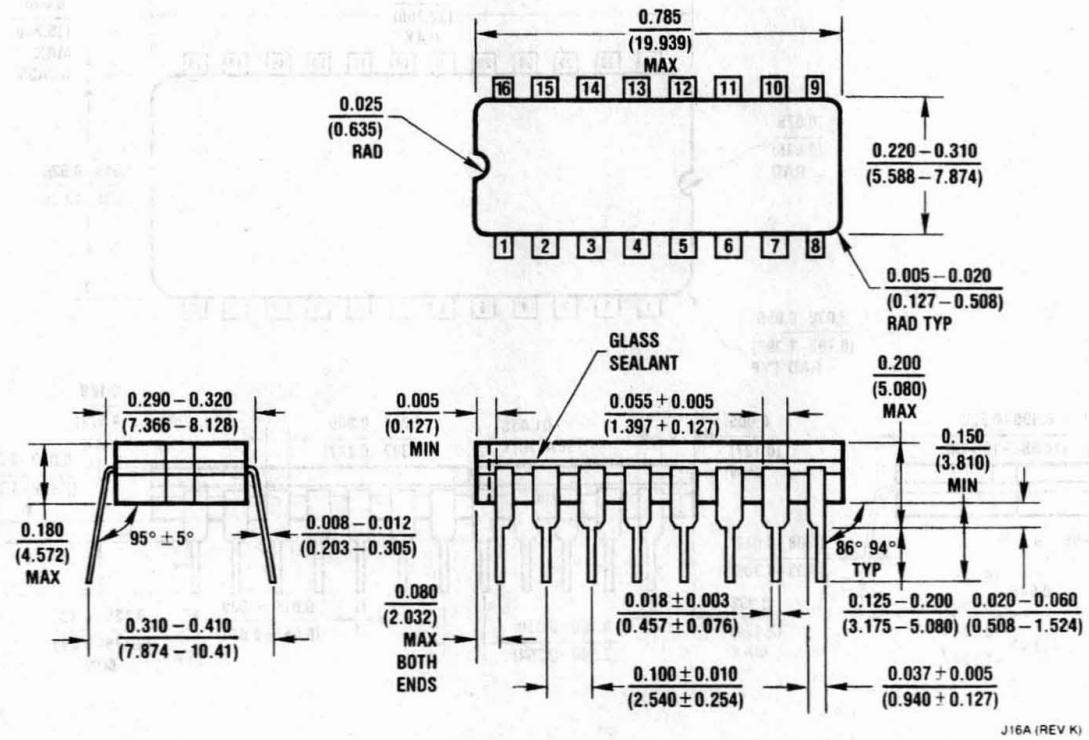
Physical Dimensions 4-3
Data Bookshelf
Sales and Distribution Offices

National Semiconductor Corporation

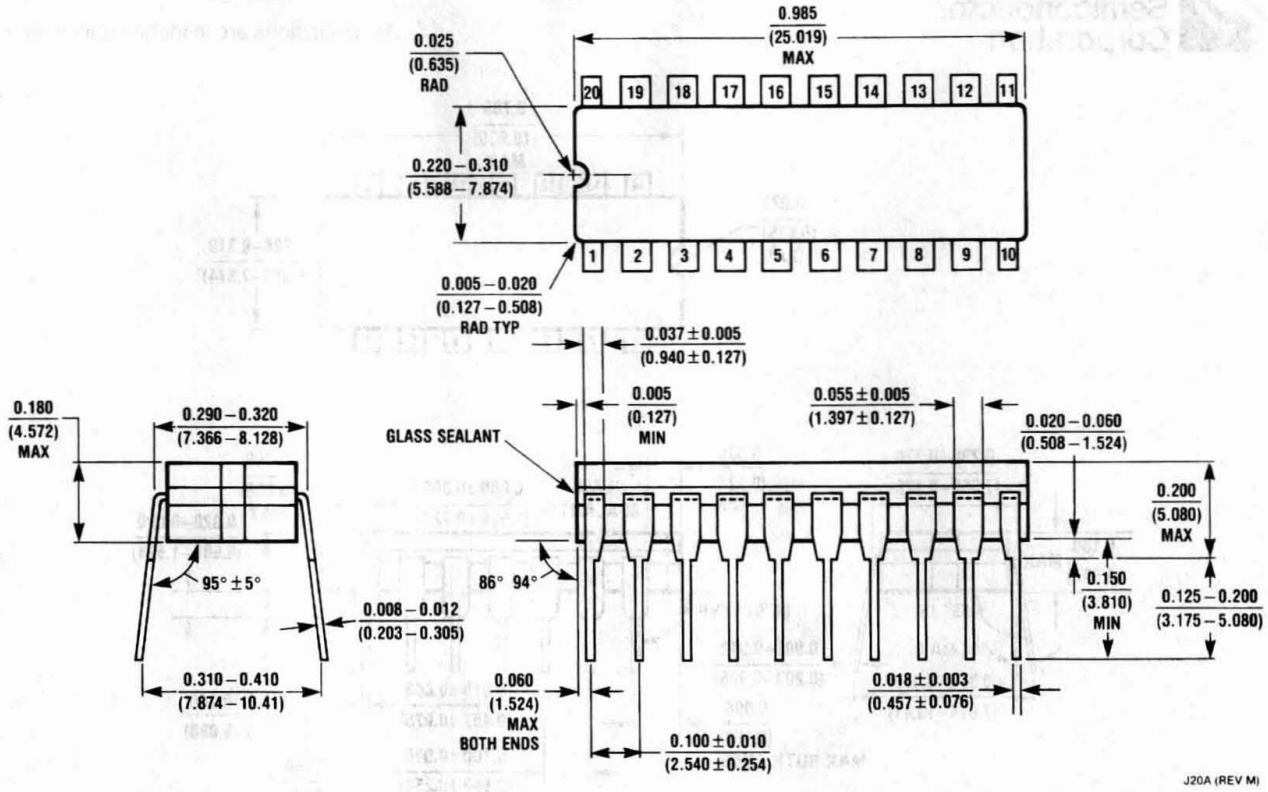
All dimensions are in inches (millimeters)



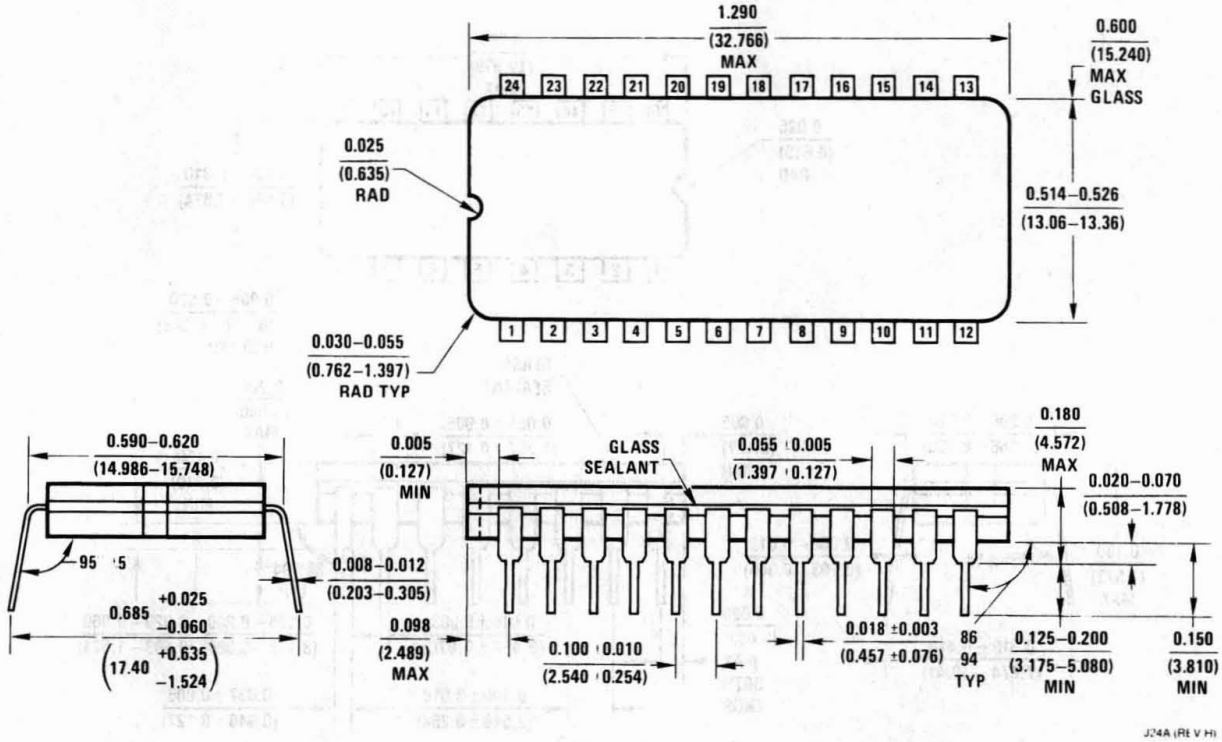
NS Package J14A



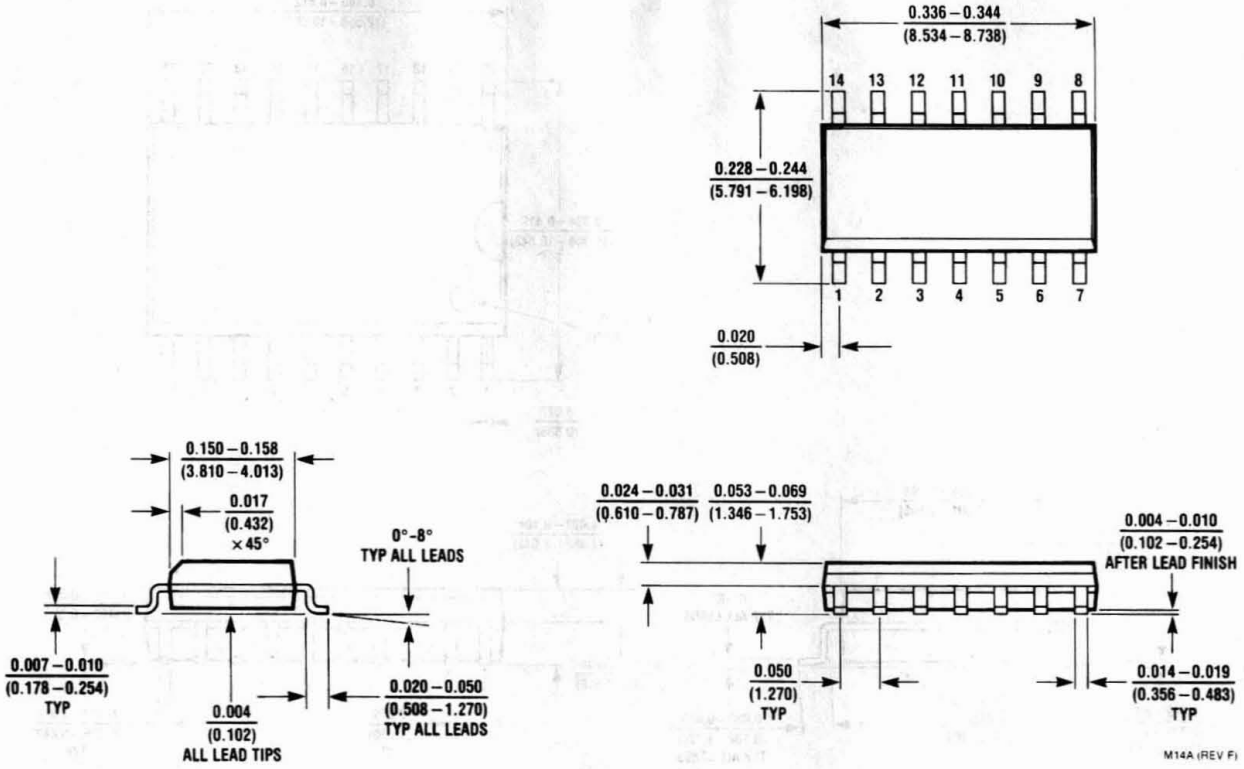
NS Package J16A



NS Package J20A



NS Package J24A



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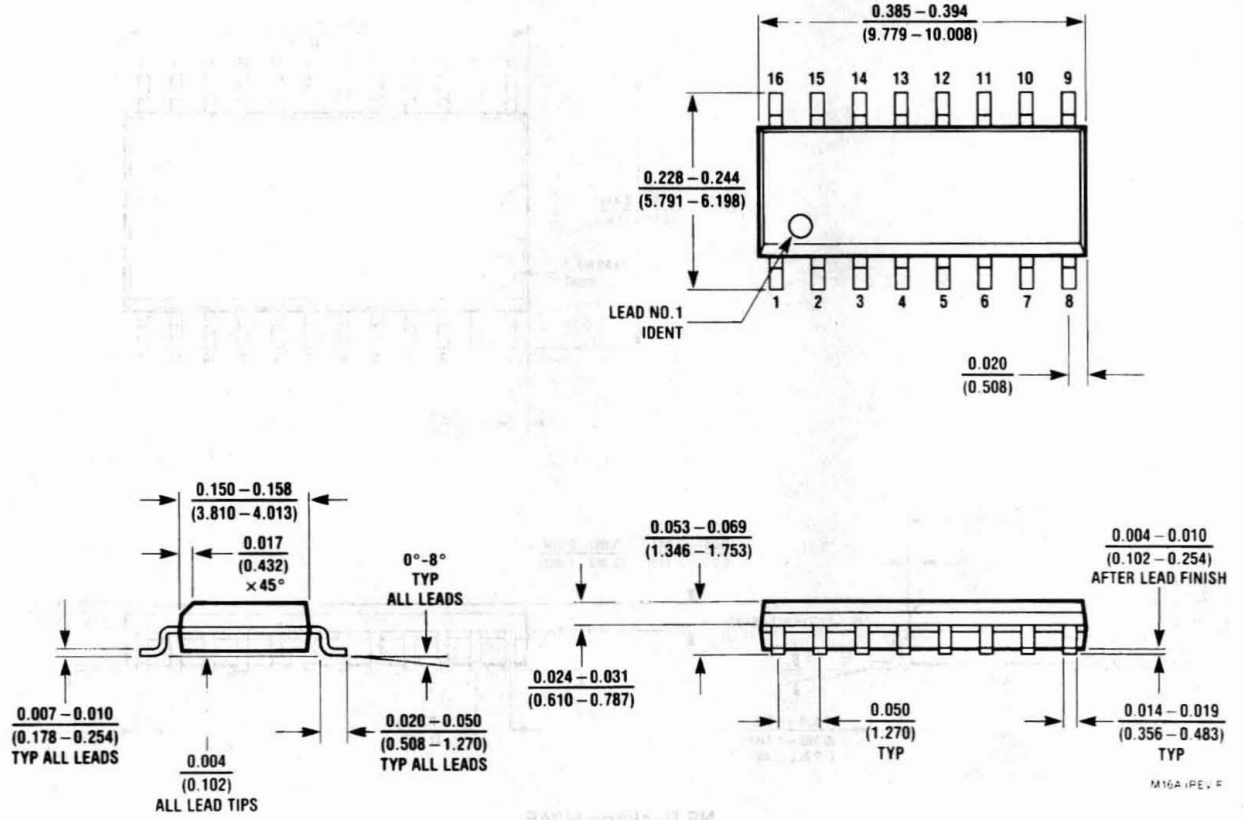

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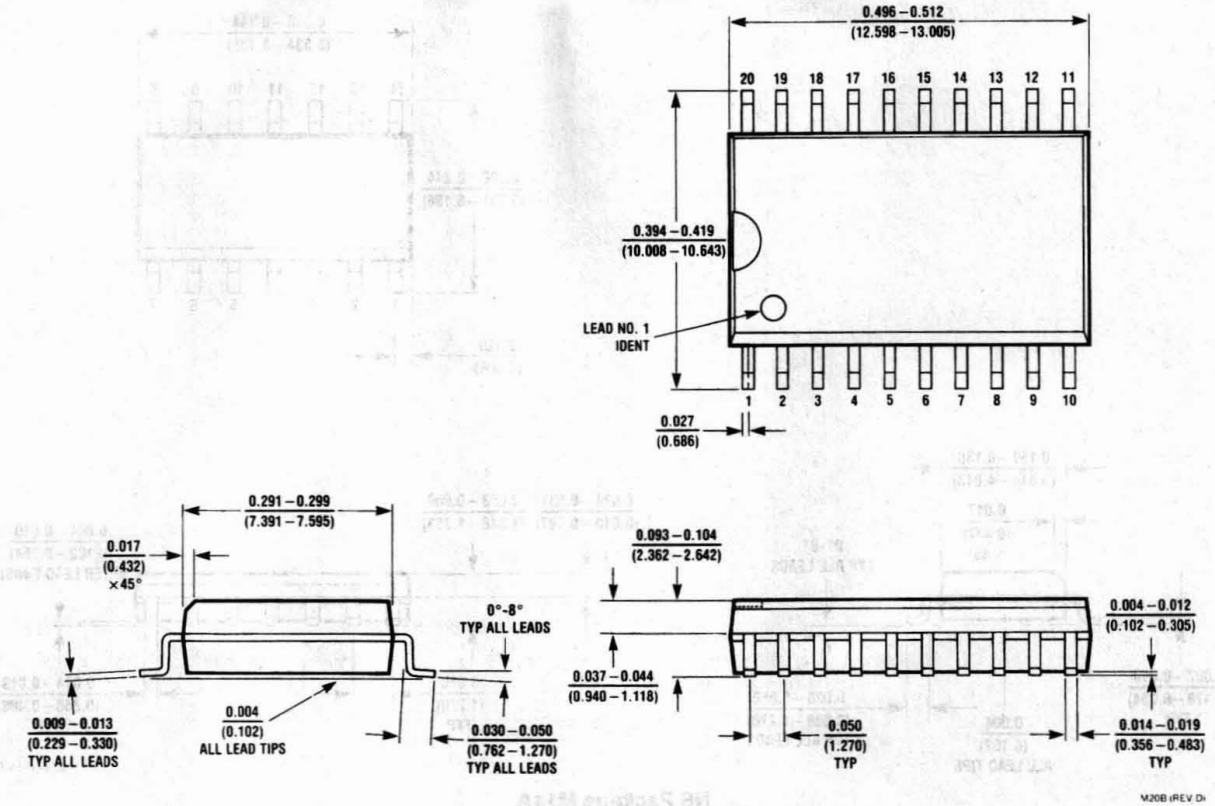

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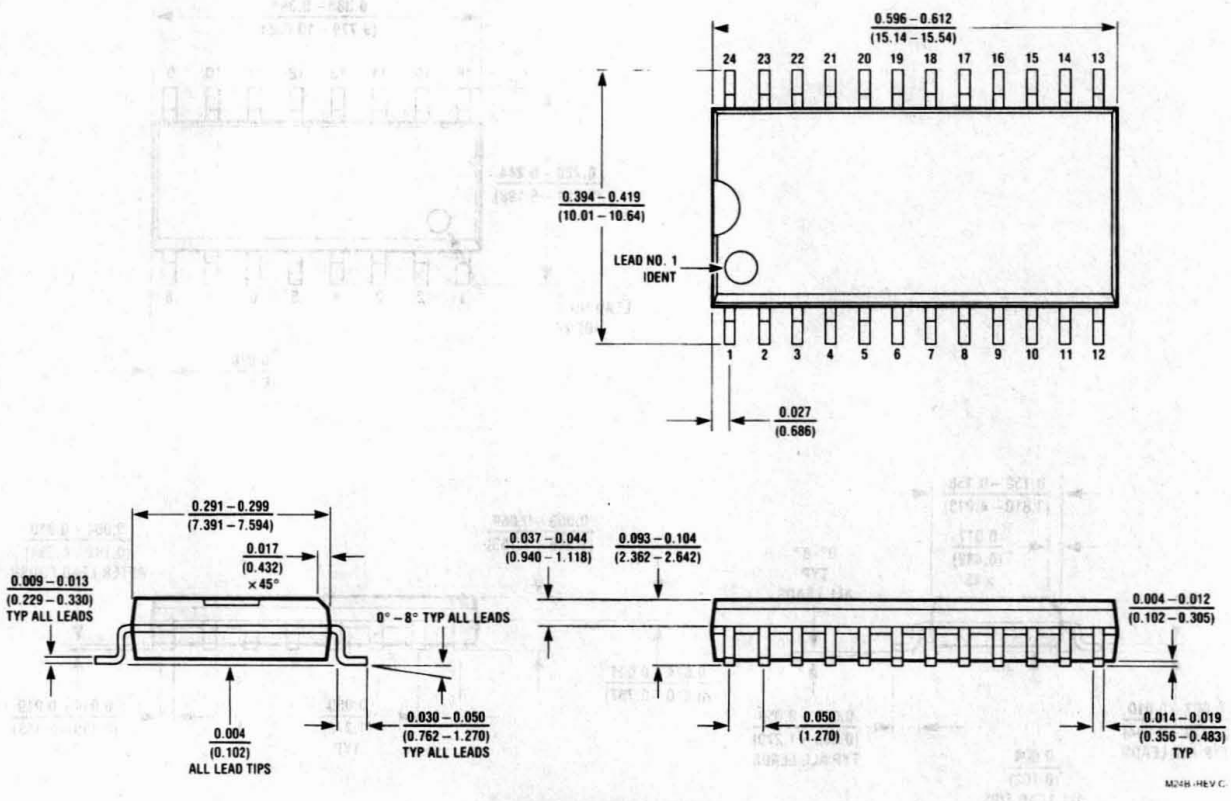

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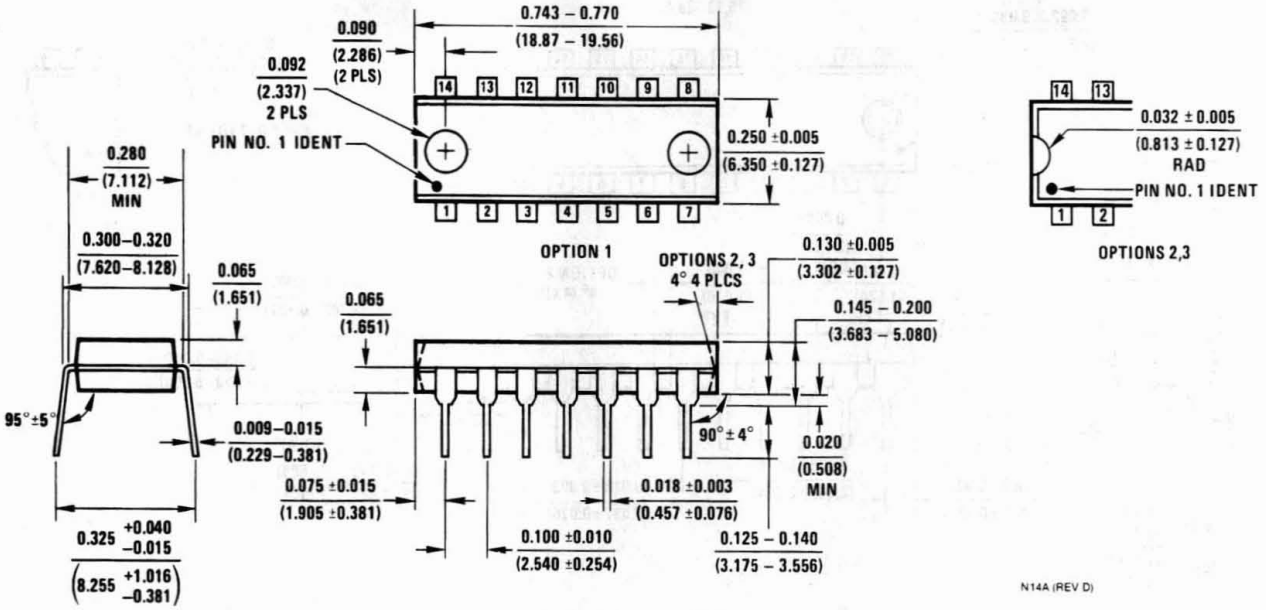

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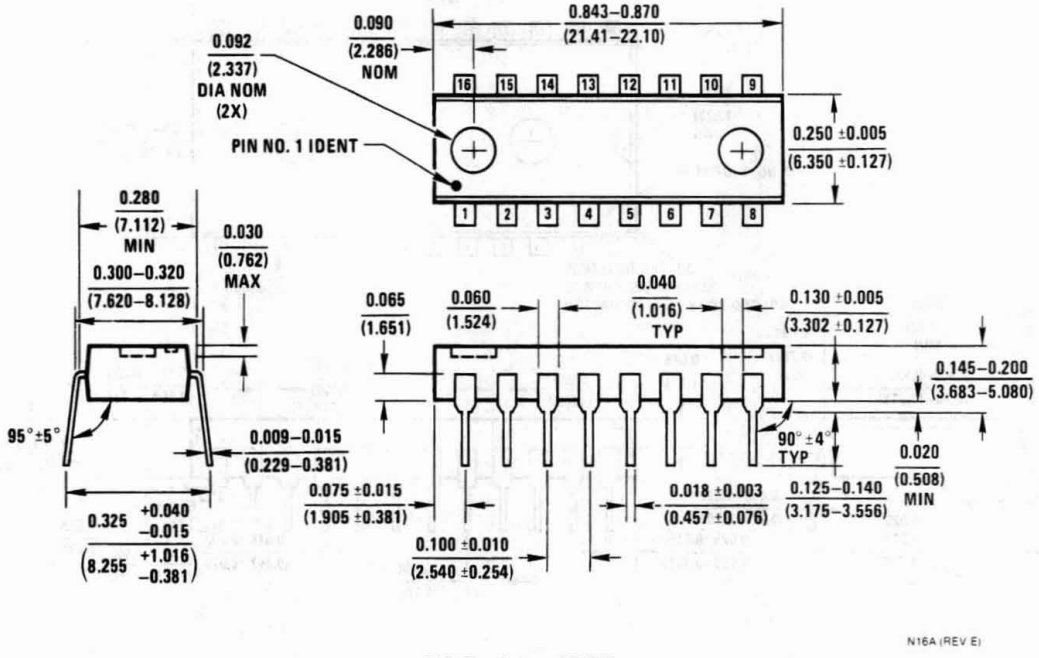

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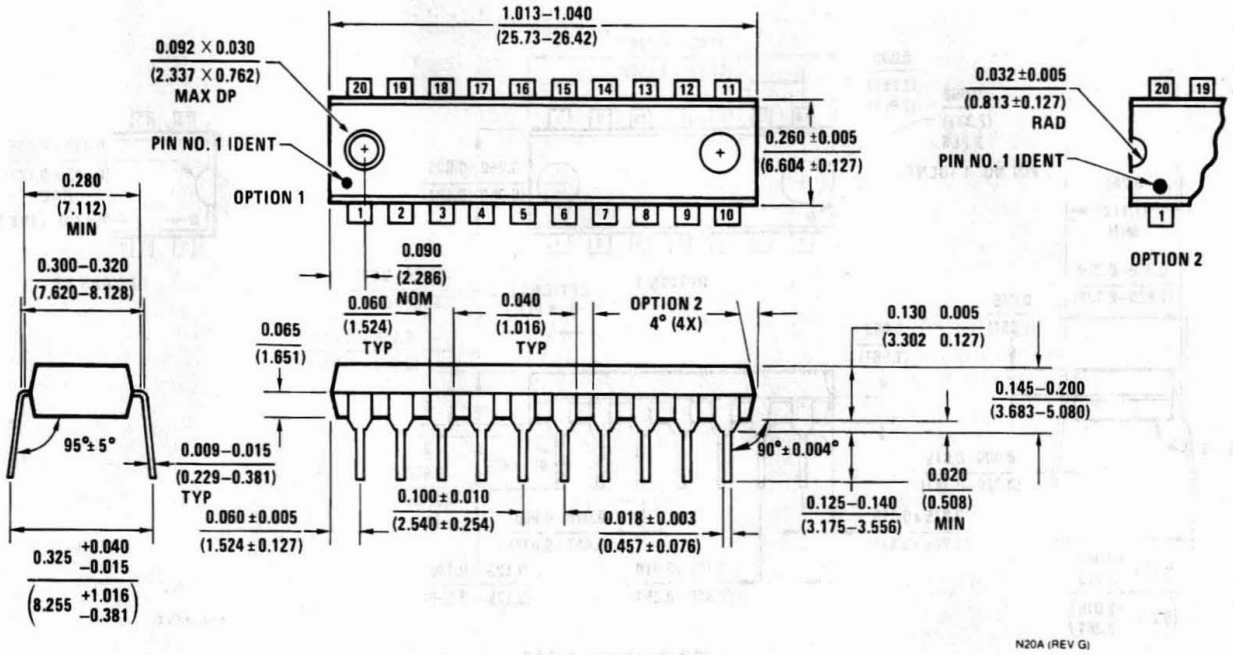

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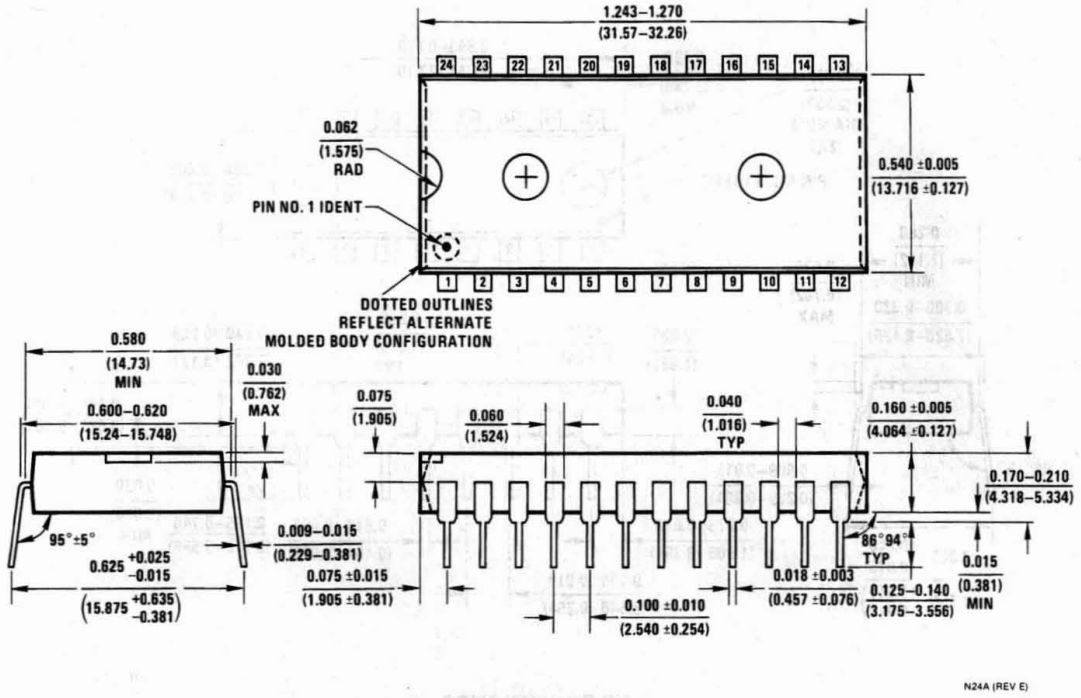

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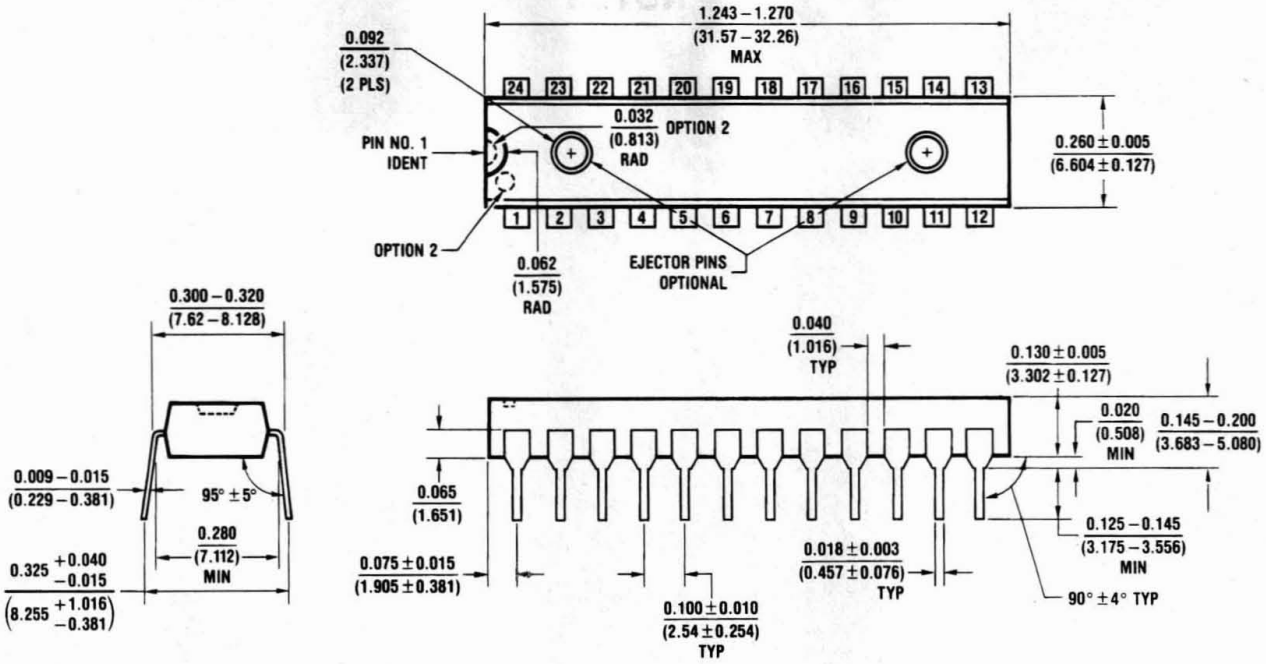

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